INDUSTRY STANDARD LINEAR ICs

2nd EDITION

April 1987

USE IN LIFE SUPPORT MUST BE EXPRESSLY AUTHORIZED

SGS' PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF SGS MICROELETTRONICA SpA. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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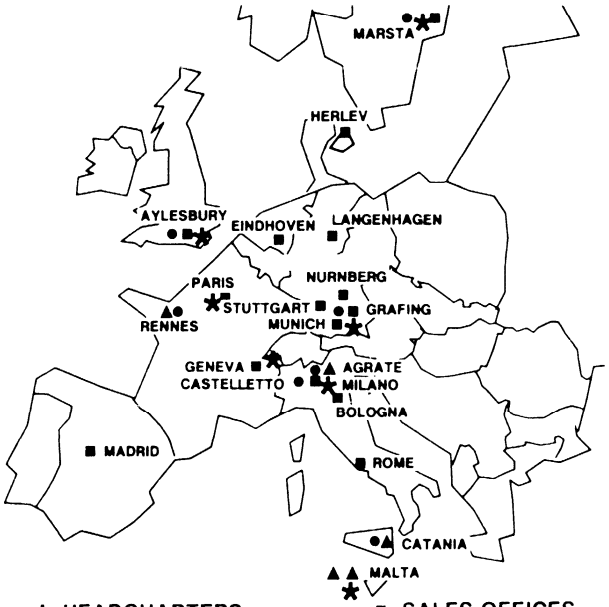
IDENTITY

Late in 1957, SGS was founded around a team of researchers who were already carrying out pioneer work in the field of semiconductors. From that small nucleus, the company has evolved into a Group of Companies, operating on a worldwide basis as a broad range semiconductor producer, with bilings over 300 million dollars and employing over 9500 people.

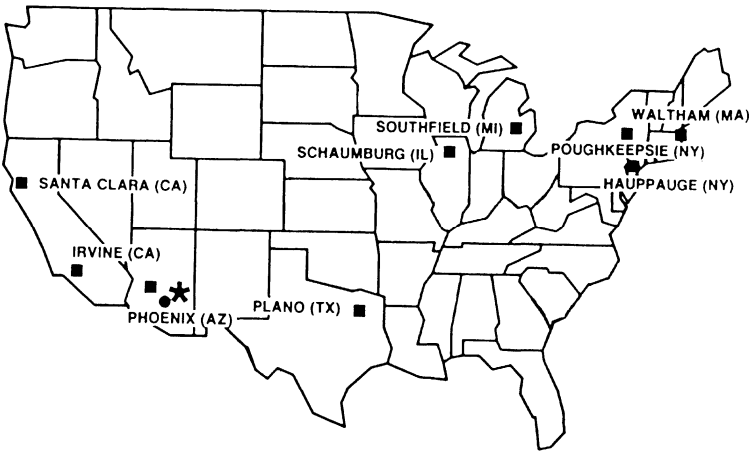
The SGS Group of Companies has now reached a total of 11 subsidiaries, located in Brazil, France, Germany, Italy, Malta, Malaysia, Singapore, Sweden, Switzerland, United Kingdom and the USA.

To go with its logo, the company takes the motto "Technology and Service", underlining the accent given to the development of state-of-the-art technologies and the corporate commitment to offer customers the best quality and service in the industry.

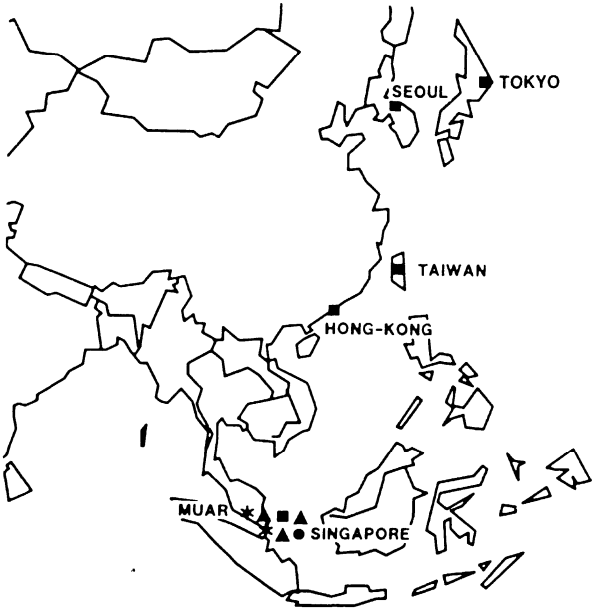
SGS IN EUROPE



SGS IN NORTH AMERICA



SGS IN ASIA/PACIFIC



* HEADQUARTERS
■ SALES OFFICES
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● DESIGN CENTERS

ALPHANUMERICAL INDEX

ALPHANUMERICAL INDEX (continued)

ALPHANUMERICAL INDEX (continued)

ALPHANUMERICAL INDEX

SELECTOR GUIDE

VOLTAGE REGULATORS

STANDARD POSITIVE

I_o max (A)	Type	Regulated output voltage (V)												Package
			5	6	7.5	8	9	10	12	15	18	20	24	
2(*)	L78S00CV		●		●		●	●	●	●	●		●	TO-220
	L78S00CT/T		●		●		●	●	●	●	●		●	TO-3
1.5	LM117K	1.2V ←adjustable→ 37V												TO-3
	LM217K													TO-3
	LM317K													TO-3
	LM317T													TO-220
1	L7800CV		●	●		●			●	●	●	●	●	TO-220
	L7800ABV(**)		●	●		●			●	●	●	●	●	TO-220
	L7800ACV(**)		●	●		●			●	●	●	●	●	TO-220
	L7800CT/T		●	●		●			●	●	●	●	●	TO-3
0.5	L78M00ABV(**)		●	●		●			●	●	●	●	●	TO-220
	L78M00CV		●	●		●			●	●	●	●	●	TO-220
	L78M00CX		●	●		●			●	●	●	●	●	SOT-82
0.15	LM723CD	2V ←adjustable→ 36V												SO-14
	LM723CH													TO-100
	LM723CJ													DIP-14C
	LM723CN													DIP-14P
	LM723J													DIP-14C
	LM723H													TO-100

STANDARD NEGATIVE

I_o max (A)	Type	Regulated output voltage (V)									Package
			-5	-5.2	-8	-12	-15	-18	-20	-24	
1	L7900ACV(**)		●	●	●	●	●	●	●	●	TO-220
	L7900CV		●	●	●	●	●	●	●	●	TO-220
	L7900CT/T		●	●	●	●	●	●	●	●	TO-3

(*)Proprietary SGS selection (**)Output voltage = ±2%

VOLTAGE REGULATORS

LOW DROP

Type	Low drop	Very low drop	Transient protection				Reset	Short circuit protection	Reverse voltage protection	Output voltage			
			±100	±80	±60	±40				5V	8.5V	10V	12V
L387A		●					●	●	●	●			
L487		●		●			●	●	●	●			
L2605	●		●					●	●	●			
L2685	●		●					●	●		●		
L2610	●		●					●	●			●	
L4705		●		●				●	●	●			
L4785		●		●				●	●		●		
L4710		●		●				●	●			●	
L4805		●			●			●	●	●			
L4885		●			●			●	●		●		
L4810		●			●			●	●			●	
L4812		●			●			●	●				●
L4920		●			●			●	●	adjustable			
L4921		●			●			●	●				
L4940/41		●				●		●	●	●			
LM2930A		●				●		●	●	●			
LM2931A		●			●			●	●	●			
LM2935(*)		●			●		●	●	●	●			

PROPRIETARY

I_O max (A)	Type	Regulated output voltage (V)						Package
			5	8.5	10	12		
4	**L296(**)**	5.1V ←adjustable→ 40V						Multiwatt 15
	L4964(**)	5.1V ←adjustable→ 28V						
2.5	**L4960(**)**	1V ←adjustable→ 40V						Heptawatt
2	**L200CH/CV** **L200CT/T**	2.9V ←adjustable→ 36V						Pentawatt TO-3 (4 lead)
1.5	**L4962(**)**	5V ←adjustable→ 40V						Powerdip 12+2+2
	L4940		●					TO-220
1.0	**L4941**		●					TO-220
0.5	**L387A**		●					Pentawatt
	L487		●					Pentawatt
	L2600V		●	●	●			TO-220
	L4700CV		●	●	●			TO-220
	L4800CV		●	●	●	●		TO-220
	L4800CX		●	●	●	●		SOT-82
	L4901-2(*)		●					Heptawatt
	L4903-4(*)		●					Minidip
	L4916			●				Minidip
	L4918			●				Pentawatt
	L4920	1.25V ←adjustable→ 20V						Pentawatt
	L4921							Minidip

(*)Dual regulator (**)Switch-mode

VOLTAGE REGULATORS

HIGH CURRENT SWITCHING

Parameters	Devices			
	L296	L4960	L4962	L4964
Voltage Reference (%)	±2	±4	±4	±3
Output Voltage Range	V_{REF} to 40V	V_{REF} to 40V	V_{REF} to 40V	V_{REF} to 28V
Output Current (A)	4.0	2.5	1.5	4.0
Internal Current Limiting	●	●	●	●
Soft Start	●	●	●	●
Inhibit Input	●			●
Reset Output	●			●
Crowbar Control	●			
Max. Oscillator Frequency (KHz)	200	120	120	120
Separate Oscillator Synch.	●			●
Thermal Protection	●	●	●	●
Package	Multiwatt 15	Heptawatt	12+2+2	Multiwatt 15

SPECIAL FUNCTIONS

Type	Description	Package
TL7700 series	Supply voltage supervisors designed for use as reset controllers in μP systems. During power-up the device tests the supply voltage and keeps the reset outputs active as long as the supply voltage has non reached its nominal voltage value. — V_S = 3V to 18V — Temperature compensated voltage reference — Externally adjustable pulse width	Minidip

OPERATIONAL AMPLIFIERS

STANDARD DUAL OPERATIONAL AMPLIFIERS

Type	Temperature Range (°C)	Input Bias Current (nA)	Input Offset Voltage (mV)	Slew Rate (V/μs)	Supply Current (mA)	Max Supply (V)	Package
LM258 D	−25 to 85	45	2	—	1	±16	SO-8
LM358 D	0 to 70	45	2	—	1	±16	
LM2904 D	−40 to 85	45	2	—	1	±13	
LS204 CM	0 to 70	100	0.5	1	0.8	±18	
LS204 M	−25 to 85	50	0.5	1.5	0.7	±18	
MC1458 CD	0 to 70	80	2	0.5	2.3	±18	
MC1458 D	0 to 70	80	2	0.5	2.3	±18	
NE532 D	0 to 70	45	2	—	1	±16	
LM258 N	−25 to 85	45	2	—	1	±16	Plastic Minidip
LM358 AN	0 to 70	45	2	—	1	±16	
LM358 N	0 to 70	45	2	—	1	±16	
LM2904 N	−40 to 85	45	2	—	1	±13	
LS204 CB	0 to 70	100	0.5	1	0.8	±18	
MC1458 CP1	0 to 70	80	2	0.5	2.3	±18	
MC1458 P1	0 to 70	80	2	0.5	2.3	±18	
NE532 N	0 to 70	45	2	—	—	±16	
TDA2320	0 to 70	100	2	1.5	0.8	±10	
TDA2320A	0 to 70	150	1	1.6	0.8	±18	
LM158 AJ	−55 to 125	20	1	—	1	±16	Ceramic Minidip
LM158 J	−55 to 125	45	2	—	1	±16	
LM258 AJ	−25 to 85	40	2	—	1	±16	
LM258 J	−25 to 85	45	2	—	1	±16	
LM358 AJ	0 to 70	45	2	—	1	±16	
LM358 J	0 to 70	45	2	—	1	±16	
LM2904 J	−40 to 85	45	2	—	1	±16	
MC1458 CU	0 to 70	80	2	0.5	2.3	±18	
MC1458 U	0 to 70	80	2	0.5	2.3	±18	
MC1558 U	−55 to 125	80	1	0.5	2.3	±22	

OPERATIONAL AMPLIFIERS

STANDARD DUAL OPERATIONAL AMPLIFIERS (Continued)

Type	Temperature Range (°C)	Input Bias Current (nA)	Input Offset Voltage (mV)	Slew Rate (V/μs)	Supply Current (mA)	Max Supply (V)	Package
NE532 FE	0 to 70	45	2	—	1	±16	Ceramic Minidip
LS204 ATB	−55 to 125	50	0.5	1.5	0.7	±18	TO-99
LS204 CTB	0 to 70	100	0.5	1	0.8	±18	
LS204 TB	−25 to 85	50	0.5	1.5	0.7	±18	

JFET-INPUT DUAL OPERATIONAL AMPLIFIERS

Type	Temperature Range (°C)	Slew Rate (V/μs)	Input Offset Voltage (mV)	Input Noise Voltage (nV/ Hz)	Supply Current (mA)	Max Supply (V)	Package
TL082 CD	0 to 70	13	5	25	2.8	±18	SO-8
TL082 ID	−25 to 85	13	5	25	2.8	±18	
MC34002 AP	0 to 70	13	1	25	2.8	±18	Plastic Minidip
MC34002 BP	0 to 70	13	3	25	2.8	±18	
MC34002 P	0 to 70	13	5	25	2.8	±18	
TL072 ACP	0 to 70	13	3	18	2.8	±18	
TL072 BCP	0 to 70	13	2	18	2.8	±18	
TL072 CP	0 to 70	13	5	18	2.8	±18	
TL072 IP	−25 to 85	13	5	18	2.8	±18	
TL082 ACP	0 to 70	13	3	25	2.8	±18	
TL082 BCP	0 to 70	13	2	25	2.8	±18	
TL082 CP	0 to 70	13	5	25	2.8	±18	
TL082 IP	−25 to 85	13	5	25	2.8	±18	
MC34002 AU	0 to 70	13	1	25	2.8	±18	Ceramic Minidip
MC34002 BU	0 to 70	13	3	25	2.8	±18	
MC34002 U	0 to 70	13	5	25	2.8	±18	
TL072 ACJG	0 to 70	13	3	18	2.8	±18	
TL072 BCJG	0 to 70	13	2	18	2.8	±18	
TL072 CJG	0 to 70	13	5	18	2.8	±18	
TL072 IJG	−25 to 85	13	5	18	2.8	±18	
TL082 ACJG	0 to 70	13	3	25	2.8	±18	
TL082 BCJG	0 to 70	13	2	25	2.8	±18	
TL082 CJG	0 to 70	13	5	25	2.8	±18	
TL082 IJG	−25 to 85	13	5	25	2.8	±18	
TL082 MJG	−55 to 125	13	3	25	2.8	±18	

OPERATIONAL AMPLIFIERS

STANDARD QUAD OPERATIONAL AMPLIFIERS

Type	Temperature Range (°C)	Input Bias Current (nA)	Input Offset Voltage (mV)	Slew Rate (V/μs)	Supply Current (mA)	Max Supply (V)	Package
LM224 D	0 to 70	45	2	—	1.5	±16	SO-14
LM324 D	0 to 70	45	2	—	1.5	±16	
LM2902 D	−40 to 85	45	2	—	1.5	±13	
LS404 CM	0 to 70	100	1	1	1.5	±18	
LS404 M	−25 to 85	50	1	1.5	1.3	±18	
MC3403 D	0 to 70	200	2	0.6	2.8	±18	
LM224 N	−25 to 85	45	2	—	1.5	±16	Plastic DIP-14
LM324 AN	0 to 70	45	2	—	1.5	±16	
LM324 N	0 to 70	45	2	—	1.5	±16	
LM2902 N	−40 to 85	45	2	—	1.5	±13	
LS404 CB	0 to 70	100	1	1	1.5	±18	
MC3303 P	−40 to 85	200	2	0.6	2.8	±18	
MC3403 P	0 to 70	200	2	0.6	2.8	±18	
LM124 AJ	−55 to 125	20	1	—	1.5	±16	Ceramic DIP-14
LM124 J	−55 to 125	45	2	—	1.5	±16	
LM224 AJ	−25 to 85	40	1	—	1.5	±16	
LM224 J	−25 to 85	45	2	—	1.5	±16	
LM324 AJ	0 to 70	45	2	—	1.5	±16	
LM324 J	0 to 70	45	2	—	1.5	±16	
LM2902J	−40 to 85	45	2	—	1.5	±13	
MC3303 L	−40 to 85	200	2	0.6	2.8	±18	
MC3403 L	0 to 70	200	2	0.6	2.8	±18	
MC3503 L	−55 to 125	200	2	0.6	2.8	±18	

OPERATIONAL AMPLIFIERS

JFET-INPUT QUAD OPERATIONAL AMPLIFIERS

Type	Temperature Range (°C)	Slew Rate (V/μs)	Input Offset Voltage (mV)	Input Noise Voltage (nV/√Hz)	Supply Current (mA)	Max Supply (V)	Package
TL084 CD	0 to 70	12	5	25	5.6	±18	SO-14
TL084 ID	−25 to 85	13	5	25	5.6	±18	
MC34004 BP	0 to 70	13	3	25	5.6	±18	Plastic DIP-14
MC34004 P	0 to 70	13	5	25	5.6	±18	
TL074 ACN	0 to 70	13	3	18	5.6	±18	
TL074 BCN	0 to 70	13	2	18	5.6	±18	
TL074 CN	0 to 70	13	5	18	5.6	±18	
TL074 IN	−25 to 85	13	5	18	5.6	±18	
TL084 ACN	0 to 70	13	3	25	5.6	±18	
TL084 BCN	0 to 70	13	2	25	5.6	±18	
TL084 CN	0 to 70	13	5	25	5.6	±18	
TL084 IN	−25 to 85	13	5	25	5.6	±18	
MC34004 BL	0 to 70	13	3	25	5.6	±18	Ceramic DIP-14
MC34004 L	0 to 70	13	5	25	5.6	±18	
TL074 ACJ	0 to 70	13	3	18	5.6	±18	
TL074 BCJ	0 to 70	13	2	18	5.6	±18	
TL074 CJ	0 to 70	13	5	18	5.6	±18	
TL074 IJ	−25 to 85	13	5	18	5.6	±18	
TL084 ACJ	0 to 70	13	3	25	5.6	±18	
TL084 BCJ	0 to 70	13	2	25	5.6	±18	
TL084 CJ	0 to 70	13	5	25	5.6	±18	
TL084 IJ	−25 to 85	13	5	25	5.6	±18	
TL084 MJ	−55 to125	13	3	25	5.6	±18	

OPERATIONAL AMPLIFIERS

SINGLE OPERATIONAL AMPLIFIERS

Type	Temperature Range (°C)	Frequency Compensat.	CMR (dB)	Input Bias Current (nA)	Slew Rate /V/μs)	Max Supply (V)	Package
LM741 CD	0 to 70	●	90	80	0.5	±18	SO-8
LM741 ID	−25 to 85	●	90	80	0.5	±18	
LM748 CD	0 to 70		90	80	—	±22	
LM748 ID	−25 to 85		90	80	—	±22	
MC1776 CD	0 to 70	●	90	15	0.8	±18	
MC1776 ID	−25 to 85	●	90	15	0.8	±18	
LM741 CN	0 to 70	●	90	80	0.5	±18	Plastic Minidip
LM741 EN	0 to 70	●	90	80	0.5	±18	
LM748 CN	0 to 70		90	80	—	±22	
MC1776 CP1	0 to 70	●	90	15	0.8	±18	
LM741 CJ	0 to 70	●	90	80	0.5	±18	Ceramic Minidip
LM741 EJ	0 to 70	●	90	80	0.5	±18	
LM741 J	−55 to 125	●	90	80	0.5	±18	
LM748 CJ	0 to 70		90	80	—	±22	
LM748 J	−55 to 125		90	80	—	±22	
MC1776 CU	0 to 70	●	90	15	0.8	±18	
MC1776 U	−55 to 125	●	90	15	0.8	±18	
LM741 AH	−55 to 125	●	95	30	0.7	±22	TO-99
LM741 CH	0 to 70	●	90	80	0.5	±18	
LM741 H	0 to 70	●	90	80	0.5	±18	
LM748 CH	0 to 70		90	80	—	±22	
LM748 H	−55 to 125		90	80	—	±22	
MC1776 CG	0 to 70	●	90	15	0.8	±18	
MC1776 G	0 to 70	●	90	15	0.8	±18	

COMPARATORS

Type		Temperature Range (°C)	Input Bias Current (mA)	Input Offset Voltage (mV)	Supply Current (mA)	Max Supply (V)	Package
LM239 D	Quad	−25 to 85	25	2	0.8	36	SO-14
LM339 D	Quad	0 to 70	25	2	0.8	36	
LM2901 D	Quad	−40 to 85	25	2	0.8	36	
MC3302 D	Quad	−40 to 85	30	3	0.8	28	
LM293 D	Dual	−25 to 85	25	2	0.4	36	SO-8
LM311 D	Single	0 to 70	100	2	5.1	36	
LM393 D	Dual	0 to 70	25	2	0.4	36	
LM2903 D	Dual	−40 to 85	25	2	0.4	36	
LM239 N	Quad	−25 to 85	25	2	0.8	36	Plastic DIP-14
LM339 AN	Quad	0 to 70	25	2	0.8	36	
LM339 N	Quad	0 to 70	25	2	0.8	36	
LM2901 N	Quad	−40 to 85	25	2	0.8	36	
MC3302 P	Quad	−40 to 85	30	3	0.8	28	
LM293 N	Duad	−25 to 85	25	2	0.4	36	Plastic Minidip
LM311 N	Single	0 to 70	100	2	5.1	36	
LM393 AN	Dual	0 to 70	25	2	0.4	36	
LM393 N	Dual	0 to 70	25	2	0.4	36	
LM2903 N	Dual	−40 to 84	25	2	0.4	36	
LM193 AJ	Dual	−55 to 125	25	1	0.4	36	Ceramic Minidip
LM193 J	Dual	−55 to 125	25	2	0.4	36	
LM293 AJ	Dual	−25 to 85	25	2	0.4	36	
LM293 J	Dual	−25 to 85	25	2	0.4	36	
LM311 J	Single	0 to 70	100	2	5.1	36	
LM393 AJ	Dual	0 to 70	25	2	0.4	36	
LM393 J	Dual	0 to 70	25	2	0.4	36	
LM2903 J	Dual	−40 to 85	25	2	0.4	36	
LM139 AJ	Quad	−55 to 125	25	1	0.8	36	Ceramic DIP-14
LM139 J	Quad	−55 to 125	25	2	0.8	36	
LM239 AJ	Quad	−25 to 85	25	2	0.8	36	
LM239 J	Quad	−25 to 85	25	2	0.8	36	
LM339 AJ	Quad	0 to 70	25	2	0.8	36	
LM339 J	Quad	0 tc 70	25	2	0.8	36	
LM2901 J	Quad	−40 to 85	25	2	0.8	36	
MC3302 L	Quad	−40 to 85	30	3	0.8	28	

DARLINGTON ARRAYS

Type	N°	V_{CEX}	I_o	Input	Configuration	Package
L601	8	90V	0.5A	General purpose	● ⊣▶⊢	Plastic DIP-16
L602	8	90V	0.4A	14-25V PMOS	● ⊣▶⊢	
L603	8	90V	0.4A	5V TTL/CMOS	● ⊣▶⊢	
L604	8	90V	0.4A	6-15V CMOS/PMOS	● ⊣▶⊢	
L702B	4	90V	2A	5V TTL	●	
L702N	4	90V	2A	5V TTL	●	Multiwatt 11
L7150	4	50V	1.5A	5V TTL/CMOS	● ⊣▶⊢	Multiwatt 15
L7152	4	50V	1.5A	6-15V CMOS/PMOS	● ⊣▶⊢	
L7180	4	80V	1.5A	5V TTL/CMOS	● ⊣▶⊢	
L7182	4	80V	1.5A	6-15V CMOS/PMOS	● ⊣▶⊢	
ULN2001A/D	7	50V	0.5A	General Purpose	● ⊣▶⊢	Plastic DIP-16 and SO-16
ULN2002A/D	7	50V	0.5A	14-25V PMOS	● ⊣▶⊢	
ULN2003A/D	7	50V	0.5A	5V TTL/CMOS	● ⊣▶⊢	
ULN2004A/D	7	50V	0.5A	6-15V CMOS/PMOS	● ⊣▶⊢	
ULQ2001R	7	50V	0.5A	General purpose	● ⊣▶⊢	Ceramic DIP-16
ULQ2002R	7	50V	0.5A	14-25V PMOS	● ⊣▶⊢	
ULQ2003R	7	50V	0.5A	5V TTL/CMOS	● ⊣▶⊢	
ULQ2004R	7	50V	0.5A	6-15V CMOS/PMOS	● ⊣▶⊢	

● = common emitters. ■ = isolated darlingtons.
⊣▶⊢ = integral suppression diodes. ▷ = predriver stage.

DARLINGTON ARRAYS

Type	N°	V_{CEX}	I_o	Input	Configuration	Package
ULN2064B	4	50V	1.5A	5V TTL/CMOS	● ⊣▶⊢	Plastic DIP-16
ULN2065B	4	80V	1.5A	5V TTL/CMOS	● ⊣▶⊢	
ULN2066B	4	50V	1.5A	6-15V CMOS/PMOS	● ⊣▶⊢	
ULN2067B	4	80V	1.5A	6-15V CMOS/PMOS	● ⊣▶⊢	
ULN2068B	4	50V	1.5A	5V CMOS/TTL	▷ ● ⊣▶⊢	
ULN2069B	4	80V	1.5A	5V CMOS/TTL	▷ ● ⊣▶⊢	
ULN2070B	4	50V	1.5A	6-15V CMOS/PMOS	▷ ● ⊣▶⊢	
ULN2071B	4	80V	1.5A	6-15V CMOS/PMOS	▷ ● ⊣▶⊢	
ULN2074B	4	50V	1.5A	General purpose	■	
ULN2075B	4	80V	1.5A	General purpose	■	
ULN2076B	4	50V	1.5A	6-15V CMOS/PMOS	■	
ULN2077B	4	80V	1.5A	6-15V CMOS/PMOS	■	
ULN2801A	8	50V	0.5A	General purpose	● ⊣▶⊢	Plastic DIP-18
ULN2802A	8	50V	0.5A	14-25V PMOS	● ⊣▶⊢	
ULN2803A	8	50V	0.5A	5V TTL/CMOS	● ⊣▶⊢	
ULN2804A	8	50V	0.5A	6-15V CMOS/PMOS	● ⊣▶⊢	
ULN2805A	8	50V	0.5A	High Output TTL	● ⊣▶⊢	

● = common emitters.
⊣▶⊢ = integral suppression diodes.
■ = isolated darlingtons.
▷ = predriver stage.

TIMERS

Type		Temperature Range (°C)	Max. Operat. Freq. (KHz)	Supply Current (mA)	Max Supply (V)	Package
NE555 D	Single	0 to 70	500	3	16	SO-8
NE556 D	Dual	0 to 70	500	6	16	SO-14
NE555 N **SE555 N**	Single	0 to 70	500	3	16	Minidip
		−40 to 85	500	3	16	
NE556 N **SE556 N**	Dual	0 to 70	500	6	16	DIP-14
		−40 to 85	500	6	16	
NE555 FE **SE555 FE**	Single	0 to 70	500	3	16	Ceramic Minidip
		−55 to 125	500	6	18	
NE556 F **SE556 F**	Dual	0 to 70	500	6	16	Ceramic DIP-14
		−55 to 125	500	6	18	

TRANSISTORS ARRAYS

Type	Temperature Range (°C)	V_{CBO} (V)	I_{cmax} (mA)	Input offset voltage (mV)	f_t (Mhz)	Package
LM3046 D	−40 to 85	20	50	0.45	550	SO-14
LM3046 N	−40 to 85	20	50	0.45	550	DIP-14
LM3045 J	−55 to 125	20	50	0.45	550	
LM3046 J	−40 to 85	20	50	0.45	550	

LINEAR DRIVERS

Type	Function	Package
L149	4A Linear Driver	Pentawatt
L165	Power Op. Amp.	Pentawatt
L272	Dual Power Op. Amp.	DIP-16
L272M	Dual Power Op. Amp.	Minidip
L2720	Dual Power Op. Amp.	DIP-16
L2722	Dual Power Op. Amp.	Minidip

QUAD LINE DRIVERS/RECEIVERS

Type	Function	Temperature Range (°C)	Rise Time (ns)	Delay Time (ns)	Supply Current (mA)	Max Supply (V)	Package
AM26LS31 **AM26LS32/33**	Driver Receivers	0 to 70	20 25	20 25	— —	7	DIP-16 SO-16J
MC1488 D	Driver	0 to 75	55	110/275	18	30	SO-14
MC1489 D **MC1489 AD**	Receivers	0 to 75	120 120	25 25	16 16	10	
MC1488 P	Driver	0 to 75	55	110/275	18	30	DIP-14
MC1489 AP **MC1489 P**	Receivers	0 to 75	120 120	25 25	16 16	10	
MC1488 L	Driver	0 to 75	55	110/275	18	30	Ceramic DIP-14
MC1489 AL **MC1489 L**	Receivers	0 to 75	120 120	25 25	16 16	10	

DATA CONVERSION

Type	Accuracy	Temperature range (°C)	Package
DAC0808 LCN **DAC0808 LCJ** **DAC0808 D1**	8 bit	0 to 75	DIP-16 Ceramic DIP-16 SO-16
DAC0808 LJ		−55 to 125	Ceramic DIP-16
DAC0807 LCN **DAC0807 LCJ** **DAC0807 D1**	7 bit	0 to 75	DIP-16 Ceramic DIP-16 SO-16
DAC0806 LCN **DAC0806 LCJ** **DAC0806 D1**	6 bit	0 to 75	DIP-16 Ceramic DIP-16 SO-16
AM6012 DC **AM6012 ADC**	12 bit	0 to 70	DIP-20
AM6012 D **AM6012 AD**	12 bit	0 to 70	SO-20L

CROSS REFERENCE

CROSS REFERENCE

INDUSTRY TYPE	SOURCE	SGS TYPE
AM26LS31CD	TEXAS	AM26LS31D1
AM26LS31CJ	TEXAS	AM26LS31CJ
AM26LS31CN	TEXAS	AM26LS31CN
AM26LS31DC	AMD	AM26LS31CJ
AM26LS31DM	AMD	AM26LS31MJ
AM26LS31L	MOTOROLA	AM26LS31CJ
AM26LS31P	MOTOROLA	AM26LS31CN
AM26LS31PC	AMD	AM26LS31CN
AM26LS32ACD	TEXAS	AM26LS32D1
AM26LS32ACJ	TEXAS	AM26LS32CJ
AM26LS32ACN	TEXAS	AM26LS32CN
AM26LS32DC	AMD	AM26LS32CJ
AM26LS32DM	AMD	AM26LS32MJ
AM26LS32L	MOTOROLA	AM26LS32CJ
AM26LS32P	MOTOROLA	AM26LS32CN
AM26LS32PC	AMD	AM26LS32CN
AM26LS33DC	AMD	AM26LS33CT
AM26LS33DM	AMD	AM26LS33MJ
AM26LS33L	MOTOROLA	AM26LS32CJ
AM26LS33P	MOTOROLA	AM26LS32CN
AM26LS33PC	AMD	AM26LS33CN
AM6012APC	AMD	AM6012APC
AM6012PC	AMD	AM6012PC
CA082AE	RCA	TL082ACP
CA082BE	RCA	TL082BCP
CA082E	RCA	TL082CP
CA084AE	RCA	TL084ACN
CA084BE	RCA	TL084BCN
CA084E	RCA	TL084CN
CA139AF	RCA	LM139AJ
CA139F	RCA	LM139J
CA1458E	RCA	MC1458P1
CA224E	RCA	LM224N
CA239AF	RCA	LM239AJ
CA239E	RCA	LM239N
CA258E	RCA	LM258N
CA2901E	RCA	LM2901N
CA2901F	RCA	LM2901J
CA2902E	RCA	LM2902N
CA2904E	RCA	LM2904N
CA301AE	RCA	LM301AN
CA301AT	RCA	LM301AH
CA3045F	RCA	LM3045J
CA3046E	RCA	LM3046N
CA324E	RCA	LM324N
CA339AE	RCA	LM339AN
CA339AF	RCA	LM339AJ
CA339E	RCA	LM339N
CA339F	RCA	LM339J
CA358AE	RCA	LM358AN
CA358E	RCA	LM358N
CA555E	RCA	NE555N

INDUSTRY TYPE	SOURCE	SGS TYPE
CA723CE	RCA	LM723CN
CA723E	RCA	LM723N
CA741CE	RCA	LM741CN
CA741E	RCA	LM741EN
CA748CE	RCA	LM748CN
DAC0806LCJ	NATIONAL	DAC0806LCJ
DAC0806LCN	NATIONAL	DAC0806LCN
DAC0807LCJ	NATIONAL	DAC0807LCJ
DAC0807LCN	NATIONAL	DAC0807LCN
DAC0808LCJ	NATIONAL	DAC0808LCJ
DAC0808LCN	NATIONAL	DAC0808LCN
DAC0808LJ	NATIONAL	DAC0808LJ
DS1488J	NATIONAL	MC1488L
DS1488N	NATIONAL	MC1488P
DS1489AJ	NATIONAL	MC1489AL
DS1489AN	NATIONAL	MC1489AP
DS1489J	NATIONAL	MC1489L
DS1489N	NATIONAL	MC1489P
DS26LS31CJ	NATIONAL	AM26LS31CJ
DS26LS31CN	NATIONAL	AM26LS31CN
DS26LS31MJ	NATIONAL	AM26LS31MJ
DS26LS32CJ	NATIONAL	AM26LS32CJ
DS26LS32CN	NATIONAL	AM26LS32CN
DS26LS32MJ	NATIONAL	AM26LS32MJ
DS26LS33CJ	NATIONAL	AM26LS33CJ
DS26LS33CN	NATIONAL	AM26LS33CN
DS26LS33MJ	NATIONAL	AM26LS33MJ
ITT552	ITT	ULN2001A
ITT554	ITT	ULN2002A
ITT556	ITT	ULN2003A
L702DP	THOMSON	L702B
L702SP	THOMSON	L702N
LM101AH	NATIONAL	LM101AH
LM101AHM	FAIRCHILD	LM101AH
LM101AJ	NATIONAL	LM101AJ
LM101AJG	TEXAS	LM101AJ
LM117K	NATIONAL	LM117K
LM124AJ	NATIONAL	LM124AJ
LM124DG	THOMSON	LM124J
LM124F	PHIL.SIGN.	LM124J
LM124J	NATIONAL	LM124J
LM139ADG	THOMSON	LM139AJ
LM139AJ	NATIONAL	LM139AJ
LM139DG	THOMSON	LM139J
LM139F	PHIL.SIGN.	LM139J
LM139J	NATIONAL	LM139J
LM1458DG	THOMSON	MC1458U
LM1458DP	THOMSON	MC1458P1
LM1458FP	THOMSON	MC1458D
LM1458J	NATIONAL	MC1458U
LM1458M	NATIONAL	MC1458D
LM1458N	NATIONAL	MC1458P1

CROSS REFERENCE

INDUSTRY TYPE	SOURCE	SGS TYPE
LM1558DG	THOMSON	MC1558U
LM1558J	NATIONAL	MC1558U
LM158AJ	NATIONAL	LM158AJ
LM158DG	THOMSON	LM158J
LM158FE	PHIL.SIGN.	LM158J
LM158J	NATIONAL	LM158J
LM158JG	TEXAS	LM158J
LM193AJ	NATIONAL	LM193AJ
LM193DG	THOMSON	LM193J
LM193FE	PHIL.SIGN.	LM193J
LM193J	NATIONAL	LM193J
LM193JG	TEXAS	LM193J
LM201AD	TEXAS	LM201AD
LM201AH	NATIONAL	LM201AH
LM201AHM	FAIRCHILD	LM201AH
LM201AJ	NATIONAL	LM201AJ
LM201AJG	TEXAS	LM201AJ
LM201AN	NATIONAL	LM201AN
LM201AP	TEXAS	LM201AN
LM217K	NATIONAL	LM217K
LM224AJ	NATIONAL	LM224AJ
LM224D	MOTOROLA	LM224D
LM224DG	THOMSON	LM224J
LM224DP	THOMSON	LM224N
LM224F	PHIL.SIGN.	LM224J
LM224J	NATIONAL	LM224J
LM224N	NATIONAL	LM224N
LM239AJ	NATIONAL	LM239AJ
LM239D	TEXAS	LM239D
LM239DP	THOMSON	LM239N
LM239F	PHIL.SIGN.	LM239J
LM239FP	THOMSON	LM239D
LM239J	NATIONAL	LM239J
LM239N	NATIONAL	LM239N
LM258AJ	NATIONAL	LM258AJ
LM258D	MOTOROLA	LM258D
LM258DP	THOMSON	LM258N
LM258FE	PHIL.SIGN.	LM258J
LM258J	NATIONAL	LM258J
LM258JG	TEXAS	LM258J
LM258N	NATIONAL	LM258N
LM258P	TEXAS	LM258N
LM2901D	MOTOROLA	LM2901D
LM2901DP	THOMSON	LM2901N
LM2901F	PHIL.SIGN.	LM2901J
LM2901FP	THOMSON	LM2901D
LM2901J	NATIONAL	LM2901J
LM2901N	NATIONAL	LM2901N
LM2902D	MOTOROLA	LM2902D
LM2902DP	THOMSON	LM2902N
LM2902FP	THOMSON	LM2902D
LM2902J	NATIONAL	LM2902J

INDUSTRY TYPE	SOURCE	SGS TYPE
LM2902N	NATIONAL	LM2902N
LM2903D	TEXAS	LM2903D
LM2903DP	THOMSON	LM2903N
LM2903FP	THOMSON	LM2903D
LM2903J	NATIONAL	LM2903J
LM2903JG	TEXAS	LM2903J
LM2903N	NATIONAL	LM2903N
LM2903P	TEXAS	LM2903N
LM2904D	MOTOROLA	LM2904D
LM2904DP	THOMSON	LM2904N
LM2904FP	THOMSON	LM2904D
LM2904J	NATIONAL	LM2904J
LM2904JG	TEXAS	LM2904J
LM2904N	NATIONAL	LM2904N
LM2904P	TEXAS	LM2904N
LM293AFE	PHIL.SIGN.	LM293AJ
LM293AJ	NATIONAL	LM293AJ
LM293D	TEXAS	LM293D
LM293FE	PHIL.SIGN.	LM293J
LM293JG	TEXAS	LM293J
LM293N	NATIONAL	LM293N
LM293P	TEXAS	LM293N
LM301AD	PHIL.SIGN.	LM301AD
LM301ADP	THOMSON	LM301AN
LM301AFE	PHIL.SIGN.	LM301AJ
LM301AFP	THOMSON	LM301AD
LM301AH	NATIONAL	LM301AH
LM301AJ	NATIONAL	LM301AJ
LM301AJG	TEXAS	LM301AJ
LM301AN	NATIONAL	LM301AN
LM301AP	TEXAS	LM301AN
LM301HC	FAIRCHILD	LM301AH
LM3045J	NATIONAL	LM3045J
LM3046N	NATIONAL	LM3046N
LM311D	MOTOROLA	LM311D
LM311DP	THOMSON	LM311N
LM311FP	THOMSON	LM311D
LM311J-8	NATIONAL	LM311J
LM311JG	TEXAS	LM311J
LM311M	NATIONAL	LM311D
LM311N	NATIONAL	LM311N
LM311P	TEXAS	LM311N
LM317K	NATIONAL	LM317K
LM317SP	THOMSON	LM317T
LM317T	NATIONAL	LM317T
LM324AJ	NATIONAL	LM324AJ
LM324AN	NATIONAL	LM324AN
LM324D	PHIL.SIGN.	LM324D
LM324DP	THOMSON	LM324N
LM324F	PHIL.SIGN.	LM324J
LM324FP	THOMSON	LM324D
LM324J	NATIONAL	LM324J

CROSS REFERENCE

INDUSTRY TYPE	SOURCE	SGS TYPE
LM324M	NATIONAL	LM324D
LM324N	NATIONAL	LM324N
LM3302DP	THOMSON	MC3302P
LM3302F	RCA	MC3302L
LM3302J	NATIONAL	MC3302L
LM3302N	NATIONAL	MC3302P
LM339ADP	THOMSON	LM339AN
LM339AJ	NATIONAL	LM339AJ
LM339AN	NATIONAL	LM339AN
LM339D	PHIL.SIGN.	LM339D
LM339DP	THOMSON	LM339N
LM339F	PHIL.SIGN.	LM339J
LM339FP	THOMSON	LM339D
LM339J	NATIONAL	LM339J
LM339M	NATIONAL	LM339D
LM339N	NATIONAL	LM339N
LM358AJ	NATIONAL	LM358AJ
LM358AJG	TEXAS	LM358AJ
LM358AN	NATIONAL	LM358AN
LM358AP	TEXAS	LM358AN
LM358D	PHIL.SIGN.	LM358D
LM358DP	THOMSON	LM358N
LM358FE	PHIL.SIGN.	LM358J
LM358FP	THOMSON	LM358D
LM358J	NATIONAL	LM358J
LM358JG	TEXAS	LM358J
LM358M	NATIONAL	LM358D
LM358N	NATIONAL	LM358N
LM358P	TEXAS	LM358N
LM393ADP	THOMSON	LM393AN
LM393AFE	PHIL.SIGN.	LM393AJ
LM393AJ	NATIONAL	LM393AJ
LM393AJG	TEXAS	LM393AJ
LM393AN	NATIONAL	LM393AN
LM393AP	TEXAS	LM393AN
LM393D	MOTOROLA	LM393D
LM393DP	THOMSON	LM393N
LM393FE	PHIL.SIGN.	LM393J
LM393FP	THOMSON	LM393D
LM393J	NATIONAL	LM393J
LM393JG	TEXAS	LM393J
LM393M	NATIONAL	LM393D
LM393N	NATIONAL	LM393N
LM393P	TEXAS	LM393N
LM555J	NATIONAL	NE555FE
LM555M	NATIONAL	NE555D
LM556J	NATIONAL	NE556F
LM556M	NATIONAL	NE556D
LM709CH	NATIONAL	LS709CTB
LM709CN	NATIONAL	LS709CB
LM709H	NATIONAL	LS709TB
LM723CFP	THOMSON	LM723CD

INDUSTRY TYPE	SOURCE	SGS TYPE
LM723CH	NATIONAL	LM723CH
LM723CJ	NATIONAL	LM723CJ
LM723CM	NATIONAL	LM723CD
LM723CN	NATIONAL	LM723CN
LM723H	NATIONAL	LM723H
LM723J	NATIONAL	LM723J
LM741AH	NATIONAL	LM741AH
LM741CH	NATIONAL	LM741CH
LM741CJ	NATIONAL	LM741CJ
LM741CM	NATIONAL	LM741CD
LM741CN	NATIONAL	LM741CN
LM741EJ	NATIONAL	LM741EJ
LM741EN	NATIONAL	LM741EN
LM741H	NATIONAL	LM741H
LM741J	NATIONAL	LM741J
LM748CJ	NATIONAL	LM748CJ
LM748CN	NATIONAL	LM748CN
LM748J	NATIONAL	LM748J
LM7805CK	NATIONAL	L7805CT
LM7805CT	NATIONAL	L7805CV
LM7812CK	NATIONAL	L7812CT
LM7812CT	NATIONAL	L7812CV
LM7815CK	NATIONAL	L7815CT
LM7815CT	NATIONAL	L7815CV
LM7905CK	NATIONAL	L7905CT
LM7905CT	NATIONAL	L7905CV
LM7912CK	NATIONAL	L7912CT
LM7912CT	NATIONAL	L7912CV
LM7915CK	NATIONAL	L7915CT
LM7915CT	NATIONAL	L7915CV
MC1408L6	MOTOROLA	DAC0806LCJ
MC1408L7	MOTOROLA	DAC0807LCJ
MC1408L8	MOTOROLA	DAC0808LCJ
MC1408P6	MOTOROLA	DAC0806LCN
MC1408P7	MOTOROLA	DAC0807LCN
MC1408P8	MOTOROLA	DAC0808LCN
MC1455D	MOTOROLA	NE555D
MC1455P1	MOTOROLA	NE555N
MC1455U	MOTOROLA	NE555FE
MC1458CD	MOTOROLA	MC1458CD
MC1458CP1	MOTOROLA	MC1458CP1
MC1458CU	MOTOROLA	MC1458CU
MC1458D	MOTOROLA	MC1458D
MC1458FE	PHIL.SIGN.	MC1458U
MC1458N	PHIL.SIGN.	MC1458P1
MC1458P1	MOTOROLA	MC1458P1
MC1458U	MOTOROLA	MC1458U
MC1488F	PHIL.SIGN.	MC1488L
MC1488L	MOTOROLA	MC1488L
MC1488N	PHIL.SIGN.	MC1488P
MC1488P	MOTOROLA	MC1488P
MC1489AF	PHIL.SIGN.	MC1489AL

CROSS REFERENCE

INDUSTRY TYPE	SOURCE	SGS TYPE
MC1489AL	MOTOROLA	MC1489AL
MC1489AN	PHIL.SIGN.	MC1489AP
MC1489AP	MOTOROLA	MC1489AP
MC1489F	PHIL.SIGN.	MC1489L
MC1489L	MOTOROLA	MC1489L
MC1489N	PHIL.SIGN.	MC1489P
MC1489P	MOTOROLA	MC1489P
MC1508L8	MOTOROLA	DAC0808LJ
MC1555U	MOTOROLA	SE555FE
MC1558FE	PHIL.SIGN.	MC1558U
MC1558JG	TEXAS	MC1558U
MC1558U	MOTOROLA	MC1558U
MC1709AG	MOTOROLA	LS709ATB
MC1709CG	MOTOROLA	LS709CTB
MC1709CP1	MOTOROLA	LS709CB
MC1709G	MOTOROLA	LS709TB
MC1723CD	MOTOROLA	LM723CD
MC1723CG	MOTOROLA	LM723CH
MC1723CL	MOTOROLA	LM723CJ
MC1723CP	MOTOROLA	LM723CN
MC1723G	MOTOROLA	LM723H
MC1723L	MOTOROLA	LM723J
MC1741CD	MOTOROLA	LM741CD
MC1741CG	MOTOROLA	LM741CH
MC1741CP1	MOTOROLA	LM741CN
MC1741CU	MOTOROLA	LM741CJ
MC1741G	MOTOROLA	LM741H
MC1741U	MOTOROLA	LM741J
MC1748CP1	MOTOROLA	LM748CN
MC1748CU	MOTOROLA	LM748CJ
MC1748U	MOTOROLA	LM748CJ
MC1776CD	MOTOROLA	MC1776CD
MC1776CG	MOTOROLA	MC1776CG
MC1776CP1	MOTOROLA	MC1776CP1
MC1776CU	MOTOROLA	MC1776CU
MC1776G	MOTOROLA	MC1776G
MC1776U	MOTOROLA	MC1776U
MC3302D	MOTOROLA	MC3302D
MC3302F	PHIL.SIGN.	MC3302L
MC3302L	MOTOROLA	MC3302L
MC3302N	PHIL.SIGN.	MC3302P
MC3302P	MOTOROLA	MC3302P
MC3303F	PHIL.SIGN.	MC3303L
MC3303J	TEXAS	MC3303L
MC3303L	MOTOROLA	MC3303L
MC3303N	TEXAS	MC3303P
MC3303P	MOTOROLA	MC3303P
MC3403D	MOTOROLA	MC3403D
MC3403DP	THOMSON	MC3403P
MC3403F	PHIL.SIGN.	MC3403L
MC3403FP	THOMSON	MC3403D
MC3403J	TEXAS	MC3403L

INDUSTRY TYPE	SOURCE	SGS TYPE
MC3403L	MOTOROLA	MC3403L
MC3403N	TEXAS	MC3403P
MC3403P	MOTOROLA	MC3403P
MC3456L	MOTOROLA	NE556F
MC3456P	MOTOROLA	NE556N
MC3503DG	THOMSON	MC3503L
MC3503F	PHIL.SIGN.	MC3503L
MC3503J	TEXAS	MC3503L
MC3503L	MOTOROLA	MC3503L
MC3556L	MOTOROLA	SE556F
MC7805ACT	MOTOROLA	L7805ACV
MC7805CK	MOTOROLA	L7805CT
MC7805CT	MOTOROLA	L7805CV
MC7805K	MOTOROLA	L7805T
MC7806ACT	MOTOROLA	L7806ACV
MC7806CK	MOTOROLA	L7806CT
MC7806CT	MOTOROLA	L7806CV
MC7806K	MOTOROLA	L7806T
MC7808ACT	MOTOROLA	L7808ACV
MC7808CK	MOTOROLA	L7808CT
MC7808CT	MOTOROLA	L7808CV
MC7808K	MOTOROLA	L7808T
MC7812ACT	MOTOROLA	L7812ACV
MC7812CK	MOTOROLA	L7812CT
MC7812CT	MOTOROLA	L7812CV
MC7812K	MOTOROLA	L7812T
MC7815ACT	MOTOROLA	L7815ACV
MC7815CK	MOTOROLA	L7815CT
MC7815CT	MOTOROLA	L7815CV
MC7815K	MOTOROLA	L7815T
MC7818ACT	MOTOROLA	L7818ACV
MC7818CK	MOTOROLA	L7818CT
MC7818CT	MOTOROLA	L7818CV
MC7818K	MOTOROLA	L7818T
MC7824ACT	MOTOROLA	L7824ACV
MC7824CT	MOTOROLA	L7824CV
MC7824K	MOTOROLA	L7824T
MC78M05CT	MOTOROLA	L78M05CV
MC78M06CT	MOTOROLA	L78M06CV
MC78M08CT	MOTOROLA	L78M08CV
MC78M12CT	MOTOROLA	L78M12CV
MC78M15CT	MOTOROLA	L78M15CV
MC78M18CT	MOTOROLA	L78M18CV
MC78M24CT	MOTORLA	L78M24CV
MC7905CK	MOTOROLA	L7905CT
MC7905CT	MOTOROLA	L7905CV
MC7908CK	MOTOROLA	L7908CT
MC7908CT	MOTOROLA	L7908CV
MC7912CK	MOTOROLA	L7912CT
MC7912CT	MOTOROLA	L7912CV
MC7915CK	MOTOROLA	L7915CT
MC7915CT	MOTOROLA	L7915CV

CROSS REFERENCE

INDUSTRY TYPE	SOURCE	SGS TYPE
MC7918CK	MOTOROLA	L7918CT
MC7918CT	MOTOROLA	L7918CV
MC7924CK	MOTOROLA	L7924CT
MC7924CT	MOTOROLA	L7924CV
MC7952CK	MOTOROLA	L7952CT
MC7952CT	MOTOROLA	L7952CV
NE532D	PHIL.SIGN.	NE532D
NE532FE	PHIL.SIGN.	NE532FE
NE532N	PHIL.SIGN.	NE532N
NE555CFP	THOMSON	NE555D
NE555D	PHIL.SIGN.	NE555D
NE555FE	PHIL.SIGN.	NE555FE
NE555JG	TEXAS	NE555FE
NE555N	PHIL.SIGN.	NE555N
NE555P	TEXAS	NE555N
NE556CFP	THOMSON	NE556D
NE556D	PHIL.SIGN.	NE556D
NE556DP	THOMSON	NE556N
NE556F	PHIL.SIGN.	NE556F
NE556JG	TEXAS	NE556F
NE556N	PHIL.SIGN.	NE556N
NE556P	TEXAS	NE556N
NE5601N	PHIL.SIGN.	ULN2001A
NE5602N	PHIL.SIGN.	ULN2002A
NE5603N	PHIL.SIGN.	ULN2003A
NE5604N	PHIL.SIGN.	ULN2004A
PWM125AK	SILICONIX	SG1525AJ
PWM125BK	SILICONIX	SG2525AJ
PWM125CK	SILICONIX	SG3525AJ
RC1458DN	RAYTHEON	MC1458P1
RC1458T	RAYTHEON	MC1458U
RC1488DC	RAYTHEON	MC1488L
RC1489ADC	RAYTHEON	MC1489AL
RC1489DC	RAYTHEON	MC1489L
RC1558T	RAYTHEON	MC1558U
RC3302DU	RAYTHEON	MC3302F
RC709DN	RAYTHEON	LS709CB
RC709T	RAYTHEON	LS709CTB
RC723D	RAYTHEON	LM723CJ
RC723T	RAYTHEON	LM723CH
RC741DN	RAYTHEON	LM741CM
RC741T	RAYTHEON	LM741CH
RM709T	RAYTHEON	LS709TB
RM723D	RAYTHEON	LM723J
RM723T	RAYTHEON	LM723H
RM741D	RAYTHEON	LM741J
RM741T	RAYTHEON	LM741H
RM748T	RAYTHEON	LM748H
SA1458N	PHIL.SIGN.	MC1458CP1
SE555FE	PHIL.SIGN.	SE555FE
SE555JG	TEXAS	SE555FE
SE556DG	THOMSON	SE556F

INDUSTRY TYPE	SOURCE	SGS TYPE
SE556F	PHIL.SIGN.	SE556F
SE556J	TEXAS	SE556F
SG1524J	SIL.GEN.	SG1524J
SG1525AJ	SIL.GEN.	SG1525AJ
SG1527AJ	SIL.GEN.	SG1527AJ
SG2001J	SIL.GEN.	ULQ2001R
SG2001N	SIL.GEN.	ULN2001A
SG2002J	SIL.GEN.	ULQ2002R
SG2002N	SIL.GEN.	ULN2002A
SG2003J	SIL.GEN.	ULQ2003R
SG2003N	SIL.GEN.	ULN2003A
SG2004J	SIL.GEN.	ULQ2004R
SG2004N	SIL.GEN.	ULN2004A
SG2524J	SIL.GEN.	SG2524J
SG2524N	SIL.GEN.	SG2524J
SG2525AJ	SIL.GEN.	SG2525AJ
SG2525AN	SIL.GEN.	SG2525AN
SG2527AJ	SIL.GEN.	SG2527AJ
SG2527AN	SIL.GEN.	SG2527AN
SG3524D	PHIL.SIGN.	SG3524D
SG3524J	SIL.GEN.	SG3524J
SG3524N	SIL.GEN.	SG3524N
SG3525AJ	SIL.GEN.	SG3525AJ
SG3525AN	SIL.GEN.	SG3525AN
SG3527AJ	SIL.GEN.	SG3527AJ
SG3527AN	SIL.GEN.	SG3527AN
SN75064NE	TEXAS	ULN2064B
SN75065NE	TEXAS	ULN2065B
SN75066NE	TEXAS	ULN2066B
SN75067NE	TEXAS	ULN2067B
SN75068NE	TEXAS	ULN2068B
SN75069NE	TEXAS	ULN2069B
SN75074NE	TEXAS	ULN2074B
SN75075NE	TEXAS	ULN2075B
SN75188J	TEXAS	MC1488L
SN75188N	TEXAS	MC1488P
SN75189AN	TEXAS	MC1489AP
SN75189AT	TEXAS	MC1489AL
SN75189J	TEXAS	MC1489L
SN75189N	TEXAS	MC1489P
TDA0200SP	THOMSON	L200CV
TL072ACJG	TEXAS	TL072ACJG
TL072ACP	TEXAS	TL072ACP
TL072BCJG	TEXAS	TL072BCJG
TL072BCP	TEXAS	TL072BCP
TL072CDP	THOMSON	TL072CP
TL072CFP	THOMSON	TL072CD
TL072CJG	TEXAS	TL072CJG
TL072CP	TEXAS	TL072CP
TL072IGJ	TEXAS	TL072IGJ
TL072IP	TEXAS	TL072IP
TL074ACJ	TEXAS	TL074ACJ

CROSS REFERENCE

INDUSTRY TYPE	SOURCE	SGS TYPE
TL074ACN	TEXAS	TL074ACN
TL074BCJ	TEXAS	TL074BCJ
TL074BCN	TEXAS	TL074BCN
TL074CDP	THOMSON	TL074CN
TL074CFP	THOMSON	TL074CD
TL074CJ	TEXAS	TL074CJ
TL074CN	TEXAS	TL074CN
TL074IJ	TEXAS	TL074IJ
TL074IN	TEXAS	TL074IN
TL082ACJG	TEXAS	TL082ACJG
TL082ACP	TEXAS	TL082ACP
TL082BCJG	TEXAS	TL082BCJG
TL082BCP	TEXAS	TL082BCP
TL082CD	TEXAS	TL082CD
TL082CDP	THOMSON	TL082CP
TL082CFP	THOMSON	TL082CD
TL082CJG	TEXAS	TL082CJG
TL082CP	TEXAS	TL082CP
TL082IJG	TEXAS	TL082IJG
TL082IP	TEXAS	TL082IP
TL082MJG	TEXAS	TL082MJG
TL084ACDP	THOMSON	TL084ACN
TL084ACJ	TEXAS	TL084ACJ
TL084ACN	TEXAS	TL084ACN
TL084BCJ	TEXAS	TL084BCJ
TL084BCN	TEXAS	TL084BCN
TL084CD	TEXAS	TL084CD
TL084CDP	THOMSON	TL084CN
TL084CFP	THOMSON	TL084CD
TL084CJ	TEXAS	TL084CJ
TL084CN	TEXAS	TL084CN
TL084IJ	TEXAS	TL084IJ
TL084IN	TEXAS	TL084IN
TL084MDG	THOMSON	TL084MJ
TL084MJ	TEXAS	TL084MJ
TL7702ACP	TEXAS	TL7702ACP
TL7705ACP	TEXAS	TL7705ACP
TL7709ACP	TEXAS	TL7709ACP
TL7712ACP	TEXAS	TL7712ACP
TL7715ACP	TEXAS	TL7715ACP
UC1524AJ	UNITRODE	UC1524AJ
UC1524AN	UNITRODE	UC1524AN
UC1840J	UNITRODE	UC1840J
UC1840N	UNITRODE	UC1840N
UC1842J	UNITRODE	UC1842J
UC1842N	UNITRODE	UC1842N
UC1846J	UNITRODE	UC1846J
UC1846N	UNITRODE	UC1846N
UC1847J	UNITRODE	UC1847J
UC1847N	UNITRODE	UC1847N
UC2524AJ	UNITRODE	UC2524AJ
UC2524AN	UNITRODE	UC2524AM

INDUSTRY TYPE	SOURCE	SGS TYPE
UC2840J	UNITRODE	UC2840J
UC2840N	UNITRODE	UC2840N
UC2842J	UNITRODE	UC2842J
UC2842N	UNITRODE	UC2842N
UC2846J	UNITRODE	UC2846J
UC2846N	UNITRODE	UC2846N
UC2847J	UNITRODE	UC2847J
UC2847N	UNITRODE	UC2847J
UC2847N	UNITRODE	UC2847N
UC2906J	UNITRODE	UC2906J
UC2906N	UNITRODE	UC2906N
UC3524AJ	UNITRODE	UC3524AJ
UC3524AN	UNITRODE	UC3524AN
UC3840J	UNITRODE	UC3840J
UC3840N	UNITRODE	UC3840N
UC3842J	UNITRODE	UC3842J
UC3842N	UNITRODE	UC3842N
UC3846J	UNITRODE	UC3846J
UC3846N	UNITRODE	UC3846N
UC3847J	UNITRODE	UC3847J
UC3847N	UNITRODE	UC3847N
UC3906J	UNITRODE	UC3906J
UC3906N	UNITRODE	UC3906N
ULN2001A	SPRAGUE	ULN2001A
ULN2001AJ	TEXAS	ULQ2001R
ULN2001AN	TEXAS	ULN2001A
ULN2001F	PHIL.SIGN.	ULQ2001R
ULN2001N	PHIL.SIGN.	ULN2001A
ULN2002A	SPRAGUE	ULN2002A
ULN2002AJ	TEXAS	ULQ2002R
ULN2002AN	TEXAS	ULN2002A
ULN2002F	PHIL.SIGN.	ULQ2002R
ULN2002N	PHIL.SIGN.	ULN2002A
ULN2003A	SPRAGUE	ULN2003A
ULN2003AJ	TEXAS	ULQ2003R
ULN2003AN	TEXAS	ULN2003A
ULN2003F	PHIL.SIGN.	ULQ2003R
ULN2003N	PHIL.SIGN.	ULN2003A
ULN2004A	SPRAGUE	ULN2004A
ULN2004AJ	TEXAS	ULQ2004R
ULN2004AN	TEXAS	ULN2004A
ULN2004F	PHIL.SIGN.	ULQ2004R
ULN2004N	PHIL.SIGN.	ULN2004A
ULN2064B	SPRAGUE	ULN2064B
ULN2064NE	TEXAS	ULN2064B
ULN2065B	SPRAGUE	ULN2065B
ULN2065NE	TEXAS	ULN2065B
ULN2066B	SPRAGUE	ULN2066B
ULN2066NE	TEXAS	ULN2066B
ULN2067B	SPRAGUE	ULN2067B
ULN2067NE	TEXAS	ULN2067B
ULN2068B	SPRAGUE	ULN2068B

CROSS REFERENCE

INDUSTRY TYPE	SOURCE	SGS TYPE
ULN2068NE	TEXAS	ULN2068B
ULN2069B	SPRAGUE	ULN2069B
ULN2069NE	TEXAS	ULN2069B
ULN2070B	SPRAGUE	ULN2070B
ULN2071B	SPRAGUE	ULN2071B
ULN2074B	SPRAGUE	ULN2074B
ULN2074NE	TEXAS	ULN2074B
ULN2075B	SPRAGUE	ULN2075B
ULN2075NE	TEXAS	ULN2075B
ULN2076B	SPRAGUE	ULN2076B
ULN2077B	SPRAGUE	ULN2077B
ULN2801A	SPRAGUE	ULN2801A
ULN2802A	SPRAGUE	ULN2802A
ULN2803A	SPRAGUE	ULN2803A
ULN2803N	TEXAS	ULN2803A
ULN2804A	SPRAGUE	ULN2804A
ULN2804N	TEXAS	ULN2804A
ULN2805A	SPRAGUE	ULN2805A
u78S05CK	THOMSON	L78S05CT
u78S05CSP	THOMSON	L78S05CV
u78S09CK	THOMSON	L78S09CT
u78S09CSP	THOMSON	L78S09CV
u78S12CK	THOMSON	L78S12CT
u78S12CSP	THOMSON	L78S12CV
u78S15CK	THOMSON	L78S15CT
u78S15CSP	THOMSON	L78S15CV
uA117KM	FAIRCHILD	LM117K
uA124DM	FAIRCHILD	LM124J
uA139ADM	FAIRCHILD	LM139AJ
uA139DM	FAIRCHILD	LM139J
uA1458CRC	FAIRCHILD	MC1458CU
uA1458CTC	FAIRCHILD	MC1458CP1
uA1458RC	FAIRCHILD	MC1458U
uA1458TC	FAIRCHILD	MC1458P1
uA1488DC	FAIRCHILD	MC1488L
uA1488PC	FAIRCHILD	MC1488P
uA1489ADC	FAIRCHILD	MC1489AL
uA1489APC	FAIRCHILD	MC1489AP
uA1489DC	FAIRCHILD	MC1489L
uA1489PC	FAIRCHILD	MC1489P
uA1558RM	FAIRCHILD	MC1558U
uA193ARM	FAIRCHILD	LM193AJ
uA193RM	FAIRCHILD	LM193J
uA224DV	FAIRCHILD	LM224J
uA224PV	FAIRCHILD	LM224N
uA239ADC	FAIRCHILD	LM239AJ
uA239DC	FAIRCHILD	LM239J
uA239PC	FAIRCHILD	LM239N
uA2901DC	FAIRCHILD	LM2901J
uA2901PC	FAIRCHILD	LM2901N
uA2902PV	FAIRCHILD	LM2902N
uA2903RC	FAIRCHILD	LM2903J

INDUSTRY TYPE	SOURCE	SGS TYPE
uA2903TC	FAIRCHILD	LM2903N
uA293ARC	FAIRCHILD	LM293AJ
uA293RC	FAIRCHILD	LM293J
uA293TC	FAIRCHILD	LM293N
uA301ATC	FAIRCHILD	LM301AN
uA317KM	FAIRCHILD	LM317K
uA324DC	FAIRCHILD	LM324J
uA324PC	FAIRCHILD	LM324N
uA3302DC	FAIRCHILD	MC3302L
uA3302PC	FAIRCHILD	MC3302P
uA3303PC	FAIRCHILD	MC3303P
uA339ADC	FAIRCHILD	LM339AJ
uA339APC	FAIRCHILD	LM339AN
uA339DC	FAIRCHILD	LM339J
uA339PC	FAIRCHILD	LM339N
uA3403DC	FAIRCHILD	MC3403L
uA3403PC	FAIRCHILD	MC3403P
uA393ARC	FAIRCHILD	LM393AJ
uA393ATC	FAIRCHILD	LM393AN
uA393RC	FAIRCHILD	LM393J
uA393TC	FAIRCHILD	LM393N
uA555TC	FAIRCHILD	NE555N
uA556PC	FAIRCHILD	NE556N
uA709AHM	FAIRCHILD	LS709ATB
uA709CP	TEXAS	LS709CB
uA709HC	FAIRCHILD	LS709CTB
uA709HM	FAIRCHILD	LS709TB
uA709PC	FAIRCHILD	LS709CB
uA723CDP	THOMSON	LM723CN
uA723CF	PHIL.SIGN.	LM723CJ
uA723CFP	THOMSON	LM723CD
uA723CH	THOMSON	LM723CH
uA723CJ	TEXAS	LM723CJ
uA723CN	PHIL.SIGN.	LM723CN
uA723DC	FAIRCHILD	LM723CJ
uA723DM	FAIRCHILD	LM723J
uA723F	PHIL.SIGN.	LM723J
uA723MDG	THOMSON	LM723J
uA723MH	THOMSON	LM723H
uA723MJN	TEXAS	LM723J
uA723PC	FAIRCHILD	LM723CN
uA741CD	PHIL.SIGN.	LM741CD
uA741CDG	THOMSON	LM741CJ
uA741CDP8	THOMSON	LM741CN
uA741CFE	PHIL.SIGN.	LM741CJ
uA741CFP	THOMSON	LM741CD
uA741CH	THOMSON	LM741CH
uA741CJG	TEXAS	LM741CJ
uA741CN	PHIL.SIGN.	LM741CN
uA741CP	TEXAS	LM741CN
uA741FE	PHIL.SIGN.	LM741J
uA741MH	THOMSON	LM741H

CROSS REFERENCE

INDUSTRY TYPE	SOURCE	SGS TYPE
uA741MJG	TEXAS	LM741J
uA741RC	FAIRCHILD	LM741CJ
uA741TC	FAIRCHILD	LM741CN
uA748CD	TEXAS	LM748D
uA748CDG	THOMSON	LM748CJ
uA748CDP	THOMSON	LM748CN
uA748CFE	PHIL.SIGN.	LM748CJ
uA748CH	THOMSON	LM748CH
uA748CJG	TEXAS	LM741CJ
uA748CN	PHIL.SIGN.	LM748CN
uA748CP	TEXAS	LM748CN
uA748FE	PHIL.SIGN.	LM748J
uA748MH	THOMSON	LM748H
uA748MJG	TEXAS	LM748J
uA748TC	FAIRCHILD	LM748CN
uA776CDP	THOMSON	MC1776CP1
uA776CFP	THOMSON	MC1776CD
uA776CH	THOMSON	MC1776CG
uA776MH	THOMSON	MC1776G
uA776TC	FAIRCHILD	MC1776CP1
uA7805CK	THOMSON	L7805CT
uA7805CKC	TEXAS	L7805CV
uA7805CSP	THOMSON	L7805CV
uA7805KC	FAIRCHILD	L7805CT
uA7805KM	FAIRCHILD	L7805T
uA7805UC	FAIRCHILD	L7805CV
uA7806CK	THOMSON	L7806CT
uA7806CKC	TEXAS	L7806CV
uA7806CSP	THOMSON	L7806CV
uA7806KC	FAIRCHILD	L7806CT
uA7806KM	FAIRCHILD	L7806T
uA7806UC	FAIRCHILD	L7806CV
uA7808CKC	TEXAS	L7808CV
uA7808KC	FAIRCHILD	L7808CT
uA7808KM	FAIRCHILD	L7808T
uA7808UC	FAIRCHILD	L7808CV
uA7812CK	THOMSON	L7812CT
uA7812CKC	TEXAS	L7812CV
uA7812CSP	THOMSON	L7812CV
uA7812KC	FAIRCHILD	L7812CT
uA7812KM	FAIRCHILD	L7812T
uA7812UC	FAIRCHILD	L7812CV
uA7815CK	THOMSON	L7815CT
uA7815CKC	TEXAS	L7815CV
uA7815CSP	THOMSON	L7815CV
uA7815KC	FAIRCHILD	L7815CT
uA7815KM	FAIRCHILD	L7815T
uA7815UC	FAIRCHILD	L7815CV
uA7818CK	THOMSON	L7818CT
uA7818CKC	TEXAS	L7818CV
uA7818CSP	THOMSON	L7818CV
uA7818KC	FAIRCHILD	L7818CT

INDUSTRY TYPE	SOURCE	SGS TYPE
uA7818KM	FAIRCHILD	L7818T
uA7818UC	FAIRCHILD	L7818CV
uA7824CK	THOMSON	L7824CT
uA7824CKC	TEXAS	L7824CV
uA7824CSP	THOMSON	L7824CV
uA7824KM	FAIRCHILD	L7824T
uA7824UC	FAICHILD	L7824CV
uA78M05CKC	TEXAS	L78M05CV
uA78M05UC	FAIRCHILD	L78M05CV
uA78M06CKC	TEXAS	L78M06CV
uA78M06UC	FAIRCHILD	L78M06CV
uA78M08CKC	TEXAS	L78M08CV
uA78M08UC	FAICHILD	L78M08CV
uA78M12CKC	TEXAS	L78M12CV
uA78M12UC	FAICHILD	L78M12CV
uA78M15CKC	TEXAS	L78M15CV
uA78M15UC	FAIRCHILD	L78M15CV
uA78M24CKC	TEXAS	L78M24CV
uA78M24UC	FAIRCHILD	L78MM24CV
uA7905CK	THOMSON	L7905CT
uA7905CKC	TEXAS	L7905CV
uA7905CSP	THOMSON	L7905CV
uA7905KC	FAIRCHILD	L7905CT
uA7905UC	FAIRCHILD	L7905CV
uA7908CKC	TEXAS	L7908CV
uA7908KC	FAIRCHILD	L7908CT
uA7908UC	FAIRCHILD	L7908CV
uA7912CK	THOMSON	L7912CT
uA7912CKC	TEXAS	L7912CV
uA7912CSP	THOMSON	L7912CV
uA7912KC	FAIRCHILD	L7912CT
uA7912UCF	FAIRCHILD	L7912CV
uA7915CK	THOMSON	L7915CT
uA7915CKC	TEXAS	L7915CV
uA7915CSP	THOMSON	L7915CV
uA7915KC	FAIRCHILD	L7915CT
uA7915UC	FAIRCHILD	L7915CV
uA7918CKC	TEXAS	L7918CV
uA7924CKC	TEXAS	L7924CV
uA7952CKC	TEXAS	L7952CV
uA9665DC	FAIRCHILD	ULQ2001R
uA9665PC	FAIRCHILD	ULN2001A
uA9666DC	FAIRCHILD	ULQ2002R
uA9666PC	FAIRCHILD	ULN2002A
uA9667DC	FAIRCHILD	ULQ2003R
uA9667PC	FAIRCHILD	ULN2003A
uA9668DC	FAIRCHILD	ULQ2004R
uA9668PC	FAIRCHILD	ULN2004A

DATASHEETS

AM26LS31

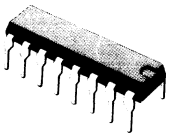
PRELIMINARY DATA

QUAD HIGH SPEED DIFFERENTIAL LINE DRIVER

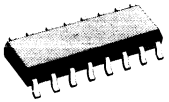
- OUTPUT SKEW -2.0ns TYPICAL
- INPUT TO OUTPUT DELAY -12ns
- OPERATION FROM SINGLE +5V SUPPLY
- OUTPUTS WON'T LOAD LINE WHEN $V_{CC} = 0$
- OUTPUT SHORT-CIRCUIT PROTECTION
- COMPLEMENTARY OUTPUTS
- MEETS THE REQUIREMENTS OF EIA STANDARD RS-422
- HIGH OUTPUT DRIVE CAPABILITY FOR 100Ω TERMINATED TRANSMISSION LINES

The AM26LS31 is a quad differential line driver, designed for digital data transmission over balanced lines. The AM26LS31 meets all the requirements of EIA standard RS-422 and federal standard 1020. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines.

The circuit provides an enable and disable function common to all four drivers. The AM26LS31 features 3-state outputs and logical OR-ed complementary enable inputs. The inputs are all LS compatible and are all one unit load.



DIP-16 Plastic (0.25) **and Ceramic**

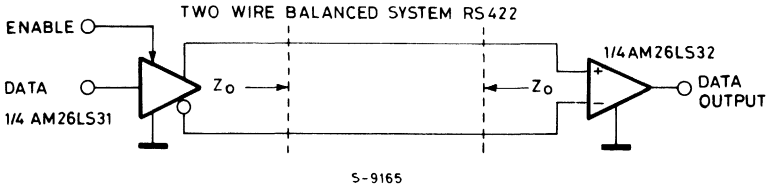


SO-16J

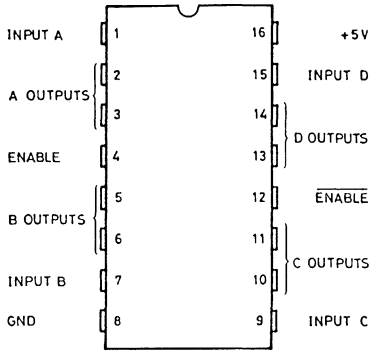
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	7	V
V_i	Input voltage	7	V
V_o	Output voltage	5.5	V
T_{stg}	Storage temperature range	-65 to 150	°C

Fig. 1 - Typical Application



CONNECTION DIAGRAM
(Top view)



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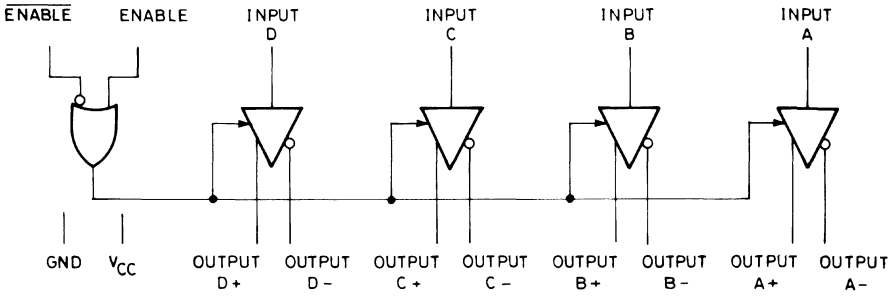
ORDERING INFORMATION

Package Type	Temperature Range	Order Number
DIP-16 Ceramic	-55 to 125°C	AM26LS31MJ
	0 to 70°C	AM26LS31CJ
DIP-16 Plastic	0 to 70°C	AM26LS31CN
SO-16J	0 to 70°C	AM26LS31D1

LOGIC DIAGRAM



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THERMAL DATA			DIP-16 Ceramic	DIP-16 Plastic	SO-16
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max.	150°C/W	200°C/W	165°C/W

ELECTRICAL CHARACTERISTICS (The following conditions apply unless otherwise specified: T_{amb} = -55°C to 125°C, V_{CC} = 5V ± 10%; T_{amb} = 0 to +70°C, V_{CC} = 5V ± 5%)

Parameter		Test Conditions	Min.	Typ. (Note 1)	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}= Min., I_{OH}= -20mA	2.5	3.2		V
V_{OL}	Output LOW Voltage	V_{CC}= Min., I_{OL}= 20mA		0.32	0.5	V
V_{IH}	Input HIGH Voltage	V_{CC}= Min.	2.0			V
V_{IL}	Input LOW Voltage	V_{CC}= Max.			0.8	V
I_{IL}	Input LOW Current	V_{CC}= Max., V_{IN}= 0.4V		-0.20	-0.36	mA
I_{IH}	Input HIGH Current	V_{CC}= Max., V_{IN}= 2.7V		0.5	20	µA
I_I	Input Reverse Current	V_{CC}= Max., V_{IN}= 7.0V		0.001	0.1	mA
I_O	Off-State (High Impedance) Output Current	V_{CC} = Max., V_O= 2.5V		0.5	20	µA
		V_{CC} = Max., V_O= 0.5V		0.5	-20	µA
V_I	Input Clamp Voltage	V_{CC}= Min., I_{IN}= 18mA		-0.8	-1.5	V
I_{SC}	Output Short Circuit Current	V_{CC}= Max.	-30	-60	-150	mA
I_{CC}	Power Supply Current	V_{CC}= Max., all outputs disabled		60	80	mA
t_{PLH}	Input to Output	V_{CC}= 5.0V, T_{amb}= 25°C, Load = Note 2		12	20	ns
t_{PHL}	Input to Output	V_{CC}= 5.0V, T_{amb}= 25°C, Load = Note 2		12	20	ns
SKEW	Output to Output	V_{CC}= 5.0V, T_{amb}= 25°C, Load = Note 2		2.0	6.0	ns
t_{LZ}	Enable to Output	V_{CC}= 5.0V, T_{amb}= 25°C, C_L = 10pF		23	35	ns
t_{HZ}	Enable to Output	V_{CC}= 5.0V, T_{amb}= 25°C, C_L= 10pF		17	30	ns
t_{ZL}	Enable to Output	V_{CC}= 5.0V, T_{amb}= 25°C, Load = Note 2		35	45	ns
t_{ZH}	Enable to Output	V_{CC}= 5.0V, T_{amb}= 25°C, Load = Note 2		30	40	ns

Notes: 1. A typical values are V_{CC} = 5.0V, T_{amb} = 25°C
2. C_L = 30pF, V_{IN} = 1.3V to V_{OUT} = 1.3V, V_{PULSE} = 0V to +3.0V, See Below.

Fig. 2 - Guaranteed V_{OH} and V_{OL} (T_{amb} = -55 °C to +125°C)

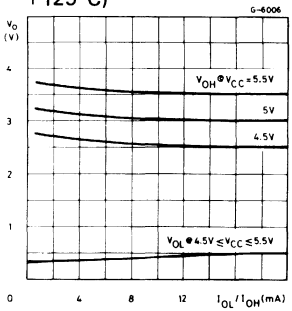


Fig. 3 - V_{OUT} vs. V_{CC}

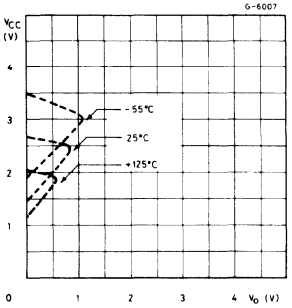


Fig. 4 - AC load test circuit for three-state outputs

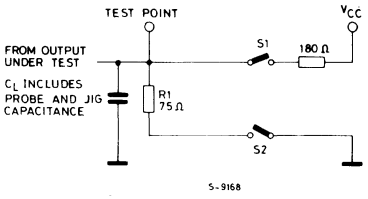


Fig. 5 - Propagation delay (Notes 1 and 3)

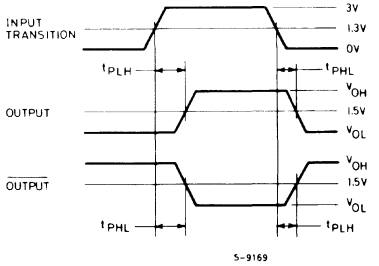
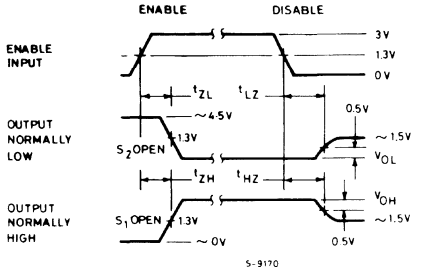


Fig. 6 - Enable and disable times (Notes 2 and 3)



Notes: 1. Diagram shown for $\overline{\text{Enable}}$ LOW.
2. S1 and S2 of Load Circuit are closed except where shown.
3. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_o = 50Ω; t_r ≤ 15ns; t_f ≤ 6.0ns.

AM26LS32
AM26LS33

PRELIMINARY DATA

RS422 AND RS423 QUAD DIFFERENTIAL LINE RECEIVERS

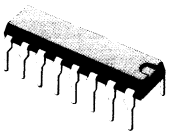
- THE AM26LS32 MEETS ALL THE REQUIREMENTS OF RS-422 AND RS-423
- 6K MINIMUM INPUT IMPEDANCE
- 30mV INPUT HYSTERESIS
- OPERATION FROM SINGLE +5V SUPPLY
- FAIL SAFE INPUT-OUTPUT RELATIONSHIP. OUTPUT ALWAYS HIGH WHEN INPUTS ARE OPEN
- THREE-STATE DRIVE, WITH CHOICE OF COMPLEMENTARY OUTPUT ENABLES, FOR RECEIVING DIRECTLY ONTO A DATA BUS
- PROPAGATION DELAY 17ns TYPICAL

The AM26LS32 is quad line receiver designed to meet the requirements of RS-422 and RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

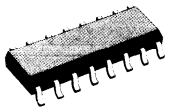
The AM26LS32 features an input sensitivity of 200mV over the input voltage range of ± 7V.

The AM26LS33 features an input sensitivity of 500mV over the input voltage range of ± 15V.

The AM26LS33 provide an enable and disable function common to all four receivers. Both parts feature 3-state outputs with 8mA sink capability and incorporate a fail safe input-output relationship which keeps the outputs high when the inputs are open.



DIP-16 Plastic (0.25) **and Ceramic**



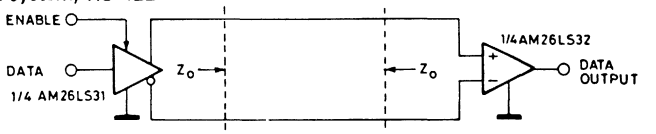
SO-16J

ABSOLUTE MAXIMUM RATINGS

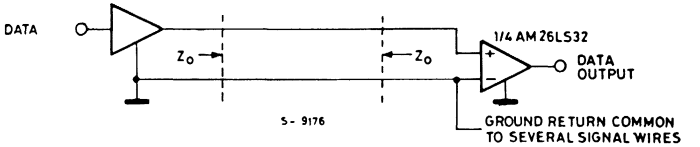
V_s	Supply voltage	7	V
CMR	Common mode range	± 25	V
V_i	Differential input voltage	± 25	V
V_E	Enable voltage	7	V
I_{os}	Output sink current	50	mA
T_{stg}	Storage temperature range	-65 to 150	°C

Fig. 1 - Typical Applications

Two wire balanced system, RS-422

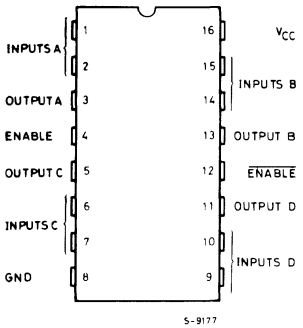


Single wire with common ground imbalanced system, RS-423



AM26LS32
AM26LS33

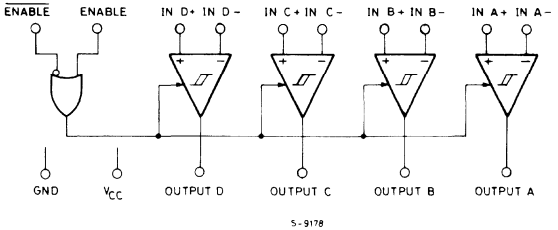
CONNECTION DIAGRAM
(Top view)



ORDERING INFORMATION

Package Type	Temperature Range	AM26LS32	AM26LS33
		Order Number	Order Number
Hermetic DIP	-55 to 125°C	AM26LS32MJ	AM26LS33MJ
Hermetic DIP	0 to 70°C	AM26LS32CJ	AM26LS33CJ
Molded DIP	0 to 70°C	AM26LS32CN	AM26LS33CN
SO-16J	0 to 70°C	AM26LS32D1	AM26LS33D1

LOGIC DIAGRAM



THERMAL DATA

			DIP-16 Ceramic	DIP-16 Plastic	SO-16
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	150°C/W	200°C/W	165°C/W

ELECTRICAL CHARACTERISTICS (The following conditions apply unless otherwise specified: T_{amb} = -55°C to 125°C, V_{CC} = 5V ± 10%; T_{amb} = 0 to 70°C, V_{CC} = 5V ± 5%)

Parameter		Test Conditions		Min.	Typ. (1)	Max.	Unit
V_{TH}	Differential Input Voltage .	V_{OUT} = V_{OL} or V_{OH}	AM26LS32, -7V ≤ V_{CM} ≤ +7V	-0.2	±0.06	+0.2	V
			AM26LS33, -15V ≤ V_{CM} ≤ +15V	-0.5	±0.12	+0.5	
R_{IN}	Input Resistance	-15V ≤ V_{CM} ≤ +15V (One input AC ground)		6.0	9.8		KΩ
I_{IN}	Input Current (Under Test)	V_{IN} = +15V, Other Input -15V ≤ V_{IN} ≤ +15V				2.3	mA
I_{IN}	Input Current (Under Test)	V_{IN} = -15V, Other input -15V ≤ V_{IN} ≤ +15V				-2.8	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., ΔV_{IN} = +1.0V	COM'L	2.7	3.4		V
		$V_{\overline{ENABLE}}$ = 0.8V, I_{OH} = -440μA	MIL	2.5	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = Min., ΔV_{IN} = -1.0V	I_{OL} = 4.0mA			0.4	V
		V_{ENABLE} = 0.8V	I_{OL} = 8.0mA			0.45	
V_{IL}	Enable LOW Voltage					0.8	V
V_{IH}	Enable HIGH Voltage			2.0			V
V_I	Enable Clamp Voltage	V_{CC} = Min., I_{IN} = -18mA				-1.5	V
I_O	Off-State (High Impedance) Output Current	V_{CC} = Max.	V_O = 2.4V			20	μA
			V_O = 0.4V			-20	
I_{IL}	Enable LOW Current	V_{IN} = 0.4V			-0.2	-0.36	mA
I_{IH}	Enable HIGH Current	V_{IN} = 2.7V			0.5	20	μA
I_I	Enable Input High Current	V_{IN} = 5.5V			1	100	μA
I_{SC}	Output Short Circuit Curr.	V_O = 0V, V_{CC} = Max., ΔV_{IN} = +1.0V		-15	-50	-85	mA
I_{CC}	Power Supply Current	V_{CC} = Max., All V_{IN} = GND, Output Disabled			52	70	mA
V_{HYST}	Input Hysteresis	T_{amb} = 25°C, V_{CC} = 5.0V, V_{CM} = 0V			30		mV
t_{PLH}	Input to Output	T_{amb} = 25°C, V_{CC} = 5.0V, C_L = 15pF, see test cond. below			17	25	ns
t_{PHL}	Input to Output	T_{amb} = 25°C, V_{CC} = 5.0V, C_L = 15pF, see test cond. below			17	25	ns
t_{LZ}	Enable to Output	T_{amb} = 25°C, V_{CC} = 5.0V, C_L = 5pF, see test cond. below			20	30	ns
t_{HZ}	Enable to Output	T_{amb} = 25°C, V_{CC} = 5.0V, C_L = 5pF, see test cond. below			15	22	ns
t_{ZL}	Enable to Output .	T_{amb} = 25°C, V_{CC} = 5.0V, C_L = 15pF, see test cond. below			15	22	ns
t_{ZH}	Enable to Output	T_{amb} = 25°C, V_{CC} = 5.0V, C_L = 15pF, see test cond. below			15	22	ns

(1) All typical values are V_{CC} = 5.0V, T_{amb} = 25°C

Fig. 2 - Load test circuit for three-state outputs

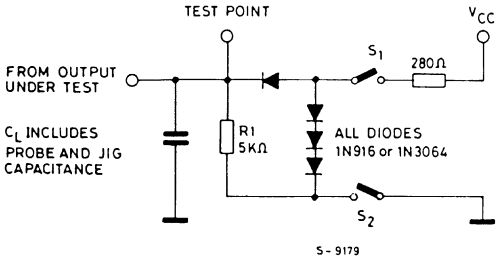


Fig. 3 - Propagation delay (notes 2 and 3)

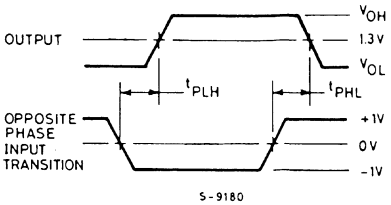
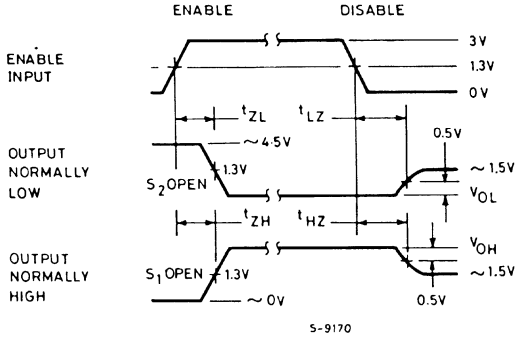


Fig. 4 - Enable and disable time (notes 2 and 3)



Notes: 1. Diagram shown for $\overline{\text{Enable}}$ LOW
2. S1 and S2 of Load Circuit are closed except where shown.
3. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_o = 50\Omega$; $t_r \leq 15$ns; $t_f \leq 6.0$ns

AM6012
AM6012A

PRELIMINARY DATA

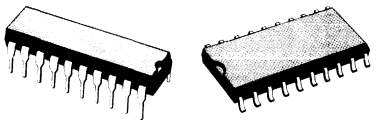
12-BIT HIGH SPEED MULTIPLYING D/A CONVERTERS

The AM6012 is an industry standard monolithic 12-bit digital-to analog converter. Complementary current output and high speed multiplying capability make the AM6012 useful in a wide range of applications such as video displays, process control circuitry and fast A/D converters. The 6012 is the first D/A to achieve 12-bit differential linearity without the use of thin film resistors or active trimming. The 6012's unique circuit design insures monotonicity without the precision trimming associated with most other 12-bit DAC architectures.

The AM6012 is packaged in a 20-pin plastic DIP and is SO-20L for surface mounting. Although tested and specified at ±15V, the AM6012 works well over a wide range of power supply voltages. Performance is essentially independent of supply voltage over the range of +5 volts, −12 volts to ±18 volts. The AM6012 series guarantees full 12-bit monotonicity for all grades and differential nonlinearity as high as 0.012% (13 bits) for the A grades and 0.025% (12 bits) for the standard grades over the entire temperature range.

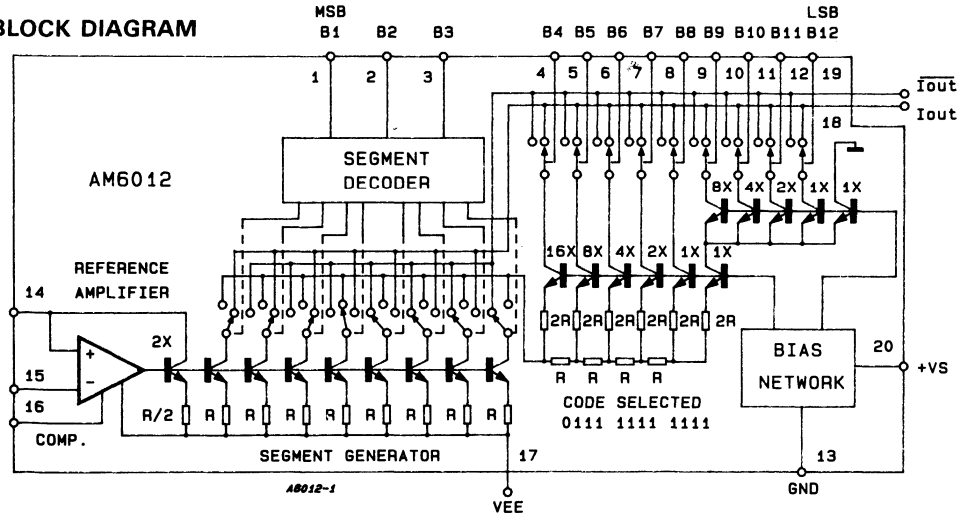
Guaranteed monotonicity and low cost make the AM6012 an ideal choice for high volume applications requiring fine local resolution. Typical applications include printer graphics and video displays. These applications need a minimum of 12 bits of resolution, although conformance to an ideal straight line from zero to full scale is less important.

- ALL GRADES 12-BIT MONOTONIC OVER TEMPERATURE
- DIFFERENTAL NONLINEARITY TO ±0.012% (13 BITS) MAX OVER TEMPERATURE (A GRADES)
- 250ns TYPICAL SETTLING TIME
- FULL SCALE CURRENT 4mA
- HIGH SPEED MULTIPLYING CAPABILITY
- TTL/CMOS/ECL/HTL COMPATIBLE
- HIGH OUTPUT COMPLIANCE: −5V TO +10V
- COMPLEMENTARY CURRENT OUTPUTS
- LOW POWER CONSUMPTION: 230mW



DIP-20 Plastic (0.4) **SO-20L**

BLOCK DIAGRAM



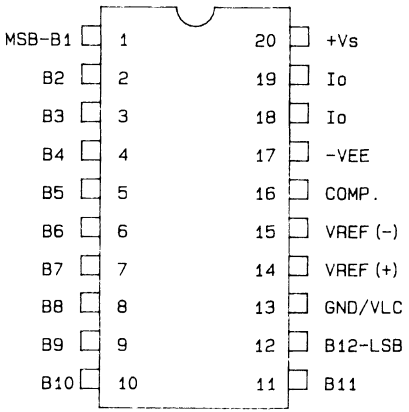
ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	0 to 70	°C
Storage Temperature	−65 to + 125	°C
Power Supply Voltage	±18	V
Logic Inputs	−5 to +18	V
Voltage at Current Outputs Pins	−8 to +12	V
Reference Inputs	$+V_S$ to $-V_{EE}$ ±18V max Differential	V
Reference Input Current	1.25	mA

CONNECTION DIAGRAM AND ORDERING INFORMATION

Type	Differential linearity (%)	Temperature Range (°C)	Package
AM6012PC	0.025	0 to 70	DIP.20
AM6012APC	0.012		
AM6012 D	0.025	0 to 70	SO.20L
AM6012 AD	0.012		

(TOP VIEW)



A6012-2

THERMAL DATA

$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	100 °C/W

ELECTRICAL CHARACTERISTICS

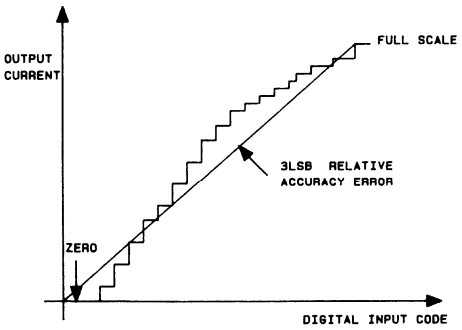
These specifications apply for $V_S = +15V$, $V_{EE} = -15V$, $I_{REF} = 1.0mA$, over the operating temperature range unless otherwise specified

Param.	Description	Test Conditions	AM6012A			AM6012			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
	Resolution		12	12	12	12	12	12	Bits
	Monotonicity		12	12	12	12	12	12	Bits
D.N.L.	Differential Nonlinearity	Deviation from ideal step size	–	–	±.012	–	–	±.025	%FS
			13	–	–	12	–	–	Bits
N.L.	Nonlinearity	Deviation from ideal straight line	–	–	±.05	–	–	±0.05	%FS
I_{FS}	Full Scale Current	$V_{REF} = 10.000V$ $R_{14} = R_{15} = 10.000k\Omega$ $T_A = 25°C$	3.967	3.999	4.031	3.935	3.999	4.063	mA
TCI_{FS}	Full Scale Temp.Co.		–	±5	±20	–	±10	±40	ppm°C
			–	±.0005	±.002		±.001	±.004	%FS°C
V_{OC}	Output Voltage Compliance	D.N.L. Specification guaranteed over compliance range $R_{OUT} > 10$ megohme typ.	−5	–	+10	−5	–	+10	V
I_{FSS}	Full Scale Symmetry	I_{FS}-I_{FS}	–	±0.2	±1.0	–	±0.4	±2.0	μA
I_{ZS}	Zero Scale Current		–	–	0.10	–	–	0.10	μA
I_S	Setting Time	To ±1/2 LSB, all bits ON or OFF, $T_A = 25°C$	–	250	500	–	250	500	nSec
t_{PLH} t_{PHL}	Propagation Delay - all bits	50% to 50%	–	25	50	–	25	50	nSec
C_{OUT}	Output Capacitance		–	20	–	–	20	–	pF
V_{IL}	Logic Input Levels — Logic "0"		–	–	0.8	–	–	0.8	V
V_{IH}	Logic Input Levels — Logic "1"		2.0	–	–	2.0	–	–	
I_{IN}	Logic Input Current	$V_{IN} = -5$ to $+18V$	–	–	40	–	–	40	μA
V_{IS}	Logic Input Swing	$V_{EE} = -15V$	−5	–	+18	−5	–	+18	V
I_{REF}	Reference Current Range		0.2	1.0	1.1	0.2	1.0	1.1	mA
I_{15}	Reference Bias Current		0	−0.5	−2.0	0	−0.5	−2.0	μA

ELECTRICAL CHARACTERISTICS (Continued)

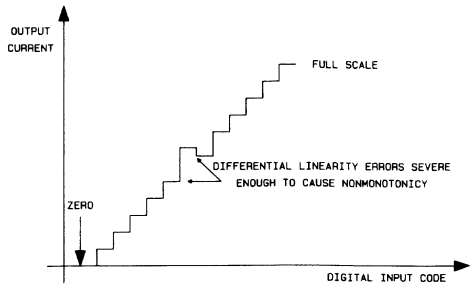
Param.	Description	Test Conditions	AM6012A			AM6012			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
di/dt	Reference Input Slew Rate	$R_{14(eq)} = 800\Omega$ CC = 0pF	4.0	8.0	–	4.0	8.0	–	mA/μs
$PSSI_{FS+}$	Power Supply Sensitivity	$V_S = (+13.5V$ to $+16.5V)$ $V_{EE} = -15V$	–	±.00005	±.001	–	±0.0005	±.001	%FS/%
$PSSI_{FS-}$		$V_{EE} = -13.5V$ to $-16.5V$ $V_S = +15V$	–	±.00025	±.001	–	±.00025	±.001	
V_S	Power Supply Range	$V_{OUT} = 0V$	4.5	–	18	4.5	–	18	V
V_{EE}			−18	–	−10.8	−18	–	−10.8	
I+	Power Supply Current	$V_S = +5V$, $V_{EE} = -15V$	–	5.7	8.5	–	5.7	8.5	mA
I−			–	−13.7	−18.0	–	−13.7	−18.0	
I+		$V_S = +15V$, $V_{EE} = -15V$		5.7	8.5	–	5.7	8.5	
I−			–	−13.7	−18.0	–	−13.7	−18.0	
P_D	Power Dissipation	$V_S = +5V$, $V_{EE} = -15V$	–	234	312	–	234	312	mW
		$V_S = +15V$, $V_{EE} = -15V$	–	291	397	–	291	397	

Fig. 1 - Relative Accuracy Error



A6012-10::DIS

Fig. 2 - Example of Nonmonotonic Behavior



A6012-10::LIB

APPLICATION INFORMATION

FUNCTIONAL DESCRIPTION

The segmented design of the AM6012, shown in the block diagram, insures that there are no significant differential nonlinearities in the transfer characteristic. The eight major carries of the most significant bits are not subject to the gross differential nonlinearities that can occasionally occur in an R-2R type DAC. This advantage is due to the fundamentally different way that the current is handled in an AM6012. In a conventional R-2R type DAC, when the input code is increemented past a major carry, a current representing the new code is substituted for the sum of all the less significant bit currents that were previously on. To avoid any nonlinearities, the two total currents must be extremely well matched. In the case of the MSB major carry in a 12-bit DAC, the match must be better than one part in 2048 to maintain monotonicity. However, in the AM6012, a new current is never substituted for the sum of several smaller ones, but redirected through alternate channels and incremented one step at a time.

For example, consider the MSB carry in an AM6012. In the initial state of 011111111111 as shown in the block diagram, the switches in the segment generator are set in such a way that currents I_0, I_1 and I_2 are steered directly into the noninverting output I_{OUT}. In addition, a portion of I_3 is directed through the 9-bit DAC that is controlled by the 9 least significant bits into I_{OUT}. With the 9LSBs set to "1", all of the I_3 current is directed to I_{OUT} except for the 1/512 that goes to ground through the right-most transistor in the 9-bit DAC. After the input word is changed to 100000000000, the segment decoder switch for I_3 will be all the way to the right, the switch for I_4 will be in the middle, and all the switches in the 9-bit DAC will be to the left. I_{OUT} will be composed of I_0, I_1, I_2 and I_3. None of I_4 will be directed into I_{OUT} until a higher code is reached. In other words, I_3 is now steered directly to I_{OUT} instead of being divided by a factor of 511/512 in the 9-bit DAC. Since no major current substitution occurs, there is less chance of a large nonlinearity at this transition than in a comparable R-2R DAC.

RELATIVE ACCURACY VS. DIFFERENTIAL NONLINEARITY

SGS defines relative accuracy as the maximum deviation of the actual, adjusted DAC output from the ideal analog output (a straight line drawn between the lowest code output voltage and the highest code output voltage) for any bit combination. Relative accuracy is often referred to as nonlinearity. The DAC transfer function shown in Figure 1 has a bow that results in a maximum relative accuracy error of 3LSB. This must be distinguished from a differential linearity error. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a ILSB change in digital input code.

For example, for a 4mA full scale output, a change of ILSB in digital input code should result in a 0.98μA change in the analog output current (ILSB = 4mA x 1/4096 = 0.98μA). If in actual use, however, a ILSB change in the input code results ina change of only 0.24μA (1/4LSB) in output current, the differential linearity error would be 0.74μA or 3/4LSB.

The AM6012 has very good differential linearity in spite of the porr relative accuracy. Conversely, the DAC of Figure 1 has very good relative accuracy but poor differential linearity. The anomaly in the middle of the transfer function is the result of a positive differential linearity error followed by a negative differential linearity error greater than 1LSB. A negative output step for an increase in digital input code is referred to as nonmonotonic behavior. In general, if a DAC has a differential linearity error specification greater than 1LSB, it may be nonmonotonic at one or more of the major carries. In most case the worst differential linearity error will occur at the MSB transition point.

As noted in the functional description, the 6012's unique design minimizes differential linearity errors at the transition points of the 3MSBs. This results in a tight specification on maximum differential nonlinearity over temperature. Differential linearity is verified on all AM6012s with 100% final testing. In many converter applications, uniform step size (or minimum differential linearity error) is more important than conformance to an ideal straight line. Twelve-bit onverters are usually needed for high resolution rather than high linearity as evidenced by the fact that few transducers are more linear than 0.1%. This is also true in video graphics, where the human eye has difficulty discerning nonlinearity of less than 5%. The AM6012 is especially well suited for these applications since it has inherently low differential linearity error.

APPLICATION INFORMATION (Continued)

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided where $I_O + I_{\overline{O}} = I_{FR}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 18 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 18 and turned on at pin 19. A decreasing logic count increase $I_{\overline{O}}$ as in a negative or inverter logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FR}; do not leave an unused output pin one.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 25V above V− and is independent of the positive supply. Negative compliance is +10V above V−.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The AM6012 operates over a wide range of power supply voltages from a total supply of 20V to 36V. When operating with V− supplies of −10V or less, $I_{REF} \leq 1mA$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common mode range, negative logic input range, and negative logic threshold range; consult the various figures fro guidance. For example, operation at −9V with $I_{REF} = 1mA$ is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the AM6012 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be used to insure logic swings, etc. remain between acceptable limits.

TEMPERATURE PERFORMANCE

The nonlinearity and mononicity specifications of the AM6012 are guaranteed to apply over the entire rated operating temperature range. Full scale output current drift is flight, typically ±10ppm/°C with zero scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R14 should match and track that of the output resistor for minimum overall full scale drift.

SETTLING TIME

The AM6012 is capable of extremely fast settling times, typically 250ns at $I_{REF} = 1.0mA$. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 25ns for each of the 12 bits. Settling time to within 1/2 LSB of the LSB is therefore 25ns, with each progressively larger bit taking successively longer. The MSB settles in 250ns, thus determining the overall settling time of 250ns. Settling to 10-bit accuracy requires about 90 to 130ms. The output capacitance of the AM6012 including the package is approximately 20pF; therefore, the output RC time constant dominates settling time if $R_L > 500\Omega$.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 0.5mA, with gradual increases for lower I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve ±2μA, therefore a 2.5kΩ load is needed to provide adequate drive for most oscilloscopes. At I_{REF} values of less than 0.5mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 011111111111 to 100000000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.1% of the final value, and thus settling times may be observed at lower values of I_{REF}.

AM6012 switching transients or "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

APPLICATION INFORMATION (Continued)

Fastest operation can be octained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference, and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1μF capacitors at the supply pins provide full transient protection.

REFERENCE AMPLIFIER SETUP

The AM6012 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +1.0mA. The full range output current is a linear function of the reference current and is given by:

$$I_{RF} = \frac{4095}{4096} \times 4 \times (I_{REF}) = 3.999\ I_{REF},$$

where $I_{REF} = I_{14}$

In positive reference applications, an external positive reference voltage forces current through R14 into the $V_{REF(+)}$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at pin 15. Reference current flows from ground through R14 into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R15 (nominally equal to R14) is used to cancel bias current errors. (Figure 3).

Bipolar references may be accommodated by offsetting V_{REF} or pin 15. The negative common-mode range of the reference amplifier is given by: $V_{CM-} = V-$ plus ($I_{REF} \times 3k\Omega$) plus 1.8V. The positive common-mode range is V+ less 1.23V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R14 should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full scale trimming may be accomplished by adjusting the value of R14, or by using a potentiometer for R14.

MULTIPLYING OPERATION

The AM6012 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 1mA to 1μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 1.0mA.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V−. The value of this capacitor depends on the impedance presented to pin 14. For R14 values of 1.0, 2.5 and 5 OkΩ; minimum values of C_C are 5, 12 and 25 pF. Larger values of R14 require proportionately increased values of C_C for proper phase margin (See Figure 4 and 5).

For fastest response to a pulse, low values of R14 enabling small C_C values should be used. If pin 14 is driven be a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall compensated which will decrease overall bandwidth and slew rate. For R14 = 1kΩ and C_C = 5pF, the reference amplifier slews at 4mA/ms enabling a transition from $I_{REF} = 0$ to I_{REF} = 1mA in 250ns.

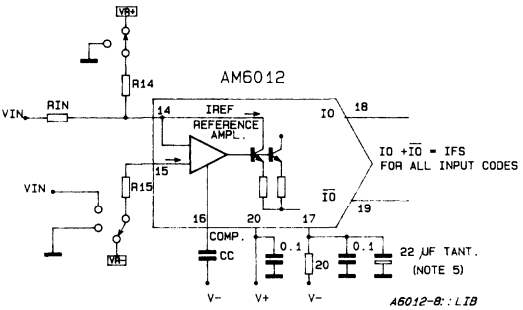
Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme. This technique provides lowest full scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff ($I_{REF} = 0$) condition. Full scale transition (0 to 1mA) occurs in 62.5ns when the equivalent impedance at pin 14 is 800Ω and $C_C = 0$. This yields a reference slew rate of 8mA/μs which is relatively independent of R_{IN} and V_{IN} values.

APPLICATION INFORMATION (Continued)

LOGIC INPUTS

The AM6012 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 40μA logic input current, and completely adjustable logic inputs may swing between −5 and +10V. This enables direct interface with +15V CMOS logic, even when the AM6012 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 13, V_{LC}). For TTL interface, simply ground pin 13. When interfacing ECL, an $I_{REF} \leq 1mA$ is recommended. For interfacing other logic families, see block titled "Interfacing With Various Logic Families". For general setup of the logic control circuit, it should be noted that pin 13 will sink 1.1mA typical, external circuitry should be designed to accommodate this current (Figure 6).

Fig. 3 - Reference amplifier biasing



Reference Configuration	R_{14}	R_{15}	R_{IN}	C_C	I_{REF}
Positive Reference	V_{R+}	0V	N/C	.01μF	V_{R+}/R_{14}
Negative Reference	0V	V_{R-}	N/C	.01μF	$-V_{R-}/R_{14}$
Lo Impedance Bipolar Reference	V_{R+}	0V	V_{IN}	(Note 1)	$V_{R+}/R_{14}) + (V_{IN}/R_{IN})$ (Note 2)
Hi Impedance Bipolar Reference	V_{R+}	V_{IN}	N/C	(Note 1)	$(V_{R+} - V_{IN})/R_{14}$ (Note 3)
Pulsed Reference (Note 4)	V_{R+}	0V	V_{IN}	No Cap	$(V_{R+}/R_{14}) + (V_{IN}/R_{IN})$

Notes:
1. The compensation capacitor a function of the impedance seen at the $+V_{REF}$ input and must be at least $5pF \times R_{14(eq)}$ in kΩ. For $R_{14} < 800\Omega$ no capacitor is necessary.
2. For negative values of V_{IN}, V_{R+}/R_{14} must be greater than $-V_{IN}$ Max/R_{IN} so that the amplifier is not turned off.
3. For positive values of V_{IN}, V_{R+} must be greater than V_{IN} Max so the amplifier is not turned off.
4. For pulsed operation, V_{R+} provides a DC offset and may be set to zero in some cases. The impedance at pin 14 should be 800Ω or less.
5. For optimum settling time, decouple V - with 20Ω and bypass with 22μF tantulum capacitor.
6. Reference current and reference resistor - there is a 1 to 4 schale factor between the reference current (I_{REF}) and the full scale output current (I_{FS}). If $V_{REF} = +10V$ and $I_{FS} = 4mA$, the value of the R_{14} is:

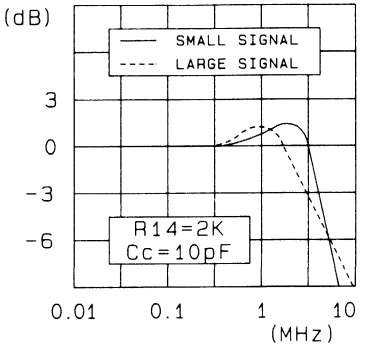
$$R_{14} = \frac{4 \times 10 \text{ Volt}}{4mA} = 10k\Omega \quad R_{14} = R_{15}$$

Fig. 4 - Minimum size compensation capacitor (I_{FS}=4mA, I_{REF}=1.0mA)

$R_{14(EQ)}$(KΩ)	C_C(pF)
10	50
5	25
2	10
1	5
5	0

Note: A 0.01 μF capacitor is recommended for fixed reference operation.

Fig. 5 - Reference Amplifier Frequency response



A6012-11: : DI

Fig. 6 - Interfacing Circuits

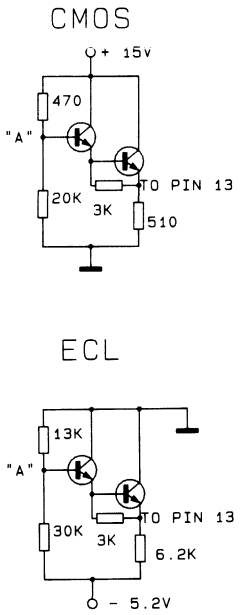


Fig. 7 - Accomodating Bipolar Reference

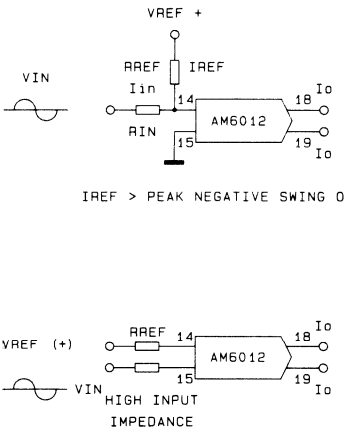
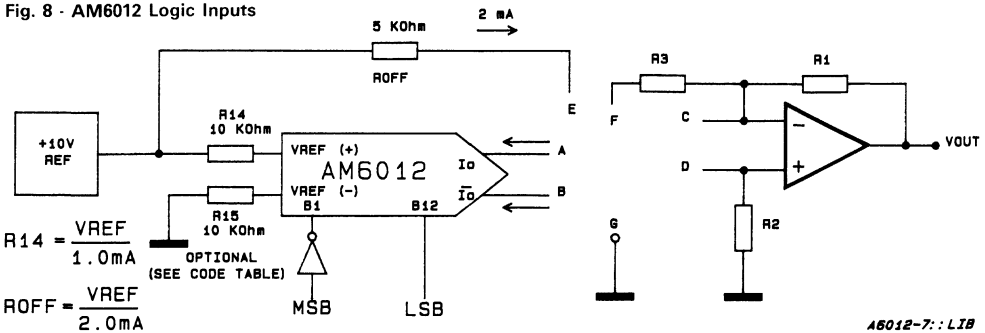


Fig. 8 - AM6012 Logic Inputs



Code Format		Connec.	Output Scale	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_O	$\bar{I}_O$	V_{OUT}
Unipolar	Straight bynary one polarity with true input code, true zero output.	a-c b-g $R_1 = R2 = 2.5K$	Positive full scale Positive full scale-LSB Zero scale	1 1 0	1 1 0	1 1 0	1 1 0	1 1 0	1 1 0	1 1 0	1 1 0	1 1 0	1 1 0	1 1 0	1 0 0	3.999 3.998 .000	.000 .001 3.999	9.9978 9.9951 .0000
	Complementary binary one polarity with complementary input code, true zero output.	a-g b-c R1 = R2 = 2.5K	Positive full scale Positive full scale-LSB Zero scale	0 0 1	0 0 1	0 0 1	0 0 1	0 0 1	0 0 1	0 0 1	0 0 1	0 0 1	0 0 1	0 0 1	0 1 1	.000 .001 3.999	3.999 3.998 .000	9.9976 9.9951 .0000
Symmetrical Offset	Straight offset binary; offset half scale, symmetrical about zero, no true zero output.	a-c b-d f-0 R1 = R3 = 2.5K R2 = 1.25K	Positive full scale Positive full scale-LSB (+) Zero scale (-) Zero scale Negative full scale-LSB Negative full scale	1 1 1 0 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 0 0 1 1 0	3.999 3.998 2.000 1.999 .001 .000	.000 .001 1.999 2.000 3.998 3.999	9.9976 9.9927 .0024 -.0024 -9.9927 -9.9976
	1's complement offset half scale symmetrical about zero, no true zero output MSB complemented (need inverter at B1).	a-c b-d f-g R1 = R3 = 2.5K R2 = 1.25K	Positive full scale Positive full scale-LSB (+) Zero scale (-) Zero scale Negative full scale-LSB Negative full scale	0 0 0 1 1 1	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 0 0 1 1 0	3.999 3.998 2.000 1.999 .001 .000	.000 .001 1.999 2.000 3.998 3.999	9.9976 9.9927 .0024 -.0024 -9.9927 -9.9976
Offset with True Zero	Offset binary, offset half scale, true zero output.	e-a-c b-g R1 = R2 = 5K	Positive full scale Positive full scale-LSB +LSB Zero Scale -LSB Negative full scale+LSB Negative full scale	1 1 1 1 0 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 0 1 0 1 1 0	3.999 3.998 2.001 2.000 1.999 .001 .000	.000 .001 1.998 1.999 2.000 3.998 3.999	9.9951 9.9902 0049 .000 -.0049 -9.9951 -10.000
	2's complement offset half scale true zero output MSB complemented (need inverter at B1)	e-a-c b-g R1 = R2 = 5K	Positive full scale Positive full scale-LSB +1 LSB Zero scale -1 LSB Negative full scale+LSB Negative full scale	0 0 0 0 1 1 1	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 0 1 0 1 1 0	3.999 3.998 2.001 2.000 1.999 .001 .000	.006 .001 1.998 1.999 2.000 3.998 3.999	9.9951 9.9902 .0049 .000 -0.049 -9.9951 -10.000

ADDITIONAL CODE MODIFICATIONS

1. Any of the offset binary codes may be complemented by reversing the output terminal pair.

Fig. 9 - Basic Negative Reference Operation

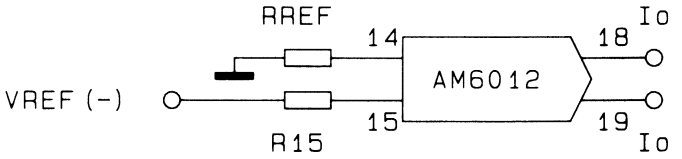


Fig. 10 - Recommended Full-scale Adjustment Circuit

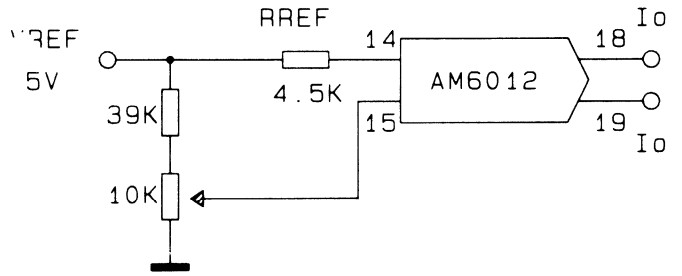


Fig. 11 - 12-BIT High-Speed A/D Converter

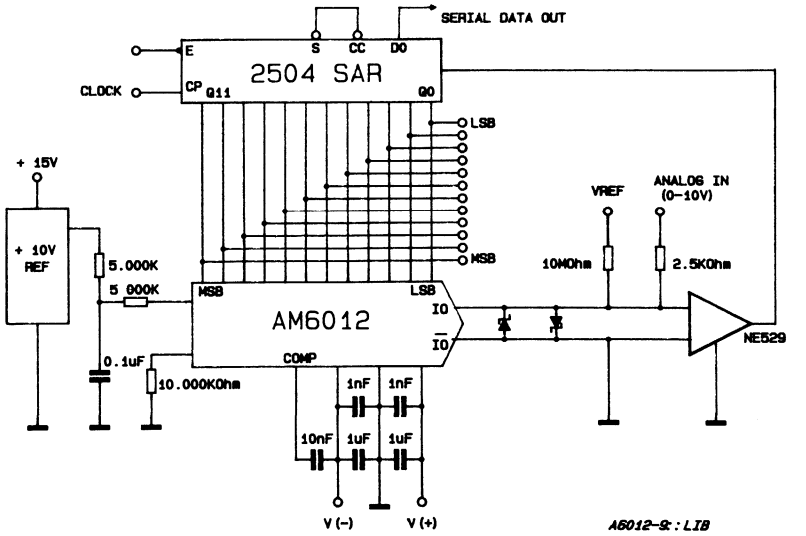


Fig. 12 - Interface with 8-bit Microprocessor Bus

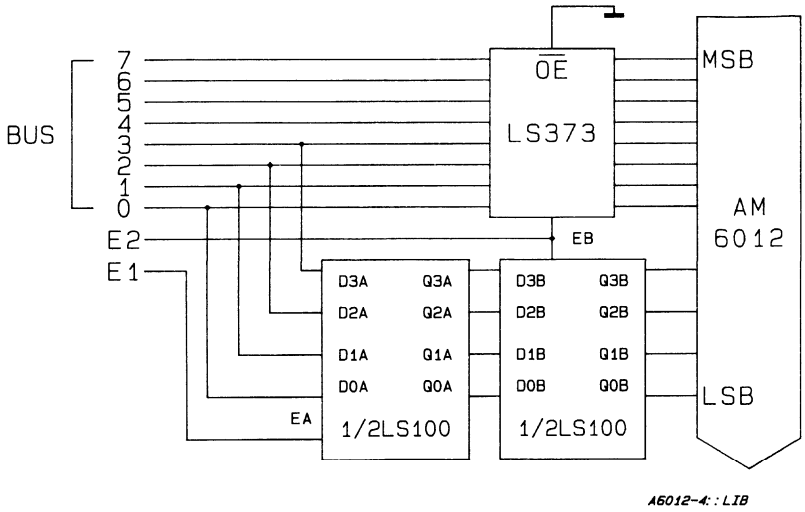
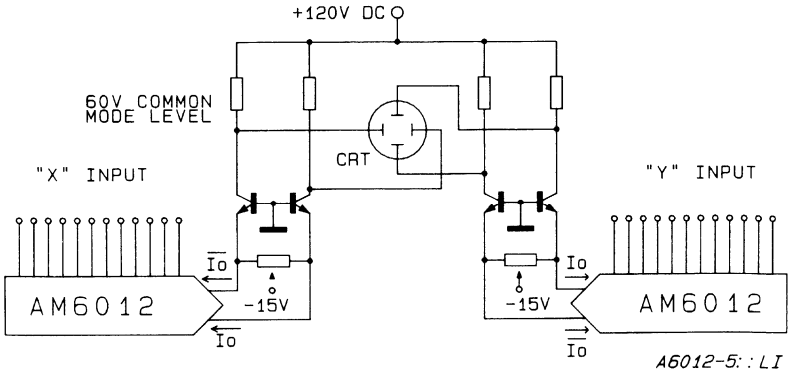


Fig. 13 - CRT Display Driver



DAC0808
DAC0807
DAC0806

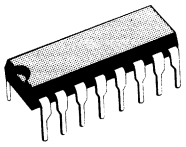
PRELIMINARY DATA

8-BIT D/A CONVERTERS

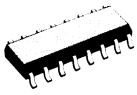
- RELATIVE ACCURACY: ±0.19% ERROR MAXIMUM (DAC0808)
- FULL SCALE CURRENT MATCH: ±1 LSB TYP
- 7 AND 6-BIT ACCURACY AVAILABLE(DAC0807, DAC0806)
- FAST SETTING TIME: 150 ns TYP
- NONINVERTING DIGITAL INPUTS ARE TTL AND CMOS COMPATIBLE
- HIGH SPEED MULTIPLYING INPUT SLEW RATE: 8 mA/μs
- POWER SUPPLY VOLTAGE RANGE: ±4.5V to ±18V
- LOW POWER CONSUMPTION: 33 mW @ ±5V

The DAC0808 series is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with ±5V supplies. No reference current (I_{REF}) trimming is required for most applications since the full scale output current is typically ±1 LSB of 255 $I_{REF}/256$. Relative accuracies of better than ±0.19% assure 8-bit monotonicity and linearity while zero level output current of less than 4 μA provides 8-bit zero accuracy for $I_{REF} \geq 2$ mA. The power supply currents of the DAC0808 series are independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range.

The DAC0808 will interface directly with popular TTL, or CMOS logic levels, and is a direct replacement for the MC1508/MC1408.

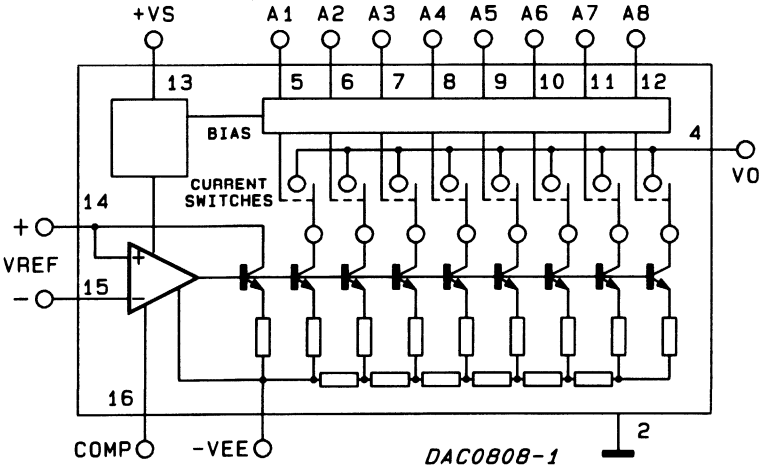


DIP-16 Plastic (0.25) **and Ceramic**



SO-16

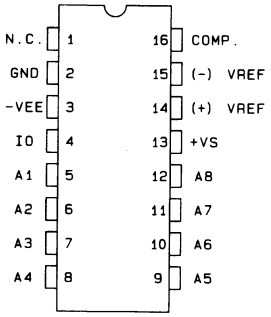
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage		
V_S	+18	V
V_{EE}	−18	V
Digital Input Voltage V5 − V12	−10 V to +18	V
Reference Current, I_{14}	5	mA
Reference Amplifier Inputs, V14, V15	V_{CC}	V_{EE}
Operating Temperature Range		
DAC0808L	$-55°C \leq T_A \leq +125$	°C
DAC0808LC/D	$0 \leq T_A \leq +75$	°C
Storage Temperature Range	−65°C to +150	°C

CONNECTION DIAGRAM AND ORDERING INFORMATION



DAC0808-13

Accuracy	Temperature range	Plastic DIP-16	Ceramic DIP-16	SO-16
8 bit	0 to 75°C	DAC0808LCN	DAC0808LCJ	DAC0808D
7 bit	0 to 75°C	DAC0807LCN	DAC0807LCJ	DAC0807D
6 bit	0 to 75°C	DAC0806LCN	DAC0806LCJ	DAC0806D
8 bit	−55 to 125°C	—	DAC0808LJ	—

THERMAL DATA

			Ceramic DIP-16	SO-16	Plastic DIP-16
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	150°C/W	120°C/W	100°C/W

ELECTRICAL CHARACTERISTICS

($V_S = 5V$, $V_{EE} = -15V$, $V_{REF}/R14 = 2$ mA, $T_A = T_{MIN}$ to T_{MAX} and all digital inputs at high logic level unless otherwise noted.)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
E_r	Relative Accuracy (Error Relative to Full Scale I_O)	*(Figure 10)*				%
	DAC0808L				±0.19	%
	DAC0807LC/D1 (Note 1)				±0.39	%
	DAC0806LC/D1 (Note 1)				±0.78	%
	Settling Time to Within 1/2 LSB (Includes t_{PLH})	$T_A = 25°C$ (Note 2) *(Figure 11)*		150		ns
t_{PLH} t_{PHL}	Propagation Delay Time	$T_A = 25°C$ *(Figure 11)*		30	100	ns
TCI_O	Output Full Scale Current Drift			±20		ppm/°C
MSB	Digital Input Logic Levels	*(Figure 9)*				
V_{IH}	High Level, Logic "1"		2			V_{DC}
V_{IL}	Low Level, Logic "0"				0.8	V_{DC}
MSB	Digital Input Current	*(Figure 9)*				
	High Level	$V_{IH} = 5V$		0	0.040	mA
	Low Level	$V_{IL} = 0.8V$		−0.003	−0.8	mA
I_{15}	Reference Input Bias Current	*(Figure 3)*		−1	−3	μA
	Output Current Range	*(Figure 9)*				
		$V_{EE} = -5V$	0	2.0	2.1	mA
		$V_{EE} = -15V$, $T_A = 25°C$	0	2.0	4.2	mA
I_O	Output Current	$V_{REF} = 2.000V$. $R14 = 1000\Omega$				
		(Figure 9)	1.9	1.99	2.1	mA
	Output Current, All Bits Low	*(Figure 9)*		0	4	μA
	Output Voltage Compliance	$E_r \leq 0.19\%$, $T_A = 25°C$				
	$V_{EE} = -5V$				−0.55, +0.4	V
	V_{EE} Below −10V				−5.0 , +0.4	V
SRI_{REF}	Reference Current Siew Rate	*(Figure 14)*	4	8		mA/μs
	Output Current Power Supply Sensitivity	$-5V \leq V_{EE} \leq -16.5V$		0.05	2.7	μA/V
Power Supply Current (All Bits Low)		*(Figure 9)*				
I_S				2.3	22	mA
I_{EE}				−4.3	−13	
Power Supply Voltage Range		$T_A = 25°C$ *(Figure 9)*				
V_S			4.5	5.0	5.5	V
V_{EE}			−4.5	−15	−16.5	
	Power Dissipation					
	All Bits Low	$V_S = 5V. V_{EE} = -5V$		33	170	mW
		$V_S = 5V. V_{EE} = -15V$		106	305	mW
	All Bits High	$V_S = 15V. V_{EE} = -5V$		90		mW
		$V_S = 15V. V_{EE} = -15V$		160		mW

Note 1: All current switches are tested to guarantee at least 50% of rated current.
Note 2: All bits switched.
Note 3: Range control is not required.

Fig. 1 - Supply Current vs Temperature

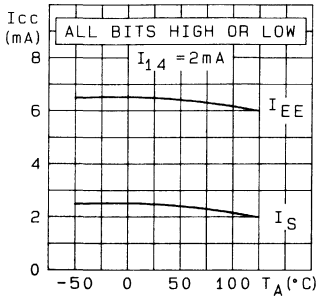


Fig. 2 - Supply Current vs Supply Voltage (V_{EE})

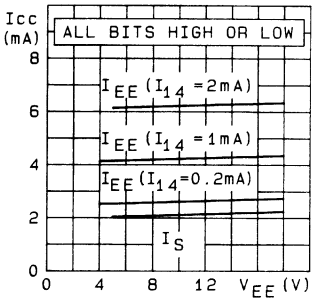


Fig. 3 - Supply Current vs Supply Voltage (V_S)

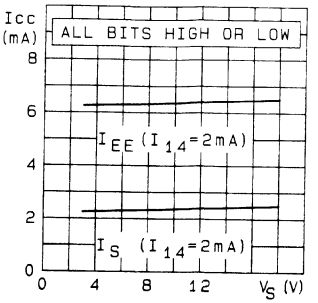


Fig. 4 - Logic Input Current vs Input Voltage

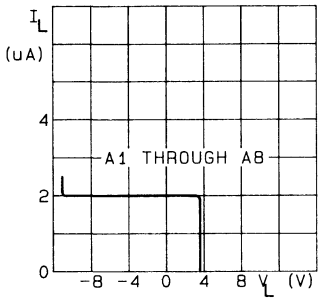


Fig. 5 - Bit Transfer Characteristics

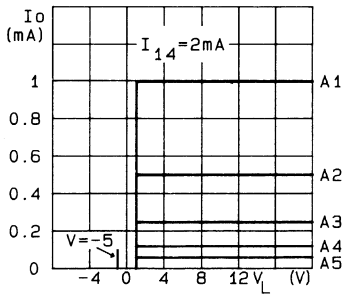


Fig. 6 - Output Voltage Compilance

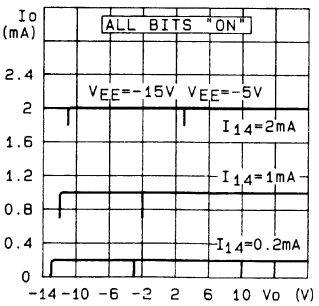


Fig. 7 - Output Voltage Compliance vs Temperature

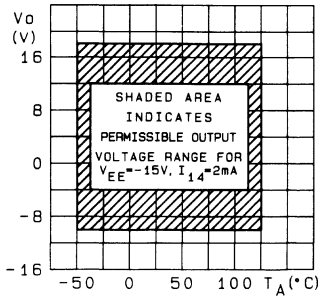
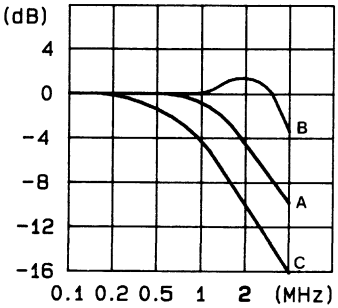


Fig. 8 - Frequency response



Unless otherwise specified: R14 = R15 = 1 kΩ, C = 15 pF, pin 16 to V_{EE}; R_L = 50Ω, pin 4 to ground.

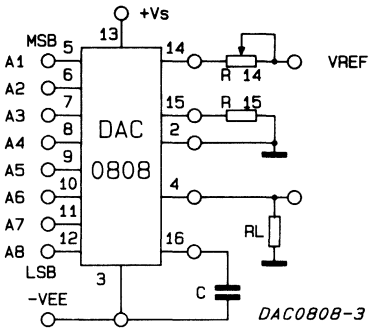
Curve A: Large Signal Bandwidth Method of *Figure 7*, V_{REF} = 2 Vp-p offset 1 V above ground

Curve B: Small Signal Bandwidth Method of *Figure 7*, R_L = 250Ω, V_{REF} = 50 mVp-p offset 200 mV above ground.

Curve C: Large and Small Signal Bandwidth Method of *Figure 9* (no op amp. R_L = 50Ω), R_S = 50Ω, V_{REF} = 2V, V_S = 100 mVp-p centered at 0V.

Test Circuits

FIGURE 9. Notation Definitions



The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K \left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256} \right)$$

where $K \cong \frac{V_{REF}}{R14}$

and A_N = "1" if A_N is at high level
A_N = "0" if A_N is at low level

FIGURE 10. Relative Accuracy

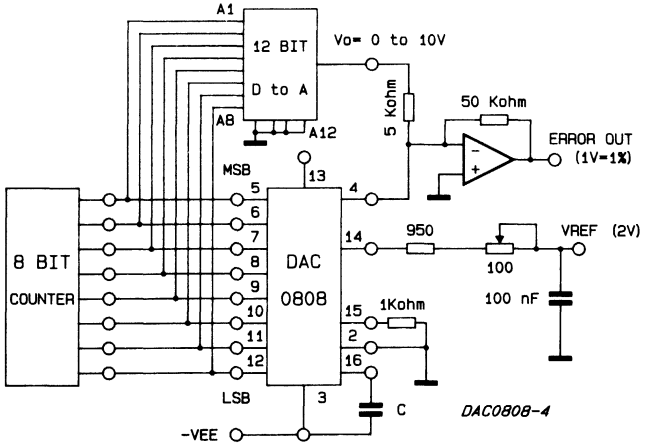
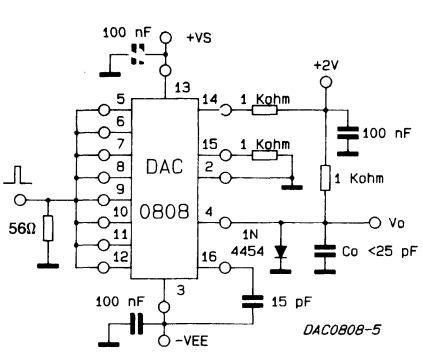


FIGURE 11. Transient Response and Settling Time



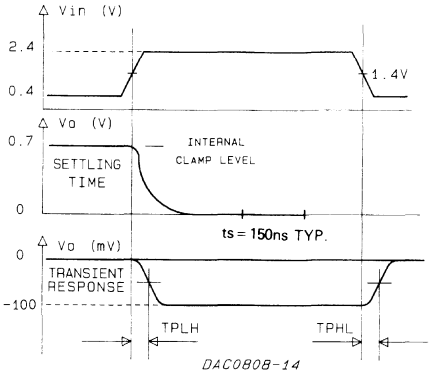
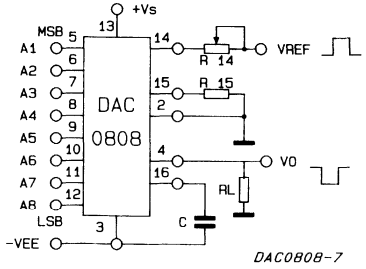


FIGURE 12. Positive V_{REF}

FIGURE 13. Negative V_{REF}



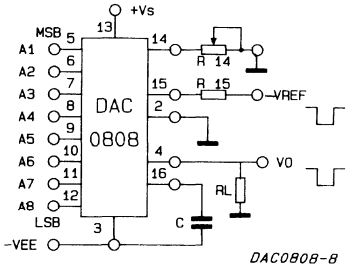
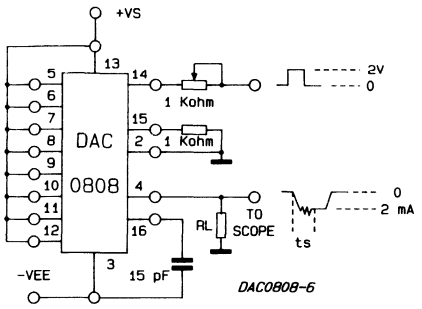


FIGURE 14. Reference Current Slew Rate Measurement



APPLICATION INFORMATION

CIRCUIT DESCRIPTION

The DAC0808 consists of a reference current amplifier, an R-2R ladder, and eight high-speed current switches. For many applications, only a reference resistor and reference voltage need be added.

The switches are noninverting in operation, therefore a high state on the input turns on the specified output current component. The switch uses current steering for high speed, and a termination amplifier consisting of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching and provides a low impedance termination of equal voltage for all legs of the ladder. The R-2R ladder divides the reference amplifier current into binarily-related components, which are fed to the switches. Nota that there is always a remainder current which is equal to the last significant bit. This current is shunted to ground, and the maximum output current is 255/256 of the reference amplifier current, or 1.992 mA for a 2.0 mA reference amplifier current if the NPN current source pair is perfectly matched.

REFERENCE AMPLIFIER DRIVE AND COMPENSATION

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I_{14}, must always flow into pin 14, regardless of the set-up method or reference voltage polarity.

Connections for a positive voltage are shown in *Figure 12*. The reference voltage source supplies the full current I_{14}. For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin; for R14 values of 1, 2.5 and 5 kΩ, minimum capacitor values are 15,37 and 75 pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection.

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown in *Figure 13*. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 3V above the V_{EE} supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at pin 15.

When a DC reference voltage is used, capacitive by pass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5V supply which drives logic is to be used as the reference, R14 should be decoupled by connecting it to 5V through another resistor and bypassing the junction of the 2 resistors with 0.1 μF to ground. For reference voltages greater than 5V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

OUTPUT VOLTAGE RANGE

The voltage on pin 4 is restricted to a range of -0.6 to 0.5V when $V_{EE} = -5V$ due to the current switching methods employed in the DAC0808.

The negative output voltage compliance of the DAC0808 is extended to $-5V$ where the negative supply voltage is more negative than $-10V$. Using a full-scale current of 1.992 mA and load resistor of 2.5 kΩ between pin 4 and ground will yield a voltage output of 256 levels between 0 and $-4.980V$. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500Ω do not significantly affect performance, but a 2.5 kΩ load increases worst-case setting time to 1.2 μs (when all bits are switched ON). Refer to the subsequent text section on Settling Time for more details output loading.

OUTPUT CURRENT RANGE

The output current maximum rating of 4.2 mA may be used only for negative supply voltages more negative than $-7V$, due to the increased voltage drop across the resistors in the reference current amplifier.

ACCURACY

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current. The relative accuracy of the DAC0808 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the DAC0808 has a very low full-scale current drift with temperature.

The DAC0808 series is guaranteed accurate to within ±1/2 LSB at a full-scale output current of 1.992 mA. This corresponds to a reference amplifier output current drive to the ladder network of 2 mA, with the loss of 1 LSB (8 μA) which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1 mA, allowing some mis-match in the NPN current source pair. The accuracy test circuit is shown in *Figure 10*. The 12-bit converter is calibrated for a full-scale output current of 1.992 mA. This is an optional step since the DAC0808 accuracy is essentially the same between 1.5 and 2.5 mA. Then the DAC0808 circuits' full-scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accuracy D-to-A converter. 16-bit accuracy implies a total error of ±1/2 of one part in 65,536, or ±0.00076%, which is much more accurate than the ±0.019% specification provided by the DAC0808.

MULTIPLYING ACCURACY

The DAC0808 may be used in the multiplying mode with 8-bit accuracy when the reference current is varied over a range of 256:1. If the reference current in the multiplying mode ranges from 16 μA to 4 mA, the additional error contributions are less than 1.6 μA. This is well within 8-bit accuracy when referred to full-scale.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the DAC0808 is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a DC reference current is 0.5 to 4 mA.

SETTLING TIME

The "worst case" switching condition occurs when all bits are switched "on", which corresponds to a low-high transition for all bits. This time is typically 150 ns for settling to within ±1/2 LSB for 8-bit accuracy and 100 ns to 1/2 LSB for 7 and 6-bit accuracy. The turn off is typically under 100 ns. These timers apply when $R_L \leq 500$ ohms and $C_0 \leq 25$ pF.

The test circuit of Figure 11 requires a smaller voltage swing for the current switches due to internal voltage clamping in the DAC0808 A 1.0-kilohm load resistor from pin 4 to ground gives a typical settling time of 200 ns. Thus, it is voltage swing and not the output RC time constant that determines setting time for most applications.
Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100 μF supply bypassing for low frequencies, and minimum scope lead length are all mondatory.

PROGRAMMABLE GAIN AMPLIFIER OR DIGITAL ATTEPUATOR

When used in the multiplying mode can be applied as a digital attenuator. See Figure 15. One advantage of this technique is that if $R_S = 50$ ohms, no compensation capacitor is needed. The small and large signal band are now identical and are shown in Figure 8C.

The best frequency response is obtained by not allowing I_{14} to reach zero. However, the high impedance node, pin 16, is clamped to prevent saturation and insure fast recovery when the current through R14 goes to zero. R_S can be set for a ± 1.0 mA variation in relation to I_{14}. I_{14} can never be negative. The output current is always unipolar. The quiescent dc output current level changes with the digital word which makes accoupling necessary.

CURRENT TO VOLTAGE CONVERSION

Voltage output of a larger magnitude are obtainable with the circuit of fig. 16 which uses an external operational amplifier as a current to voltage converter. This configuration automatically keeps the output of the DAC0808 ground potential and the operational amplifier can generate a positive voltage limited only by its positive supply voltage. Frequency response and setting time are primarily determined by the characteristics of the operational amplifier. In addition, the operational amplifier must be compensated for unity gain, and in some cases over compensation may be desirable.
Note that this configuration results in a positive output voltage only, the magnitude of which is dependent on the digital input. The LM301 can be used in a feedforwerd mode resulting in a full scale setting time on the order of 2.0 μs.

COMBINED OUTPUT AMPLIFIER AND VOLTAGE REFERENCE

For many of its applications the DAC0808 requires a reference voltage and an operational amplifier. Normally the operational amplifier is used as a current to voltage converter and its output need only go positive. With the popular LM723 voltage regulator both of these functions are provided in a single package with the added bonus of up to 150 mA output current. See Figure 17. The reference voltage is developed with respect to the negative voltage and appears as a common-mode signal to the reference amplifier in the D-to-A converter. This allows use of its amplifier as a classic current-to-voltage converter with the non-inverting input grounded.
Since ± 15V and $+5.0$V are normally available in a combination digital-to-analog system, only the -5.0 V need be developed. A resistor divider is sufficiently accurate since the allowable range on pin 5 is from -2.0 to -8.0 volts. The 5.0 kilohm pulldown resistor on the amplifier output is necessary for fast negative transitions.
Full scale output may be increasing R_O and raising the $+15$V supply voltage to 35 V maximum. The resistor divider should be altered to comply with the maximum limit of 40 volts across the LM723 C_O may be decreased to maintain the same R_OC_O product if maximum speed is desired.

PROGRAMMABLE POWER SUPPLY

The circuit of figure 17 can be used as a digitally programmed power supply by the addition of thumbwheel switches and a BCD-to-binary converter. The output voltage can be scaled in several ways, including 0 to $+25.5$ volts in 0.1 $-$ volt increments, ± 10 mV.

PANEL METER READOUT

The DAC0808 can be used to read out the status of BCD or binary registers or counters a digital control system. The current output can be used to drive directly an analog panel meter. External meter shunts may be necessary if a meter of less than 20 mA full scale is used. Full scale calibration can be done by adjusting R14 or V_{ref} (see fig. 18).

CHARACTER GENERATOR

In a character generation system fig. 19 one DAC0808 circuit uses a fixed reference voltage and its digital input defines the starting point for a stroke. The second converter circuit has a ramp input for the reference and its digital input defines the slope of the stroke. Note that this approach does not result in a 16-bit D-to-A converter (see Accuracy Section).

TWO-DIGIT BCD CONVERSION

Two 8-bit, D-to-A converters can be used to build a two digit BCD D-to-A or A-to-D converter (fig. 21). If both outputs feed the virtual ground of an operational amplifier, 10:1 current scaling can be achieved with a resistive current divider. If current output is desired, the units may be operated at full scale current levels of 4.0 mA and 0.4 mA with the outputs connected to sum the currents. The error of the D-to-A converter handling the least significant bits will be scaled down by a factor of ten and thus an DAC0806 may be used for the least significant word.

FIGURE 15. Programmable Gain Amplifier or Digital Attenuator Circuit

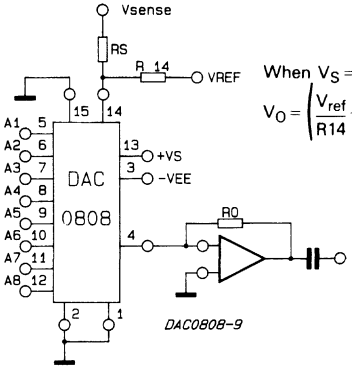


FIGURE 16.

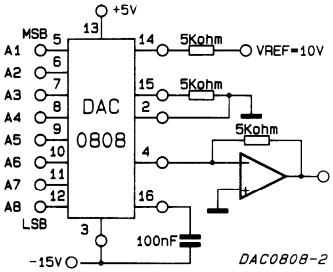


FIGURE 17. Combined output amplifier and voltage reference circuit

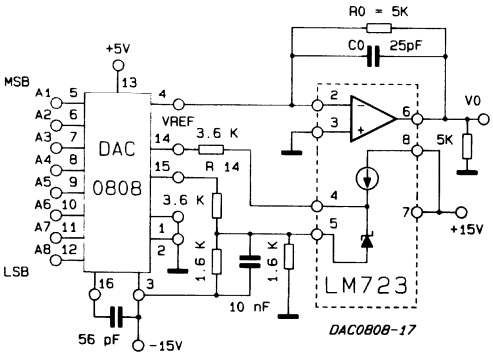


FIGURE 18. Panel meter readout circuit

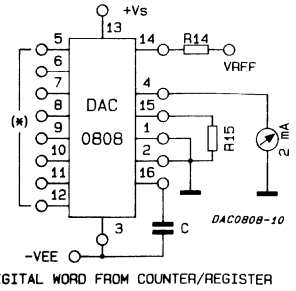
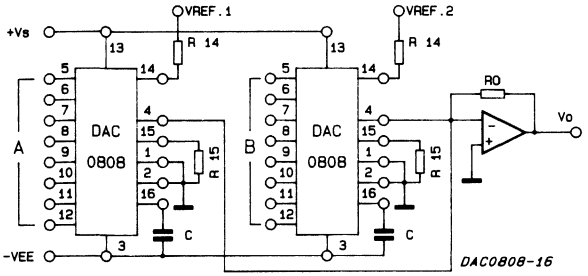


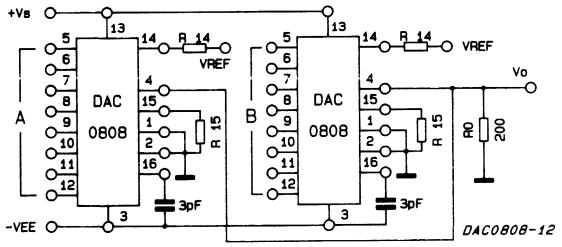
FIGURE 19. Digital summing and character generation



$$V_O = (I_{O1} + I_{O2})\, R_O$$

$$V_O = \left[\frac{V_{ref1}}{R14_1}\,\{A\} + \frac{V_{ref2}}{R14_2}\,\{B\}\right] R_O$$

FIGURE 20. Analog product of two digital words (High Speed Operation)



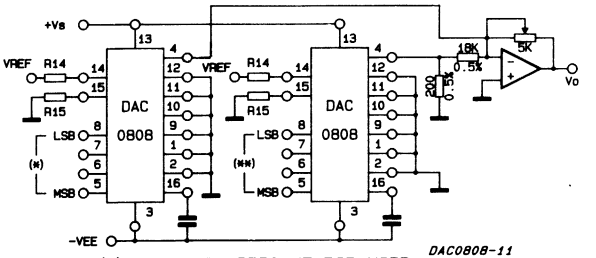
$$V_O = -I_{O1}\, R_O = \frac{V_{ref}}{R14_1}\,\{A\}\, R_O$$

$$I_{O2} = \frac{\{B\}\,|V_O|}{R14_2} - \frac{\{B\}}{R14_2}\left[R_O\left(\frac{V_{ref}}{R14_1}\right)\{A\}\right]$$

Since $R_O = R14_2$ and $K = \dfrac{V_{ref}}{R14_1}$

$$I_{O2} = K\,\{A\}\,\{B\}$$ K can be an analog variable

FIGURE 21. Two-digit BCD conversion



(*) MOST SIGNIFICANT BCD WORD
(**) LEAST SIGNIFICANT BCD WORD

L149

4A LINEAR DRIVER

- HIGH OUTPUT CURRENT (4A PEAK)
- HIGH CURRENT GAIN (10.000 TYP.)
- OPERATION UP TO ± 20V
- THERMAL PROTECTION
- SHORT CIRCUIT PROTECTION
- OPERATION WITHIN SOA
- HIGH SLEW-RATE (30V/μs)

The L149 is a general purpose power booster in Pentawatt® package consisting of a quasi-complementary darlington output stage with the associated biasing system and inhibit facility.

The device is particularly suited for use with an operational amplifier inside a closed loop configuration to increase output current.

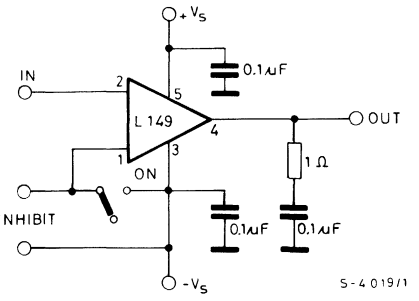
Pentawatt®

ORDERING NUMBER: L149V

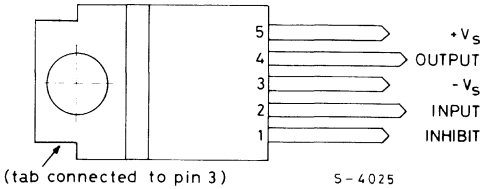
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 20	V
V_i	Input voltage	V_s	
$V_5 - V_4$	Upper power transistor V_{CE}	40	V
$V_4 - V_3$	Lower power transistor V_{CE}	40	V
I_o	DC output current	3	A
I_o	Peak output current (internally limited)	4	A
V_{INH}	Input inhibit voltage	$-V_s$ +5	V
		$-V_s$ -1.5	V
P_{tot}	Power dissipation at T_{case} = 75°C	25	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

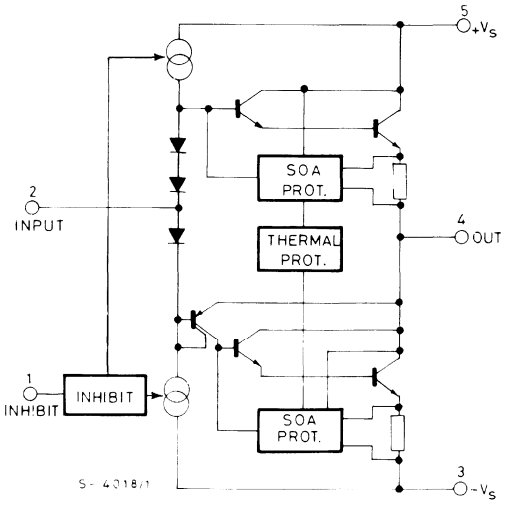
TEST CIRCUIT



CONNECTION DIAGRAM (top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (T_j = 25°C, V_s = ± 16V)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage				± 20	V
I_d	Quiescent drain current	V_s = ± 16V		30		mA
I_{in}	Input current	V_s = ± 16V V_i = 0V		200	400	μA
h_{FE}	DC current gain	V_s = ± 16V I_o = 3A	6000	10000		–
G_v	Voltage gain	V_s = ± 16V I_o = 1.5A		1		–
V_{CEsat}	Saturation voltage (for each transistor)	I_o = 3A			3.5	V
V_{os}	Input offset voltage	V_s = ± 16V			0.3	V
V_{INH}	Inhibit input voltage (pins 1-3)	ON condition			± 0.3	V
		OFF condition	± 1.8			
R_{INH}	Inhibit input resistance			2.0		KΩ
SR	Slew rate			30		V/μs
B	Power bandwidth	V_o = ± 10V, d = 1%, R_L = 8Ω		200		KHz

APPLICATION INFORMATION

Fig. 1 - High slew-rate power operational amplifier (SR = 13V/μs)

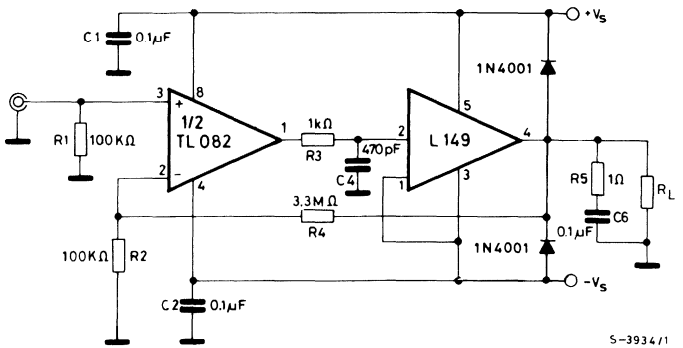


Fig. 2 - Maximum saturation voltage vs. output current

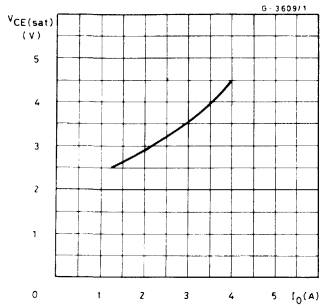


Fig. 3 - Current limiting characteristics

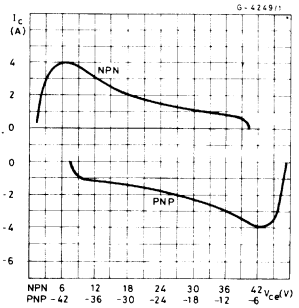


Fig. 4 - Supply voltage rejection vs. frequency

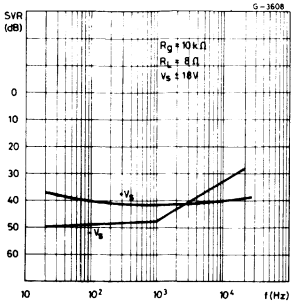


Fig. 5 - Distortion vs. output power (f = 1 KHz)

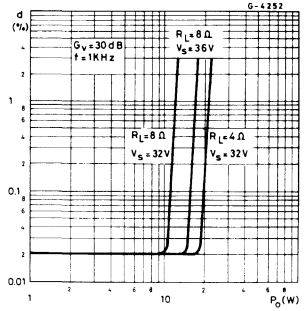


Fig. 6 - Distortion vs. output power (f= 10 KHz)

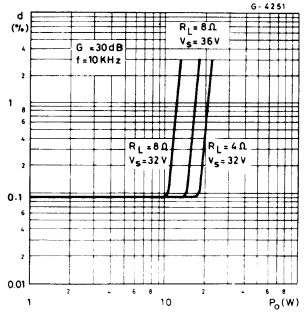


Fig. 7 - Output power vs. supply voltage

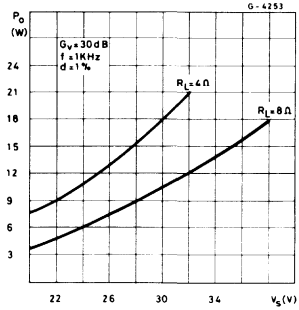
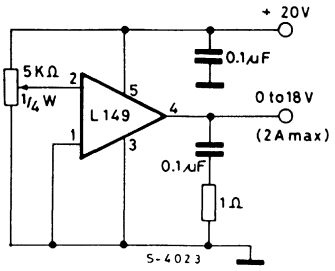


Fig. 8 - Electronic potentiometer (short-circuit protected)

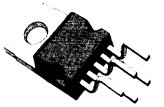


L165

3A POWER OPERATIONAL AMPLIFIER

- OUTPUT CURRENT UP TO 3A
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGES
- SOA PROTECTION
- THERMAL PROTECTION
- ± 18V SUPPLY

The L165 is a monolithic integrated circuit in Pentawatt® package, intended for use as power operational amplifier in a wide range of applications, including servo amplifiers and power supplies. The high gain and high output power capability provide superior performance wherever an operational amplifier/power booster combination is required.



Pentawatt®

ORDERING NUMBER: L165V

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 18	V
$V_5 - V_4$	Upper power transistor V_{CE}	36	V
$V_4 - V_3$	Lower power transistor V_{CE}	36	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	± 15	V
I_o	Peak output current (internally limited)	3.5	A
P_{tot}	Power dissipation at $T_{case} = 90°C$	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

APPLICATION CIRCUITS

Fig. 1 - Gain > 10

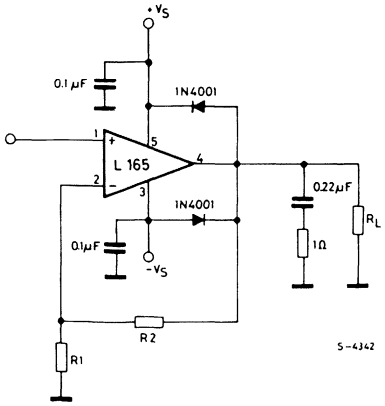
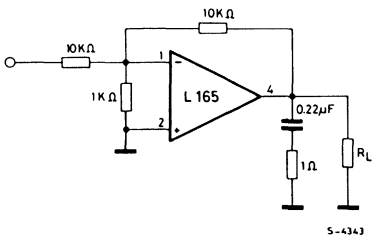
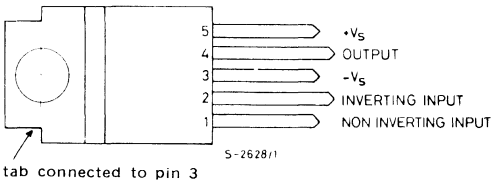


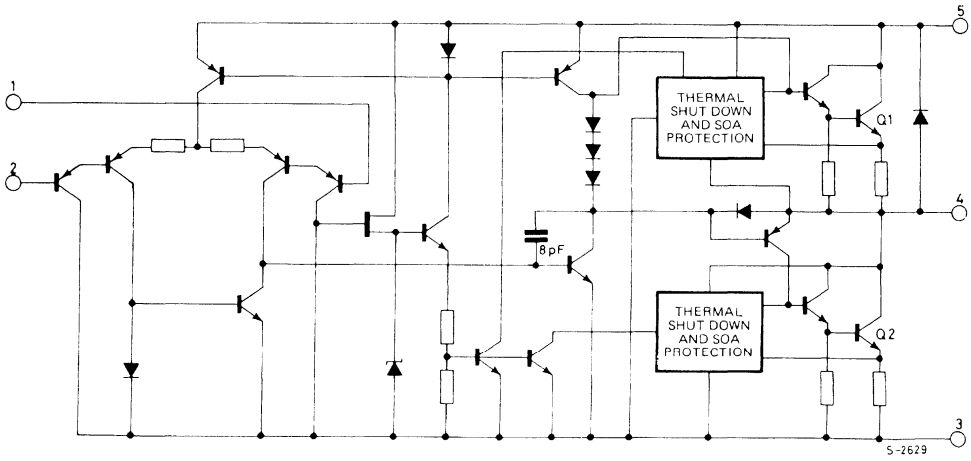
Fig. 2 - Unity gain configuration



CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (V_s = ± 15V, T_j = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		± 6		±18	V
I_d	Quiescent drain current	V_s = ± 18V		40	60	mA
I_b	Input bias current			0.2	1	μA
V_{os}	Input offset voltage			± 2	±10	mV
I_{os}	Input offset current			±20	±200	nA
SR	Slew-Rate	G_v= 10		8		V/μs
		G_v= 1 (°)		6		
V_o	Output voltage swing	f = 1 kHz I_p = 0.3A		27		V_{pp}
		f = 1 kHz I_p = 3A		24		V_{pp}
		f = 10 kHz I_p = 0.3A		27		V_{pp}
		f = 10 kHz I_p = 3A		23		V_{pp}
R_i	Input resistance (pin 1)	f = 1 KHz	100	500		KΩ
G_v	Voltage gain (open loop)			80		dB
e_N	Input noise voltage	B = 10 to 10 000 Hz		2		μV
i_N	Input noise current			100		pA
CMR	Common mode rejection	$R_g \leqslant$ 10 KΩ G_v= 30 dB		70		dB
SVR	Supply voltage rejection	R_g= 22 kΩ G_v = 10 V_{ripple}= 0.5 V_{rms} f_{ripple}= 100 Hz		60		dB
		R_g= 22 kΩ G_v = 100 V_{ripple}= 0.5 V_{rms} f_{ripple}= 100 Hz		40		dB
η	Efficiency	f = 1 kHz I_p = 1.6A; P_o = 5W R_L= 4Ω		70		%
		f = 1 kHz I_p = 3A; P_o = 18W R_L= 4Ω		60		%
T_{sd}	Thermal shut-down case temperature	P_{tot}= 12W		110		°C
		P_{tot}= 6W		130		°C

(°) Circuit of fig. 2

Fig. 3 - Open loop frequency response

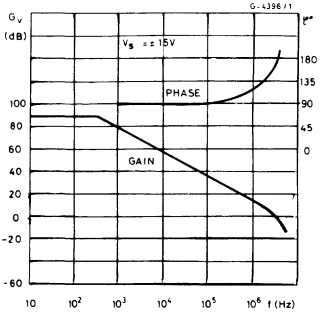


Fig. 4 - Closed-loop frequency response (circuit of fig. 2)

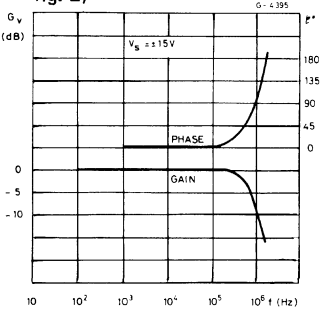


Fig. 5 - Large signal frequency response

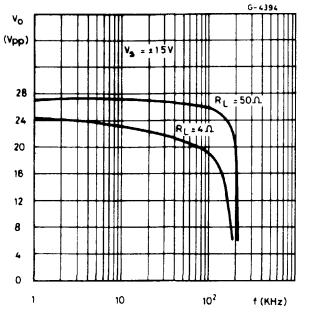


Fig. 6 - Maximum output current vs. voltage [V_{CE}] across each output transistor

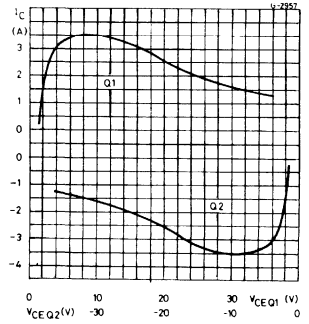


Fig. 7 - Safe operating area and collector characteristics of the protected power transistor

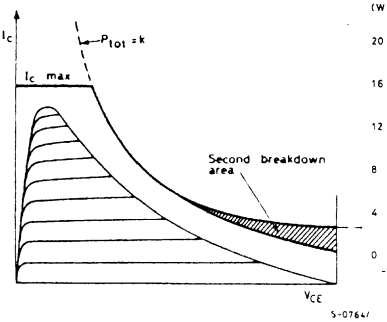


Fig. 8 - Maximum allowable power dissipation vs. ambient temperature

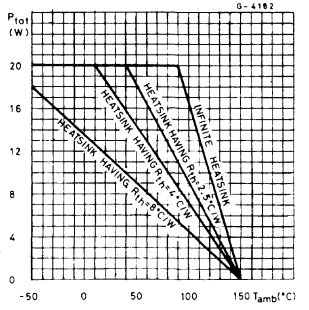
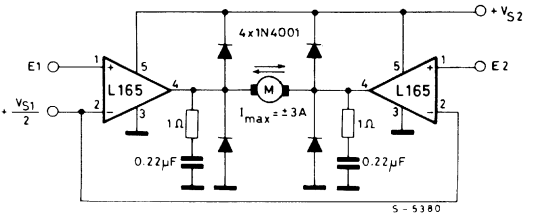


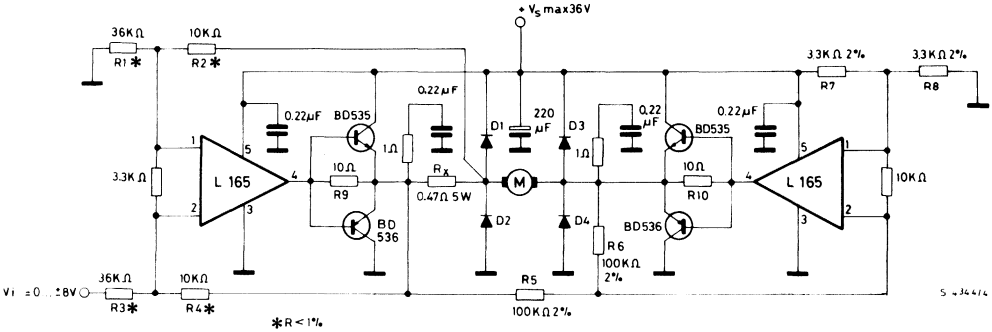
Fig. 9 - Bidirectional DC motor control with TTL/CMOS/μP compatible inputs



Must be $V_{S2} \geqslant V_{S1}$

E1, E2 = logic inputs
V_{S1} = logic supply voltage

Fig. 10 - Motor current control circuit with external power transistors ($I_{motor} > 3.5A$)

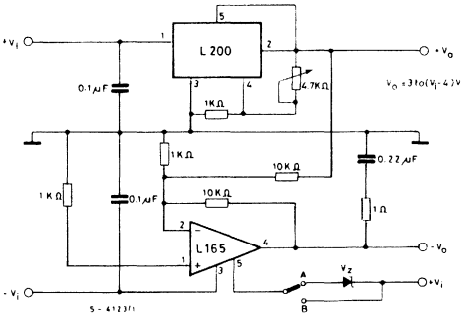


D1 to D4 : $\begin{cases} V_F \leqslant 1.2V \text{ @ } I = 4A \\ trr \leqslant 500 \text{ ns} \end{cases}$

Note: The input voltage level is compatible with L291 (5-BIT D/A converter).

The transfer function is : $\frac{I_M}{V_i} = \frac{R4}{Rx \ R3}$

Fig. 11 - High current tracking regulator

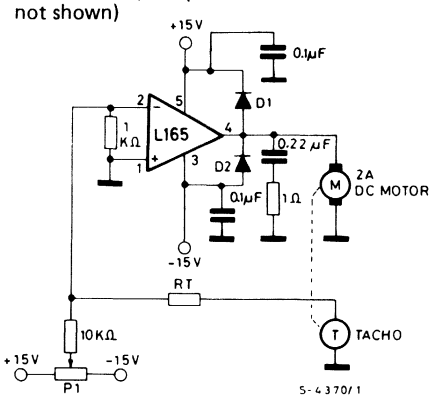


A: for ± 18 ⩽ V_i ⩽ ± 32

Note – V_Z must be chosen in order to verify
$2 V_i - V_Z \leqslant 36V$

B: for $V_i \leqslant \pm 18V$

Fig. 12 - Bidirectional speed control of DC motor (Compensation networks not shown)



D1, D2 : $\begin{cases} V_F \leqslant 1.2V \text{ @ } I = 2A \\ trr \leqslant 500 \text{ ns} \end{cases}$

Fig. 13 - Split power supply

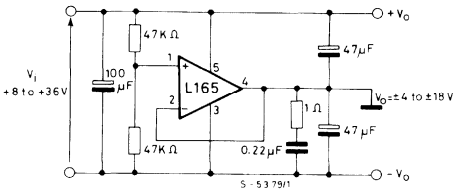
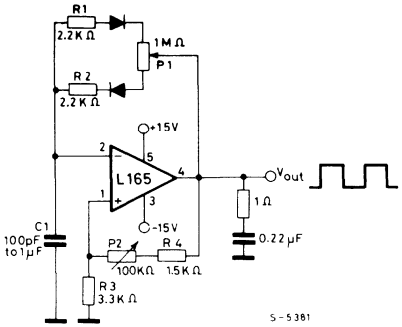


Fig. 14 - Power squarewave oscillator with independent adjustments for frequency and duty-cycle.



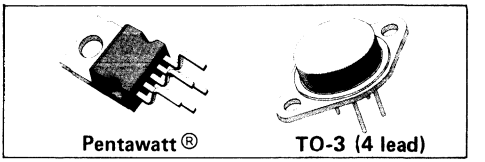
P1 : duty-cycle adjust
P2 : frequency adjust (f = 700 Hz with C1= 10 nF, P2= 100 KΩ, f=25 Hz with C1= 10 nF, P2= 0)

L200

ADJUSTABLE VOLTAGE AND CURRENT REGULATOR

- ADJUSTABLE OUTPUT CURRENT UP TO 2A (GUARANTEED UP TO $T_j = 150°C$)
- ADJUSTABLE OUTPUT VOLTAGE DOWN TO 2.85V
- INPUT OVERVOLTAGE PROTECTION (UP TO 60V, 10ms)
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR S.O.A. PROTECTION
- THERMAL OVERLOAD PROTECTION
- LOW BIAS CURRENT ON REGULATION PIN
- LOW STANDBY CURRENT DRAIN

The L200 is a monolithic integrated circuit for voltage and current programmable regulation. It is available in Pentawatt® package or 4-lead TO-3 metal case. Current limiting, power limiting, thermal shutdown and input overvoltage protection (up to 60V) make the L200 virtually blow-out proof. The L200 can be used to replace fixed voltage regulators when high output voltage precision is required and eliminates the need to stock a range of fixed voltage regulators.



ABSOLUTE MAXIMUM RATINGS

V_i	DC input voltage	40	V
V_i	Peak input voltage (10 ms)	60	V
ΔV_{i-o}	Dropout voltage	32	V
I_o	Output current	internally limited	
P_{tot}	Power dissipation	internally limited	
T_{stg}	Storage temperature	-55 to 150	°C
T_{op}	Operating junction temperature for L200C	-25 to 150	°C
	for L200	-55 to 150	°C

APPLICATION CIRCUITS

Fig. 1 - Programmable voltage regulator with current limiting

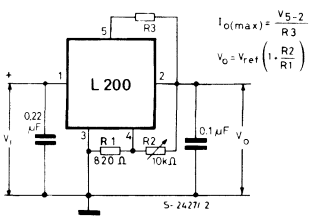
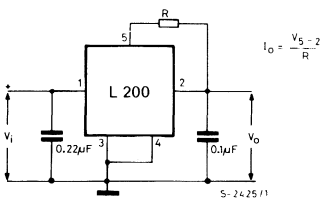
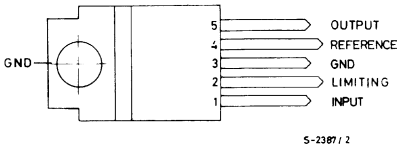
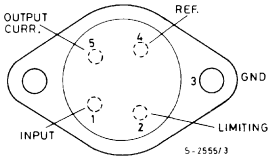


Fig. 2 - Programmable current regulator



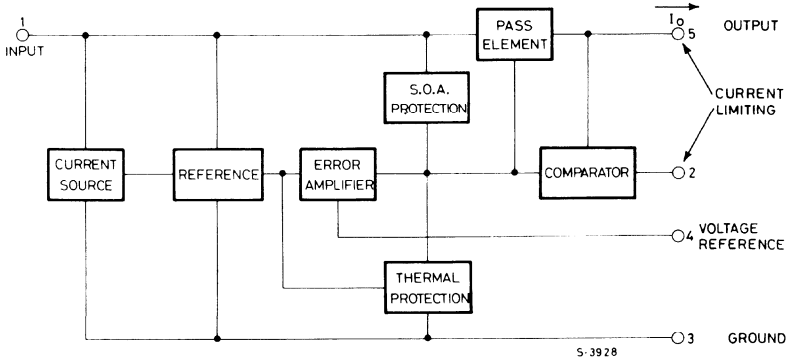
CONNECTION DIAGRAMS AND ORDERING NUMBERS
(top views)



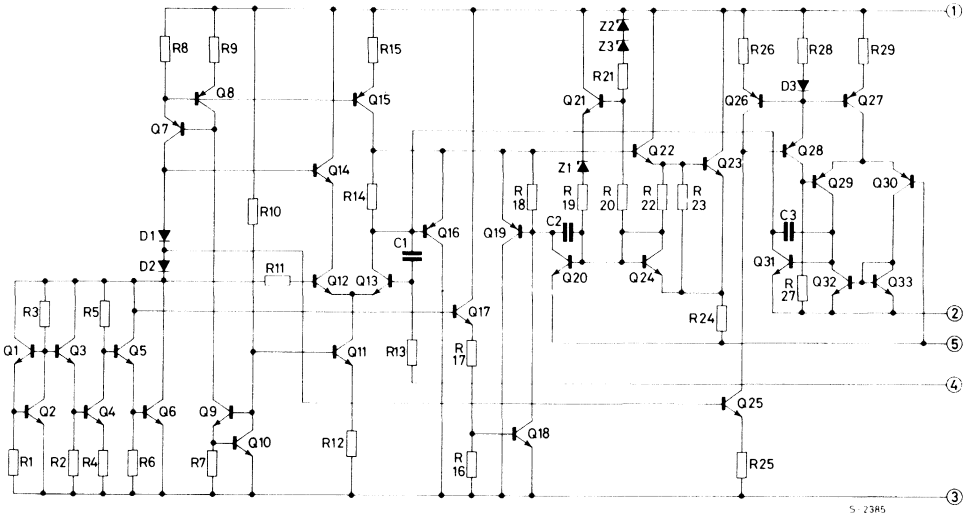


Type	Pentawatt®	TO-3
L 200		L 200 T
L 200 C	L 200 CH L 200 CV	L 200 CT

BLOCK DIAGRAM



SCHEMATIC DIAGRAM



THERMAL DATA

			TO-3	Pentawatt®
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4 °C/W	3 °C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	35 °C/W	50 °C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
VOLTAGE REGULATION LOOP						
I_d	Quiescent drain current (pin 3)	V_i = 20V		4.2	9.2	mA
e_N	Output noise voltage	$V_o = V_{ref}$ I_o = 10 mA B = 1 MHz		80		μV
V_o	Output voltage range	I_o = 10 mA	2.85		36	V
$\frac{\Delta V_o}{V_o}$	Voltage load regulation (note 1)	ΔI_o = 2A ΔI_o = 1.5A		0.15 0.1	1 0.9	% %
$\frac{\Delta V_i}{\Delta V_o}$	Line regulation	V_o = 5V V_i = 8 to 18V	48	60		dB
SVR	Supply voltage rejection	V_o = 5V I_o = 500 mA ΔV_i = 10 V_{pp} f = 100 Hz (note 2)	48	60		dB

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
ΔV_{i-o}	Droupout voltage between pins 1 and 5	I_o = 1.5A $\Delta V_o \leqslant 2\%$		2	2.5	V
V_{ref}	Reference voltage (pin 4)	V_i = 20V I_o = 10 mA	2.64	2.77	2.86	V
ΔV_{ref}	Average temperature coefficient of reference voltage	V_i = 20V I_o = 10 mA for T_j= -25 to 125°C for T_j= 125 to 150°C		-0.25 -1.5		mV/°C mV/°C
I_4	Bias current at pin 4			3	10	μA
$\frac{\Delta I_4}{\Delta T \cdot I_4}$	Average temperature coefficient (pin 4)			-0.5		%/°C
Z_o	Output impedance	V_i = 10V V_o= V_{ref} I_o= 0.5A f = 100 Hz		1.5		mΩ

CURRENT REGULATION LOOP

V_{SC}	Current limit sense voltage between pins 5 and 2	V_i = 10V V_o = V_{ref} I_5= 100 mA	0.38	0.45	0.52	V
$\frac{\Delta V_{sc}}{\Delta T \cdot V_{sc}}$	Average temperature coefficient of V_{SC}			0.03		%/°C
$\frac{\Delta I_o}{I_o}$	Current load regulation	V_i = 10V ΔV_o= 3V I_o = 0.5A I_o = 1A I_o = 1.5A		1.4 1 0.9		% % %
I_{sc}	Peak short circuit current	V_i - V_o = 14V (pins 2 and 5 short circuited)			3.6	A

Note 1): A load step of 2A can be applied provided that input-output differential voltage is lower than 20V (see fig. 3).

Note 2): The same performance can be maintained at higher output levels if a bypassing capacitor is provided between pins 2 and 4.

Fig. 3 - Typical safe operating area protection

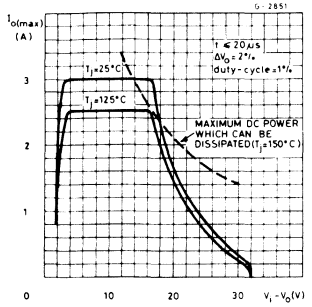


Fig. 4 - Quiescent current vs. supply voltage

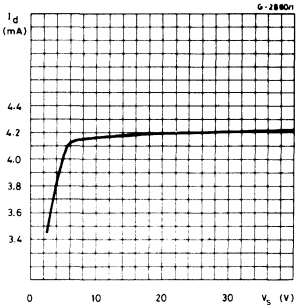


Fig. 5 - Quiescent current vs. junction temperature

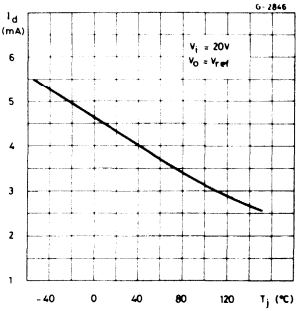


Fig. 6 - Quiescent current vs. output current

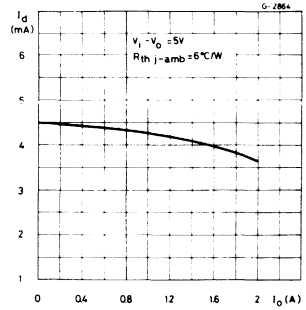


Fig. 7 - Output noise voltage vs. output voltage

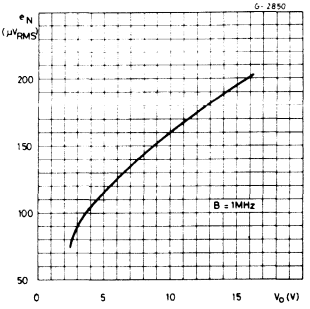


Fig. 8 - Output noise voltage vs. frequency

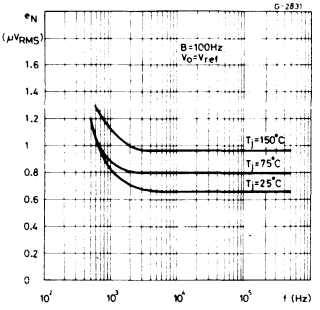


Fig. 9 - Reference voltage vs. junction temperature

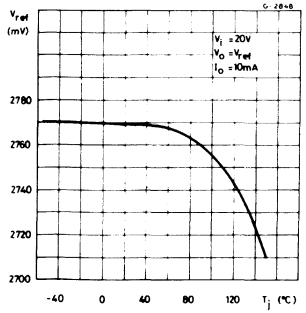


Fig. 10 - Voltage load regulation vs. junction temperature

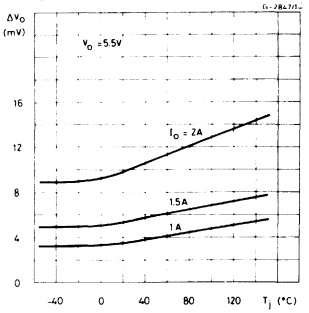


Fig. 11 - Supply voltage rejection vs. frequency

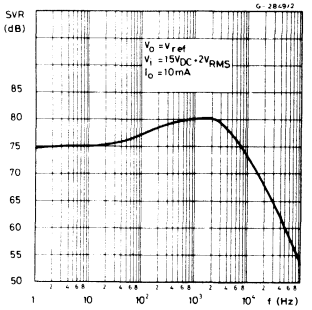


Fig. 12 - Dropout voltage vs. junction temperature

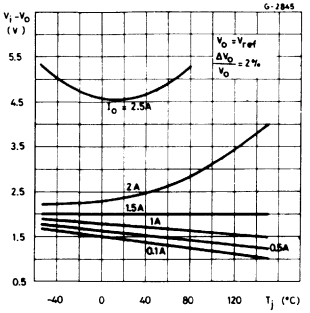


Fig. 13 - Output impedance vs. frequency

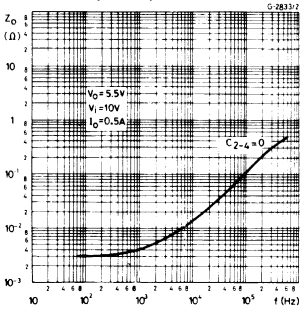


Fig. 14 - Output impedance vs. output current

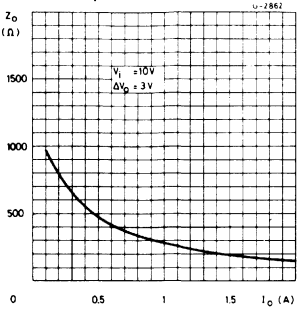


Fig. 15 - Voltage transient response

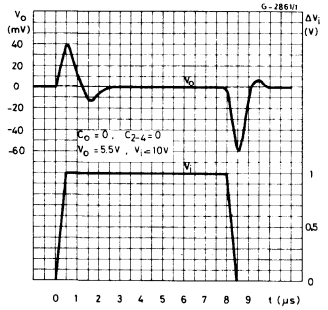


Fig. 16 - Load transient response

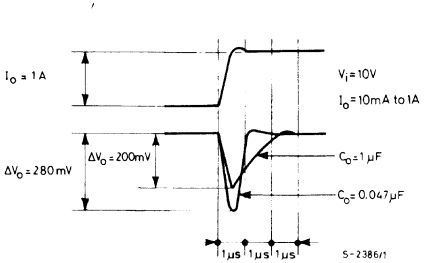


Fig. 17 - Load transient response

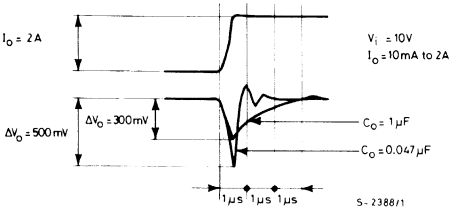
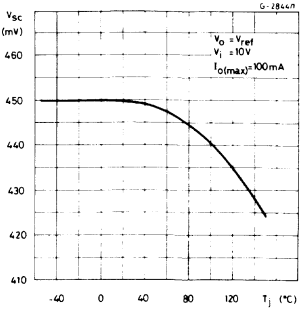


Fig. 18 - Current limit sense voltage vs. junction temperature



APPLICATION CIRCUITS

Fig. 19 - Programmable voltage regulator

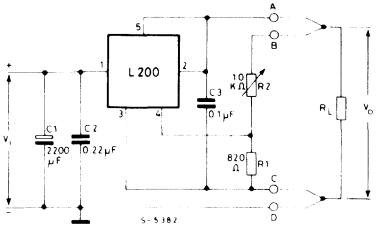


Fig. 20 - P.C. board and components layout of fig. 19. (1 : 1 scale)

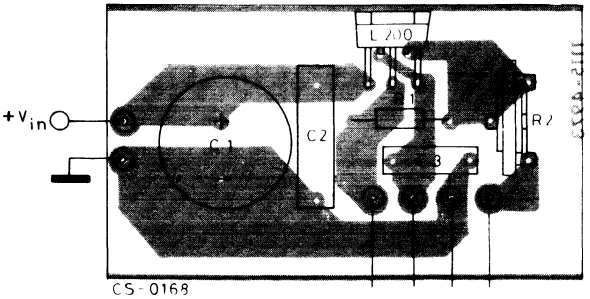


Fig. 21 - High current voltage regulator with short circuit protection

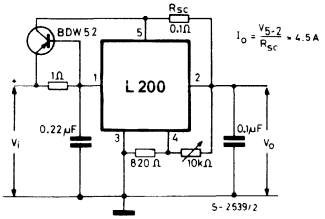


Fig. 22 - Digitally selected regulator with inhibit

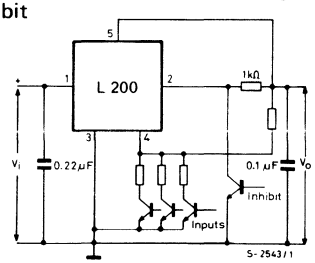
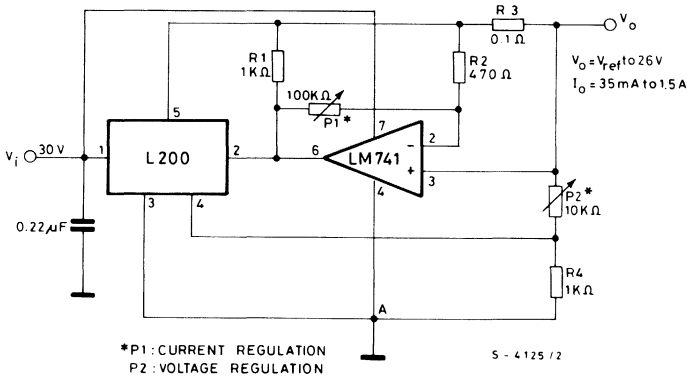


Fig. 23 - Programmable voltage and current regulator



Note: Connecting point A to a negative voltage (for example -3V/10 mA) it is possible to extend the output voltage range down to 0V and to obtain the current limiting down to this level (output short-circuit condition).

APPLICATION CIRCUITS

Fig. 24 - High current regulator with NPN pass transistor

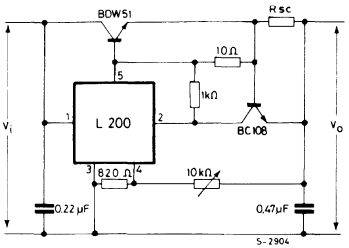
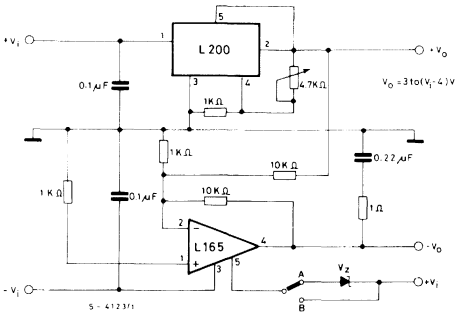


Fig. 25 - High current tracking regulator



A: for $\pm 18 \leqslant V_i \leqslant \pm 32$

Note – V_Z must be chosen in order to verify $2V_i - V_Z \leqslant 36V$

B: for $V_i \leqslant \pm 18V$

Fig. 26 - High input and output voltage

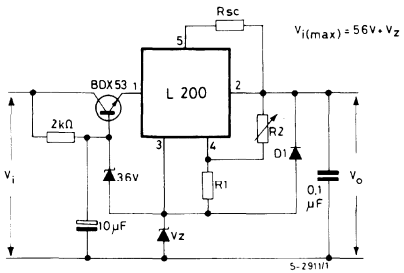
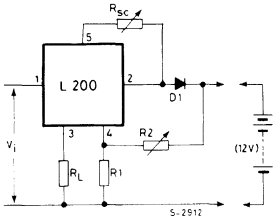


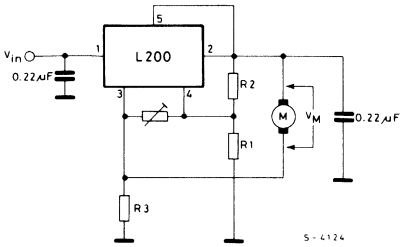
Fig. 27 - Constant current battery charger



The resistors R_1 and R_2 determine the final charging voltage and R_{sc} the initial charging current. D_1 prevents discharge of the battery throught the regulator.
The resistor R_L limits the reverse currents through the regulator (which should be 100 mA max) when the battery is accidentally reverse connected. If R_L is in series with a bulb of 12V/50 mA rating this will indicate incorrect connection.

APPLICATION CIRCUITS (continued)

Fig. 28 - 30W Motor speed control



$$R_3 = \frac{R_1}{R_2} \cdot R_M$$

$$V_M = V_{ref} \cdot (1 + \frac{R_2}{R_1})$$

Fig. 29 - Low turn on

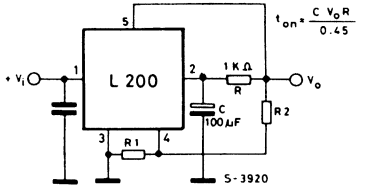
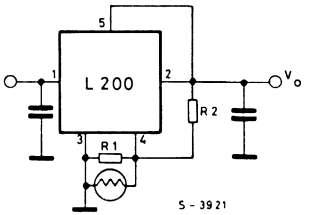


Fig. 30 - Light controller



L272
L272M

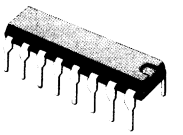
PRELIMINARY DATA

DUAL POWER OPERATIONAL AMPLIFIERS

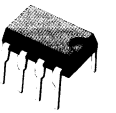
- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN

The L272 and L272M are monolithic integrated circuits in powerdip and minidip packages intended for use as power operational amplifiers in a wide range of applications including servo amplifiers and power supplies, compact disc, VCR, etc.

The high gain and high output power capability provide superior performance whatever an operational amplifier/power booster combination is required.



Powerdip (8 + 8)



Minidip Plastic

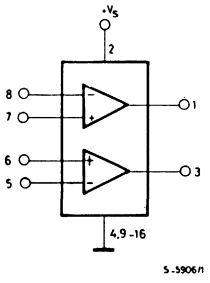
ORDERING NUMBERS:

L272 L272M

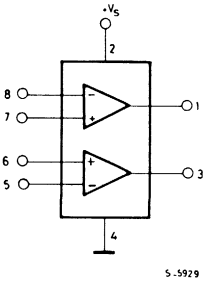
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	28	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	$\pm V_s$	
I_o	DC output current	1	A
I_p	Peak output current (non repetitive)	1.5	A
P_{tot}	Power dissipation at $T_{amb} = 80°C$ **(L272)**, $T_{amb} = 50°C$ **(L272M)**	1	W
	$T_{case} = 75°C$ **(L272)**	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

BLOCK DIAGRAM



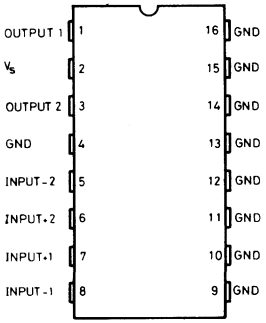
L272



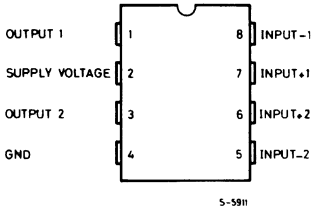
L272M

L272
L272M

CONNECTION DIAGRAM
(Top view)

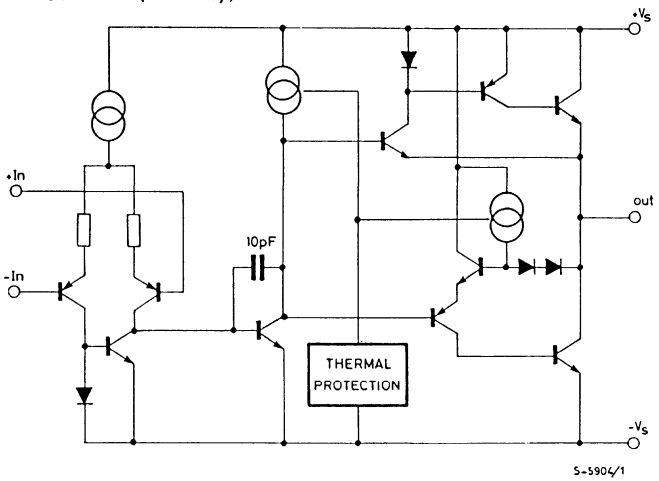


L272



L272M

SCHEMATIC DIAGRAM (one only)



THERMAL DATA

			Powerdip	Minidip
$R_{th\ j\text{-}case}$	Thermal resistance junction-pins	max	15°C/W	*70°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70°C/W	100°C/W

* Thermal resistance junction-pin 4

ELECTRICAL CHARACTERISTICS (V_s = 24V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			4		28	V
I_s	Quiescent drain current	$V_o = \frac{V_s}{2}$	V_s = 24V		8	12	mA
			V_s = 12V		7.5	11	mA
I_b	Input bias current				0.3	2.5	μA
V_{os}	Input offset voltage				15	60	mV
I_{os}	Input offset current				50	250	mA
SR	Slew rate				1		V/μs
B	Gain-bandwidth product				350		KHz
R_I	Input resistance			500			KΩ
G_v	O.L. voltage gain	f = 100Hz		60	70		dB
		f = 1KHz			50		dB
e_N	Input noise voltage	B = 20KHz			10		μV
I_N	Input noise current	B = 20KHz			200		pA
CRR	Common Mode rejection	f = 1KHz		60	75		dB
SVR	Supply voltage rejection	f = 100Hz R_G = 10KΩ V_R = 0.5V	V_s = 24V V_s = ±12V V_s = ± 6V	54	70 62 56		dB dB dB
V_o	Output voltage swing		I_p = 0.1A I_p = 0.5A	21	23 22.5		V V
C_s	Channel separation	f = 1KHz; R_L = 10Ω; G_v = 30dB	V_s = 24V V_s = ± 6V		60 60		dB dB
d	Distortion	f = 1KHz V_s = 24V	G_v = 30dB R_L = ∞		0.5		%
T_{sd}	Thermal shutdown junction temperature				145		°C

Fig. 1 - Quiescent current vs. supply voltage

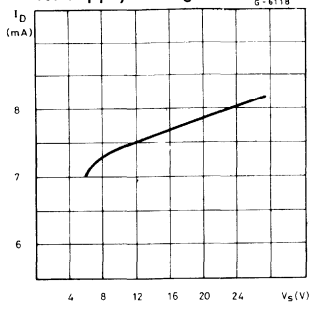


Fig. 2 - Quiescent drain current vs. temperature

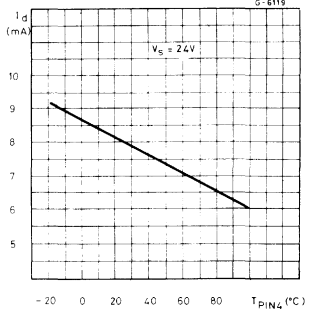


Fig. 3 - Open loop voltage gain

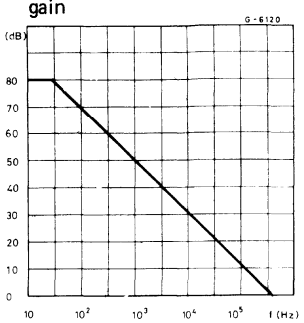


Fig. 4 - Output voltage swing vs. load current

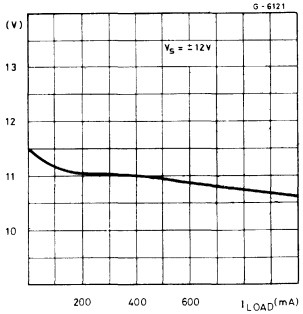


Fig. 5 - Output voltage swing vs. load current

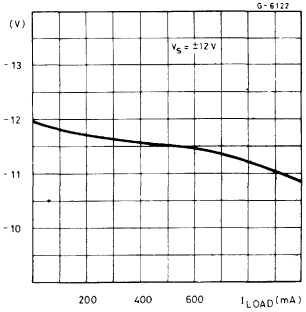


Fig. 6 - Supply voltage rejection vs. frequency

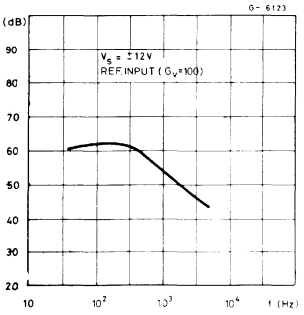


Fig. 7 - Channel separation vs. frequency

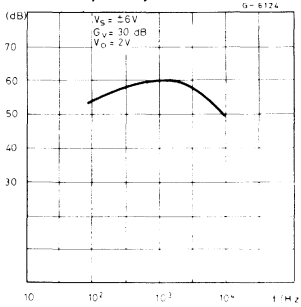
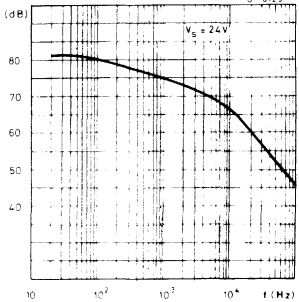


Fig. 8 - Common mode rejection vs. frequency



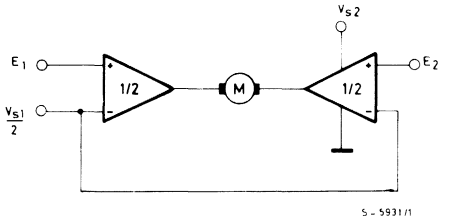
APPLICATION SUGGESTION

NOTE

In order to avoid possible instability occurring into final stage the usual suggestions for the linear power stages are useful, as for instance:

- layout accuracy;
- A 100nF capacitor corrected between supply pins and ground;
- boucherot cell (0.1 to 0.2μF + 1Ω series) between outputs and ground or across the load.

Fig. 9 - Bidirectional DC motor control with μP compatible inputs



V_{S1} = logic supply voltage

Must be $V_{S2} > V_{S1}$

E1, E2 = logic inputs

Fig. 10 - Servocontrol for compact-disc

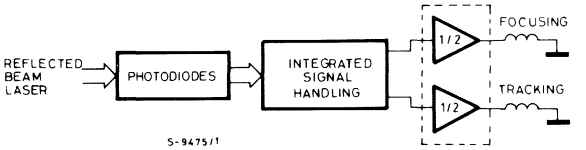


Fig. 11 - Capstan motor control in video recorders

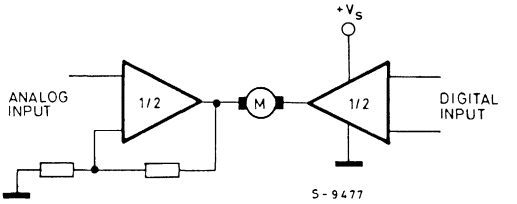
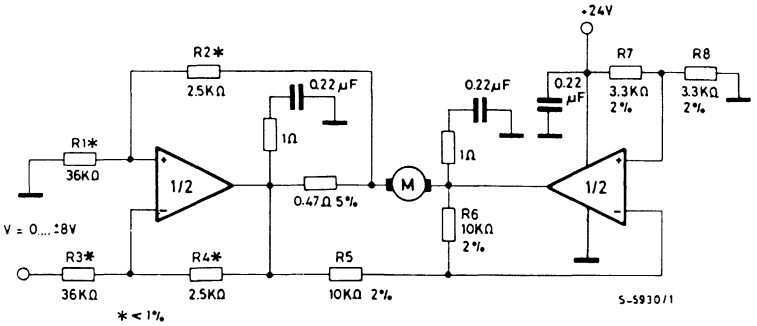


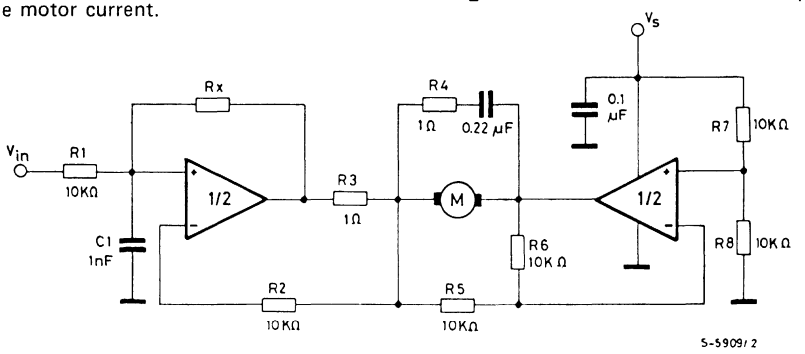
Fig. 12 - Motor current control circuit



Note: The input voltage level is compatible with L291 (5-BIT D/A converter)

Fig. 13 - Bidirectional speed control of DC motors.

For circuit stability ensure that $R_X > \frac{2R3 \circ R1}{R_M}$ where R_M = internal resistance of motor. The voltage available at the terminals of the motor is $V_M = 2 (V_i - \frac{V_s}{2}) + |R_o|. I_M$ where $|R_o| = \frac{2R \circ R1}{R_X}$ and I_M is the motor current.



L296
L296P

PRELIMINARY DATA

HIGH CURRENT SWITCHING REGULATORS

- 4A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- 0 TO 100% DUTY CYCLE RANGE
- PRECISE (±2%) ON-CHIP REFERENCE
- SWITCHING FREQUENCY UP TO 200KHz
- VERY HIGH EFFICIENCY (UP TO 90%)
- VERY FEW EXTERNAL COMPONENTS
- SOFT START
- RESET OUTPUT
- EXTERNAL PROGRAMMABLE LIMITING CURRENT (L296P)
- CONTROL CIRCUIT FOR CROWBAR SCR
- INPUT FOR REMOTE INHIBIT AND SYNCHRONUS PWM
- THERMAL SHUTDOWN.

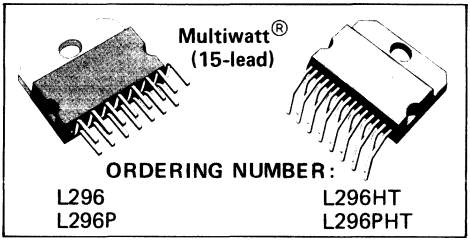
The L296 and L296P are stepdown power switching regulators delivering 4A at a voltage variable from 5.1V to 40V.

Features of the devices include soft start, remote inhibit, thermal protection, a reset output for microprocessors and a PWM comparator input for synchronization in multichip configurations.

The L296P includes external programmable limiting current.

The L296 and L296P are mounted in a 15-lead Multiwatt® plastic power package and requires very few external components.

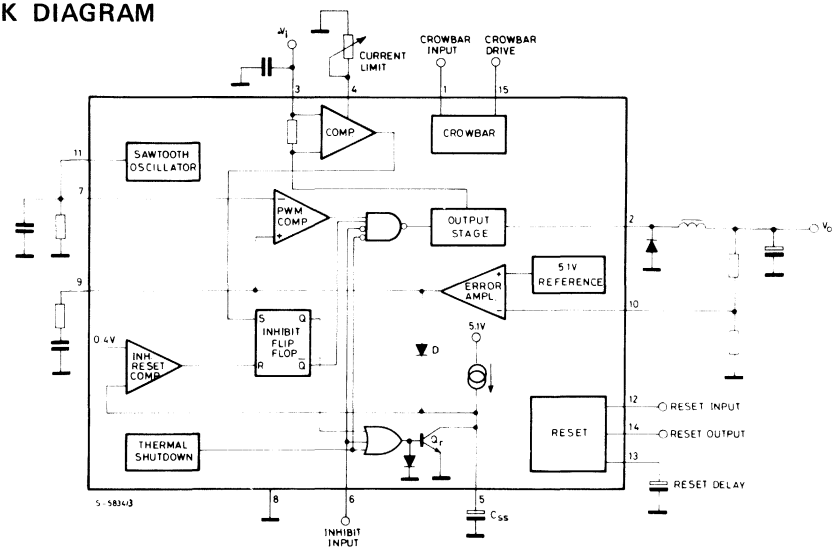
Efficient operation at switching frequencies up to 200KHz allows a reduction in the size and cost of external filter components. A voltage sense input and SCR drive output are provided for optional crowbar overvoltage protection with an external SCR.



ORDERING NUMBER:

L296	L296HT
L296P	L296PHT

BLOCK DIAGRAM



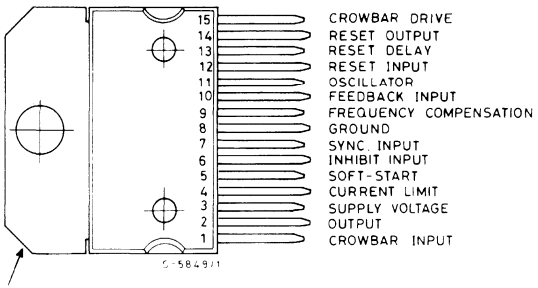
ABSOLUTE MAXIMUM RATINGS

V_i	Input voltage (pin 3)	50	V
$V_i - V_2$	Input to output voltage difference	50	V
V_2	Output DC voltage	-1	V
	Output peak voltage at t = 0.1 μsec f = 200 kHz	-7	V
V_1, V_{12}	Voltage at pins 1, 12	10	V
V_{15}	Voltage at pin 15	15	V
V_4, V_5, V_7, V_9, V_{13}	Voltage at pins 4, 5, 7, 9 and 13	5.5	V
V_{10}, V_6	Voltage at pins 10 and 6	7	V
V_{14}	Voltage at pin 14 ($I_{14} \leqslant 1$ mA)	V_i	
I_9	Pin 9 sink current	1	mA
I_{11}	Pin 11 source current	20	mA
I_{14}	Pin 14 sink current ($V_{14} < 5V$)	50	mA
P_{tot}	Power dissipation at $T_{case} \leqslant 90$ °C	20	W
T_j, T_{stg}	Junction and storage temperature	-40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	35	°C/W

CONNECTION DIAGRAM
(top view)



Tab connected to pin 8

PIN FUNCTIONS

N°	NAME	FUNCTION
1	CROWBAR INPUT	Voltage sense input for crowbar overvoltage protection. Normally connected to the feedback input thus triggering the SCR when V_{out} exceeds nominal by 20%. May also monitor the input and a voltage divider can be added to increase the threshold. Connected to ground when SCR not used.
2	OUTPUT	Regulator output.
3	SUPPLY VOLTAGE	Unregulated voltage input. An internal regulator powers the L296's internal logic.
4	CURRENT LIMIT	A resistor connected between this terminal and ground sets the current limiter threshold. If this terminal is left unconnected the threshold is internally set (see electrical charateristics).
5	SOFT START	Soft start time constant. A capacitor is connected between this terminal and ground to define the soft start time constant. This capacitor also determines the average short circuit output current.
6	INHIBIT INPUT	TTL – level remote inhibit. A logic high level on this input disables the device.
7	SYNC INPUT	Multiple L296s are synchronized by connecting the pin 7 inputs together and omitting the oscillator RC network on all but one device.
8	GROUND	Common ground terminal.
9	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
10	FEEDBACK INPUT	The feedback terminal of the regulation loop. The output is connected directly to this terminal for 5.1V operation; it is connected via a divider for higher voltages.
11	OSCILLATOR	A parallel RC network connected to this terminal determines the switching frequency. This pin must be connected to pin 7 input when the internal oscillator is used.

PIN FUNCTIONS (continued)

N°	NAME	FUNCTION
12	RESET INPUT	Input of the reset circuit. The threshold is roughly 5V. It may be connected to the feedback point or via a divider to the input.
13	RESET DELAY	A capacitor connected between this terminal and ground determines the reset signal delay time.
14	RESET OUTPUT	Open collector reset signal output. This output is high when the supply is safe.
15	CROWBAR OUTPUT	SCR gate drive output of the crowbar circuit.

CIRCUIT OPERATION (refer to the block diagram)

The L296 and L296P are monolithic stepdown switching regulators providing output voltages from 5.1V to 40V and delivering 4A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1V on-chip reference (zener zap trimmed to ± 2%). This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage. The gain and frequency stability of the loop can be adjusted by an external RC network connected to pin 9. Closing the loop directly gives an output voltage of 5.1V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor C_{ss} and allowed to rise, linearly, as this capacitor is charged by a constant current source.

Output overload protection is provided in the form of a current limiter. The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4V. The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network.

The reset circuit generates an output signal when the supply voltage exceeds a threshold programmed by an external divider. The reset signal is generated with a delay time programmed by an external capacitor. When the supply falls below the threshold the reset output goes low immediately. The reset output is an open collector.

The crowbar circuit senses the output voltage and the crowbar output can provide a current of 100 mA to switch on an external SCR. This SCR is triggered when the output voltage exceeds the nominal by 20%. There is no internal connection between the output and crowbar sense input therefore the crowbar can monitor either the input or the output.

A TTL - level inhibit input is provided for applications such as remote on/off control. This input is activated by high logic level and disables circuit operation. After an inhibit the L296 restarts under control of the soft start network.

The thermal overload circuit disables circuit operation when the junction temperature reaches about 150°C and has hysteresis to prevent unstable conditions.

CIRCUIT OPERATION (continued)

Fig. 1 - Reset output waveforms

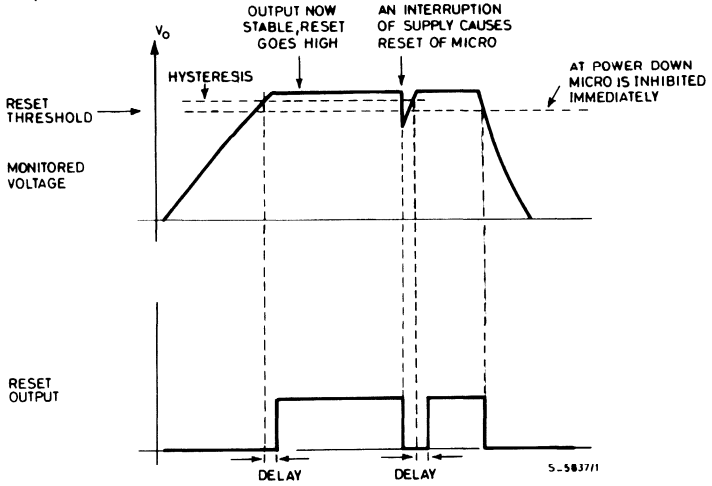


Fig. 2 - Soft start waveforms

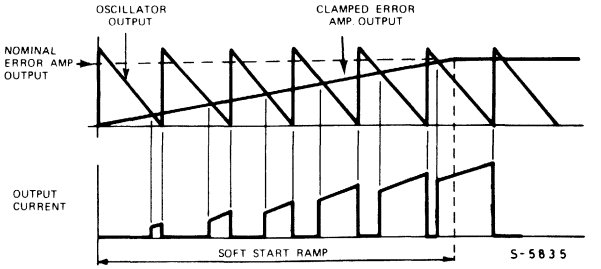
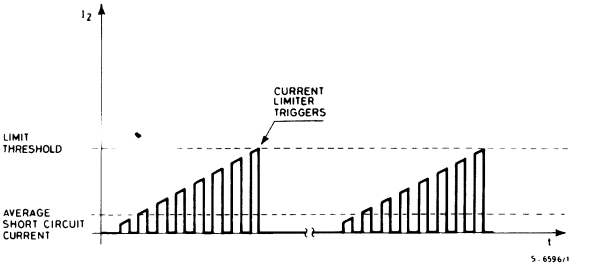


Fig. 3 - Current limiter waveforms



ELECTRICAL CHARACTERISTICS (Refer to the test circuits $T_j = 25°C$, $V_i = 35V$, unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit	Fig.
DYNAMIC CHARACTERISTICS (pin 6 to GND unless otherwise specified)								
V_o	Output voltage range	V_i = 46V	I_o = 1A	V_{ref}		40	V	4
V_i	Input voltage range	$V_o = V_{ref}$ to 36V	$I_o \leqslant$ 3A	9		46	V	4
V_i	Input voltage range	Note (1) $V_o = V_{REF}$ to 36V	I_o = 4A			46	V	4
ΔV_o	Line regulation	V_i = 10V to 40V, $V_o = V_{ref}$,	I_o = 2A		15	50	mV	4
ΔV_o	Load regulation		I_o = 2A to 4A		10	30	mV	4
		$V_o = V_{ref}$	I_o = 0.5A to 4A		15	45	mV	4
V_{ref}	Internal reference voltage (pin 10)	V_i = 9V to 46V I_o = 2A		5	5.1	5.2	V	4
$\frac{\Delta V_{ref}}{\Delta T}$	Average temperature coefficient of reference voltage	T_j = 0°C to 125°C	I_o = 2A		0.4		mV/°C	
V_d	Dropout voltage between pin 2 and pin 3	I_o = 4A			2	3.2	V	4
		I_o = 2A			1.3	2.1	V	4
I_{2L}	Current limiting threshold (pin 2)	L296 V_i = 9V to 40V $V_o = V_{ref}$ to 36V	pin 4 open	4.5		7.5	A	4
		L296P V_i = 9V to 40V $V_o = V_{ref}$	pin 4 open	5		7	A	4
			R_{lim} = 22KΩ	2.5		4.5	A	4
I_{SH}	Input average current	V_i = 46V; Output short-circuited			60	100	mA	4
η	Efficiency	I_o = 3A	$V_o = V_{ref}$		75		%	4
			V_o = 12V		85		%	4
SVR	Supply voltage ripple rejection	$\Delta V_i = 2V_{rms}$ $V_o = V_{ref}$	f_{ripple} = 100Hz I_o = 2A	50	56		dB	4
f	Switching frequency			85	100	115	KHz	4
$\frac{\Delta f}{\Delta V_i}$	Voltage stability of switching frequency	V_i = 9V to 46V			0.5		%	4
$\frac{\Delta f}{\Delta T_j}$	Temperature stability of switching frequency	T_j = 0°C to 125°C			1		%	4
f_{max}	Maximum operating switching frequency	$V_o = V_{ref}$; I_o = 1A		200			KHz	–
T_{sd}	Thermal shutdown junction temperature			135	145		°C	–
DC CHARACTERISTICS								
I_{3Q}	Quiescent drain curr.	V_i = 46V V_7 = 0V S1 : B S2 : B	V_6 = 0V		66	85	mA	6a
			V_6 = 3V		30	40	mA	6a
$-I_{2L}$	Output leakage curr.	V_i = 46V, V_6 = 3V, S1 : B, S2 : A, V_7 = 0V				2	mA	6a

Note (1): Using min. 7A schottky diode

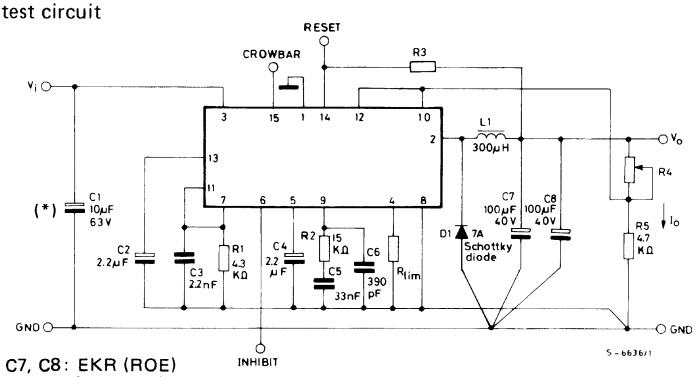
ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit	Fig.
SOFT START							
$I_{5\,so}$	Source current	V_6 = 0V, V_5 = 3V	100	130	160	μA	6b
$I_{5\,si}$	Sink current	V_6 = 3V, V_5 = 3V	50	70	120	μA	6b
INHIBIT							
V_{6L}	Low input voltage	V_I = 9V to 46V S1 : B S2 : B; V_7 = 0V	-0.3		0.8	V	6a
V_{6H}	High input voltage		2		5.5	V	6a
$-I_{6L}$	Input current with low input voltage	V_I = 9V to 46V, V_6 = 0.8V			10	μA	6a
$-I_{6H}$	Input current with high input voltage	V_7 = 0V S1 : B S2 : B, V_6 = 2V			3	μA	6a
ERROR AMPLIFIER							
V_{9H}	High level output volt.	V_{10} = 4.7V, I_9 = 100μA, S1 : A, S2 : A	3.5			V	6c
V_{9L}	Low level output volt.	V_{10} = 5.3V, I_9 = 100μA, S1 : A, S2 : E			0.5	V	6c
$I_{9\,si}$	Sink output current	V_{10} = 5.3V, S1 : A, S2 : B	100	150		μA	6c
$-I_{9\,so}$	Source output current	V_{10} = 4.7V, S1 : A, S2 : D	100	150		μA	6c
I_{10}	Input bias current	V_{10} = 5.2V S1 : B		2	10	μA	6c
		V_{10} = 6.4V, S1 : B, L296P		2	10	μA	6c
G_v	DC open loop Gain	V_9 = 1V to 3V, S1 : A, S2 : C	46	55		dB	6c
OSCILLATOR AND PWM COMPARATOR							
$-I_7$	Input bias current of PWM comparator	V_7 = 0.5V to 3.5V			5	μA	6a
$-I_{11}$	Oscillator source curr.	V_{11} = 2V, S1 : A S2 : B	5			mA	6A
RESET							
$V_{12\,R}$	Rising threshold voltage	V_I = 9V to 46V, S1 : B, S2 : B	V_{ref} -150mV	V_{ref} -100mV	V_{ref} -50mV	V	6d
$V_{12\,F}$	Falling threshold voltage		4.75	V_{ref} -150mV	V_{ref} -100mV	V	6d
$V_{13\,D}$	Delay threshold volt.	V_{12} = 5.3V, S1 : A, S2 : B	4.3	4.5	4.7	V	6d
$V_{13\,H}$	Delay threshold voltage hysteresis			100		mV	6d
$V_{14\,S}$	Output saturation volt.	I_{14} = 16mA; V_{12} = 4.7V; S1, S2 : B			0.4	V	6d
I_{12}	Input bias current	V_{12} = 0V to V_{ref}, S1 : B, S2 : B		1	3	μA	6d
$-I_{13\,so}$	Delay source current	V_{13} = 3V S1 : A S2 : B, V_{12} = 5.3V	70	110	140	μA	6d
$I_{13\,si}$	Delay sink current	V_{12} = 4.7V	10			mA	6d
I_{14}	Output leakage curr.	V_I = 46V, V_{12} = 5.3V, S1 : B, S2 : A			100	μA	6d

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Condition		Min.	Typ.	Max.	Unit	Fig.
CROWBAR								
V_1	Input threshold voltage	S1 : B		5.5	6	6.4	V	6b
V_{15}	Output saturation voltage	V_i = 9V to 46V, I_{15} = 5mA	V_1 = 5.4V S1 : A		0.2	0.4	V	6b
I_1	Input bias current	V_1 = 6V,	S1 : B			10	μA	6b
$-I_{15}$	Output source current	V_i = 9V to 46V, V_{15} = 2V	V_1 = 6.5V S1 : B	70	100		mA	6b

Fig. 4 - Dynamic test circuit



C7, C8: EKR (ROE)
L1: L = 300μH at 8A Core type: MAGNETICS 58930 - A2 MPP
R = 50mΩ N° turns: 43 Wire Gauge: 1mm (18 AWG) COGEMA 946044
(*) Minimum suggested value (10μF) to avoid oscillations. Ripple consideration leads to typical value of 1000μF or higher.

Fig. 5 - PC. board and component layout of the circuit of fig. 4 (1:1 scale)

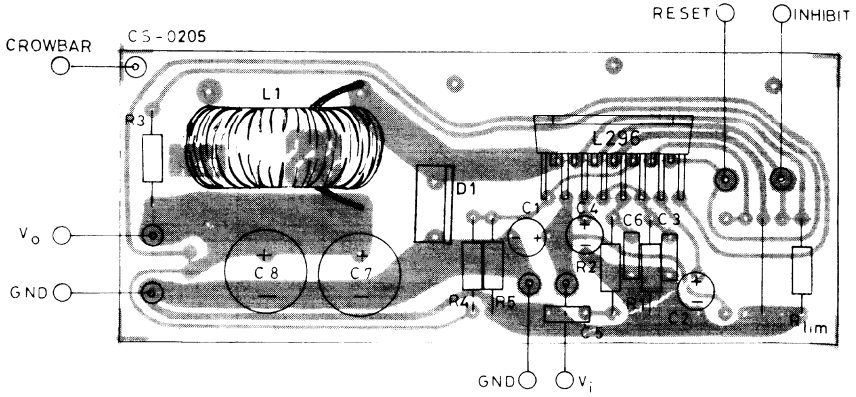


Fig. 6 - DC test circuits

Fig. 6a

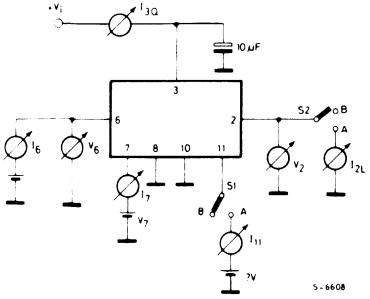


Fig. 6b

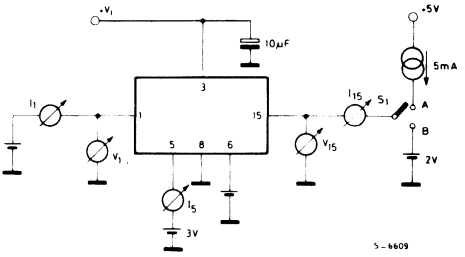


Fig. 6c

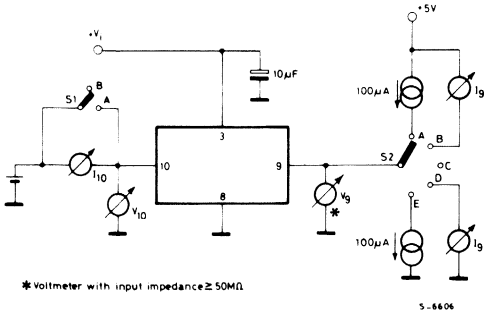
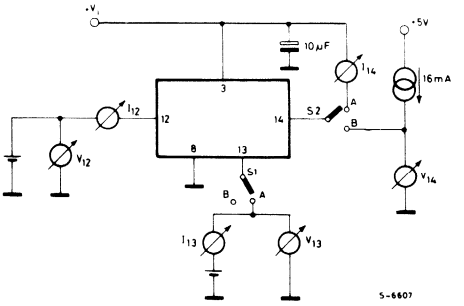


Fig. 6d



1 - Set V_{10} for $V_9 = 1V$

2 - Change V_{10} to obtain $V_9 = 3V$

3 - $G_v = \frac{\Delta V_9}{\Delta V_{10}} = \frac{2V}{\Delta V_{10}}$

Fig. 7 - Quiescent drain current vs. supply voltage (0% duty cycle - see fig. 6a)

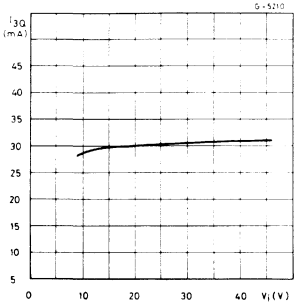


Fig. 8 - Quiescent drain current vs. supply voltage (100% duty cycle see fig. 6a)

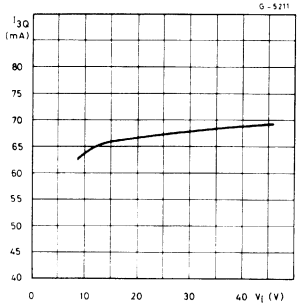


Fig. 9 - Quiescent drain current vs. junction temperature (0% duty cycle - see fig. 6a)

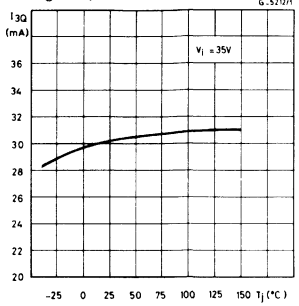


Fig. 10 - Quiescent drain current vs. junction temperature (100% duty cycle - see fig. 6a)

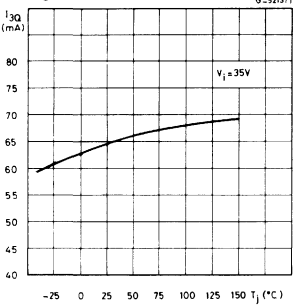


Fig. 11 - Reference voltage (pin 10) vs. V_i (see fig. 4)

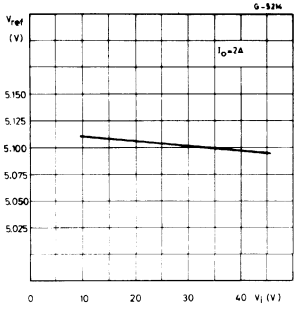


Fig. 12 - Reference voltage (pin 10) vs. junction temperature (see fig. 4)

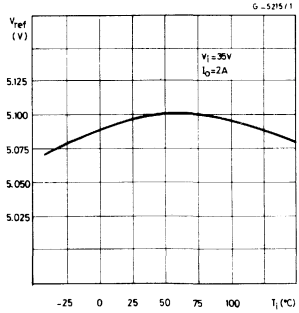


Fig. 13 - Open loop frequency and phase response of error amplifier (see fig. 6c)

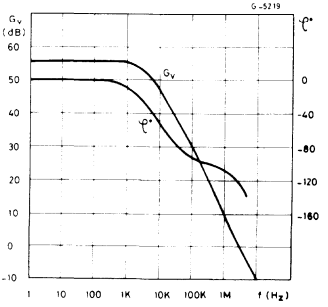


Fig. 14 - Switching frequency vs. input voltage (see fig. 4)

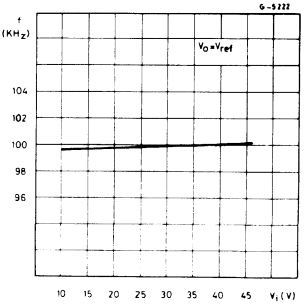


Fig. 15 - Switching frequency vs. junction temperature (see fig. 4)

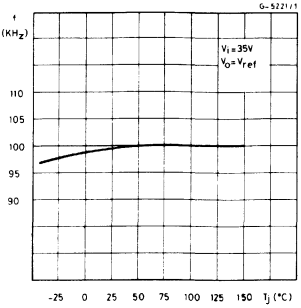


Fig. 16 - Switching frequency vs. R1 (see fig. 4)

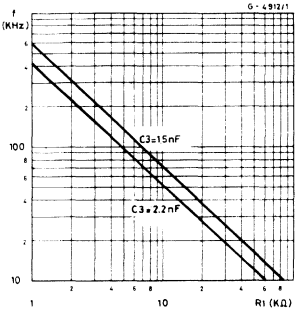


Fig. 17 - Line transient response (see fig. 4)

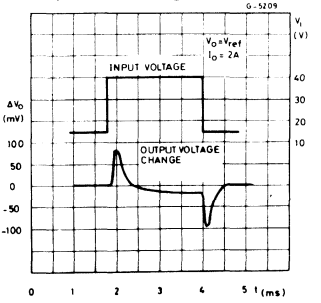


Fig. 18 - Load transient response (see fig. 4)

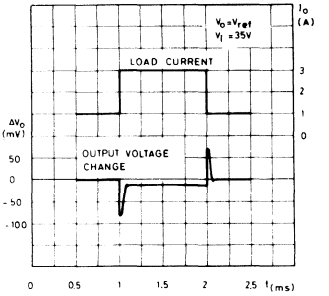


Fig. 19 - Supply voltage ripple rejection vs. frequency (see fig. 4)

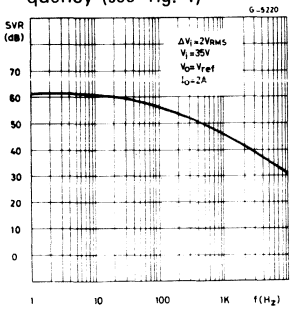


Fig. 20 - Dropout voltage between pin 3 and pin 2 vs. current at pin 2

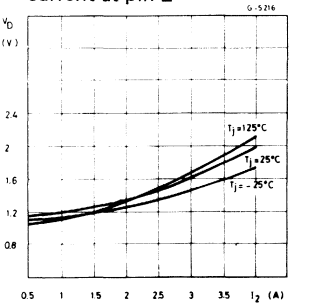


Fig. 21 - Dropout voltage between pin 3 and pin 2 vs. junction temperature

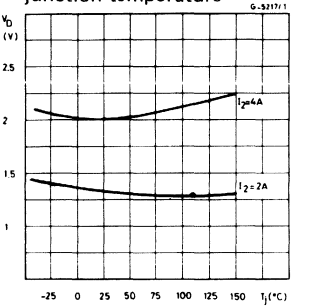


Fig. 22 - Power dissipation derating curve

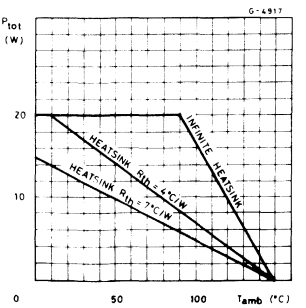


Fig. 23 - Power dissipation (device only) vs. input voltage

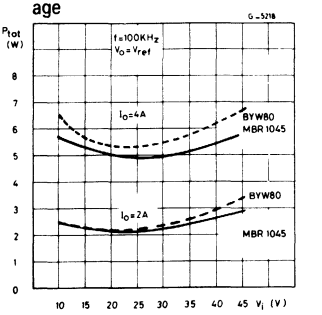


Fig. 24 - Power dissipation (device only) vs. input voltage

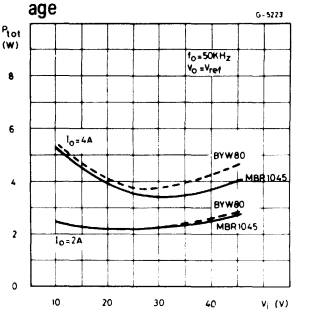


Fig. 25 - Power dissipation (device only) vs. output voltage (see fig. 4)

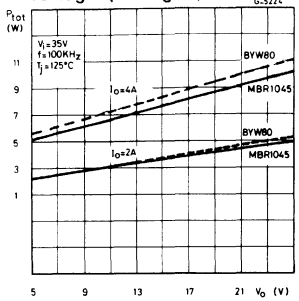


Fig. 26 - Power dissipation (device only) vs. output voltage (see fig. 4)

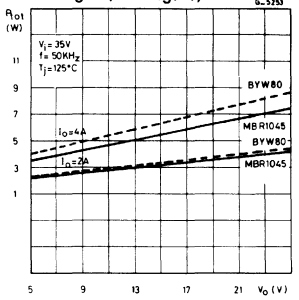


Fig. 27 - Voltage and current waveforms at pin 2 (see fig. 4)

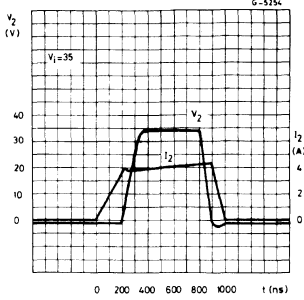


Fig. 28 - Efficiency vs. output current

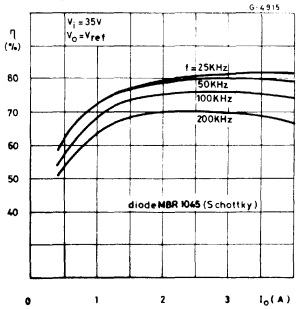


Fig. 29 - Efficiency vs. output current

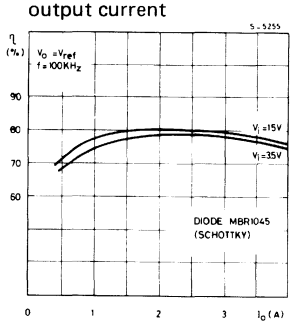


Fig. 30 - Efficiency vs. output voltage

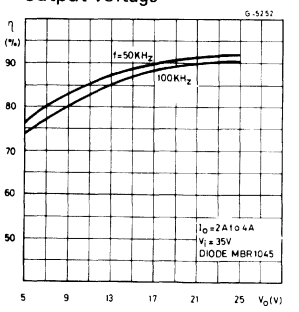


Fig. 31 - Current limiting threshold vs. $R_{pin\ 4}$ (L296P only)

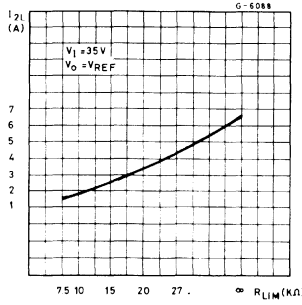


Fig. 32 - Current limiting threshold vs. junction temperature

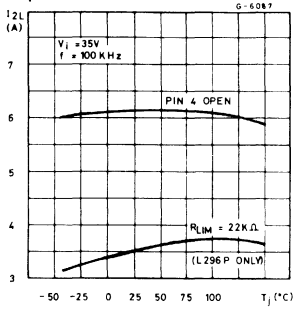
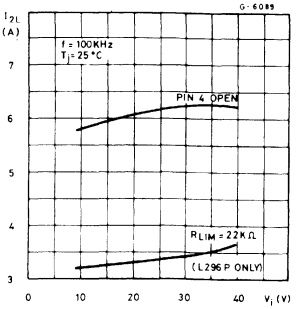
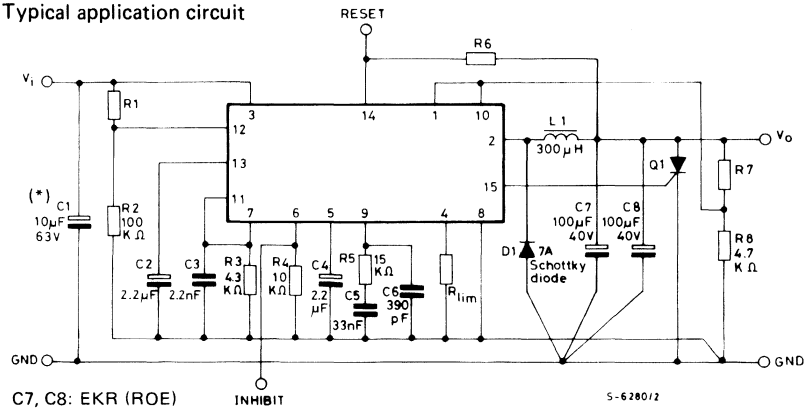


Fig. 33 - Current limiting threshold vs. supply voltage



APPLICATION INFORMATION

Fig. 34 - Typical application circuit



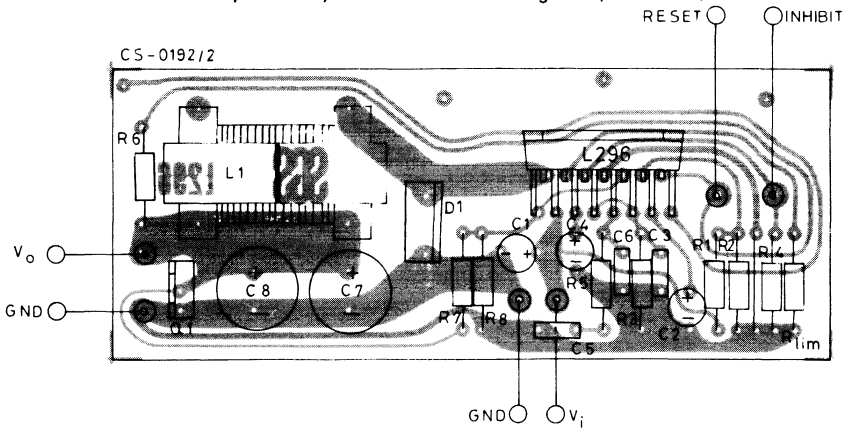
(*) Minimum value (10μF) to avoid oscillations; ripple consideration leads to typical value of 1000μF or higher
L1: 58930 - MPP COGEMA 946044; GUP 20 COGEMA 946045

SUGGESTED INDUCTOR (L1)

Core Type	No Turns	Wire Gauge	Air Gap
Magnetics 58930 - A2MPP	43	1.0 mm.	–
Thomson GUP 20x16x7	65	0.8 mm.	1 mm.
Siemens EC 35/17/10 (B6633& - G0500 - X127)	40	2 x 0.8 mm.	–
VOGT 250 μH Toroidal coil, part number 5730501800			

Resistor values for standard output voltages		
V_o	R8	R7
12V	4.7 kΩ	6.2 kΩ
15V	4.7 kΩ	9.1 kΩ
18V	4.7 kΩ	12 kΩ
24V	4.7 kΩ	18 kΩ

Fig. 35 - P.C. board and component layout of the circuit of fig. 34 (1 : 1 scale)



SELECTION OF COMPONENT VALUES (See fig. 31)

Component	Recommended Value	Purpose	Allowed rage Min	Allowed rage Max	NOTES
R1 R2	– 100 kΩ	Set input voltage threshold for reset.	–	220 kΩ	$R1/R2 = \frac{V_{i\,min}}{5} - 1$ If output voltage is sensed R1 and R2 may be limited and pin 12 connected to pin 10.
R3	4.3 kΩ	Sets switching frequency	1 kΩ	100 kΩ	
R4	10 kΩ	Pull-down resistor		22 kΩ	May be omitted and pin 6 grounded if inhibit not used.
R5	15 kΩ	Frequency compensation	10 kΩ		
R6		Collector load for reset output	$\frac{V_o}{0.05A}$		Omitted if reset function not used.
R7 R8	– 4.7 kΩ	Divider to set output voltage	– –	– 10 kΩ	$R7/R8 = \frac{V_o - V_{ref}}{V_{ref}} -$
R_{lim}	–	Sets current limit level	7.5 kΩ		If R_{lim} is omitted and pin 4 left open the current limit is internally fixed.
C1	10 μF	Stability	2.2 μF		
C2	2.2 μF	Sets reset delay	–	–	Omitted if reset function not used.
C3	2.2 nF	Sets switching frequency	1 nF	3.3 nF	
C4	2.2 μF	Soft start	1 μF	–	Also determines average short circuit current.
C5	33 nF	Frequency compensation			
C6	390 pF	High frequency compensation	–	–	Not required for 5V operation
C7,C8 L1	100 μF 300 μH	Output filter	– 100 μH	–	
Q1		Crowbar protection			The SCR must be able to withstand the peak discharge current of the output capacitor and the short circuit current of the device.
D1		Recirculation diode			7A schottky or 35ns t_{rr} diode.

APPLICATION INFORMATION (continued)

Fig. 36 - A minimal 5.1V fixed regulator. Very few components are required

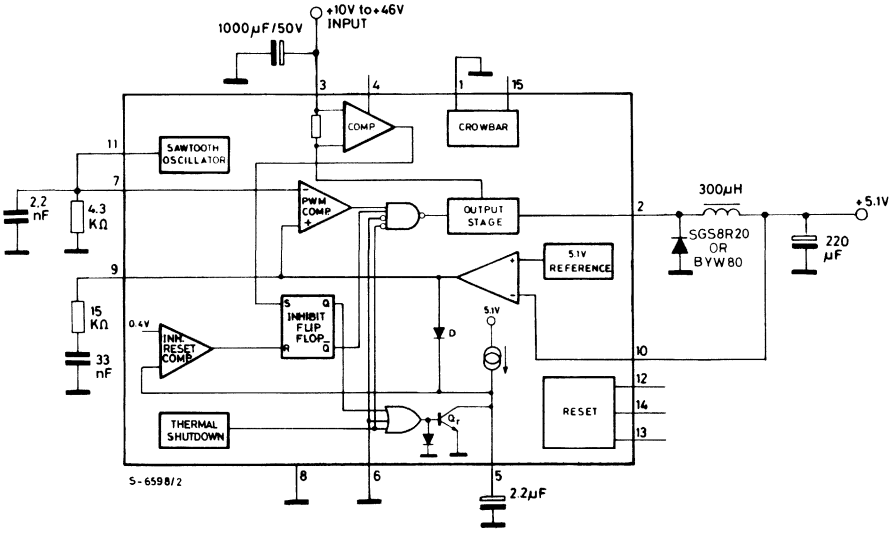
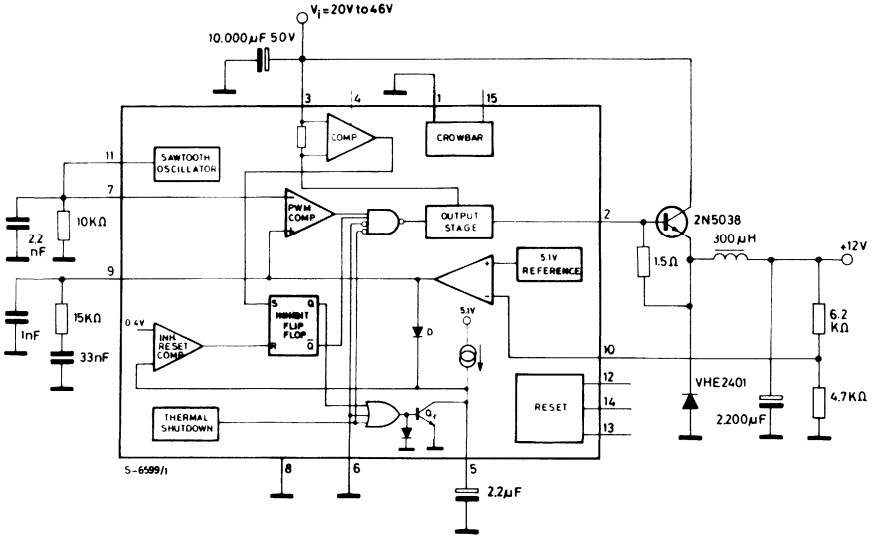
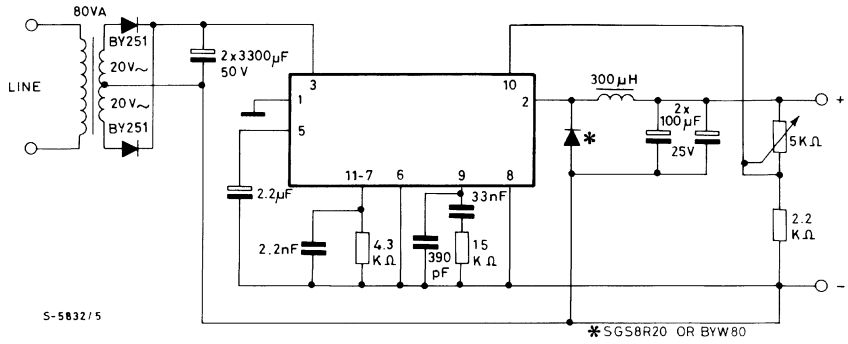


Fig. 37 - 12V/10A Power supply



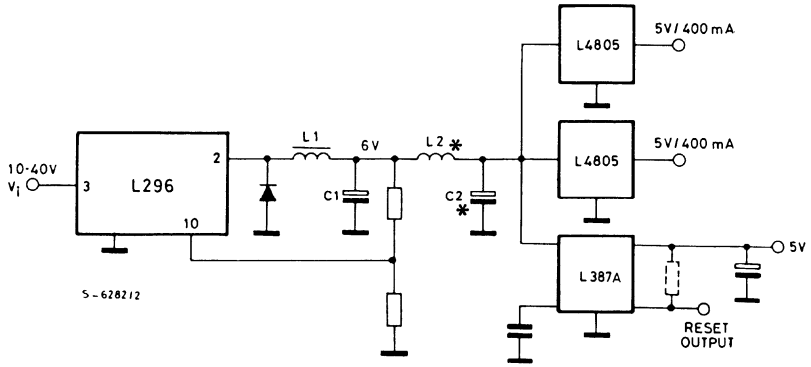
APPLICATION INFORMATION (continued)

Fig. 38 - Programmable power supply



V_o = 5.1 to 15V
I_o = 4A max. (min. load current = 100 mA)
ripple ⩽ 20 mV
load regulation (1A to 4A) = 10 mV (V_o = 5.1V)
line regulation (220V ± 15% and to I_o = 3A) = 15 mV (V_o = 5.1V)

Fig. 39 - Preregulator for distributed supplies



(*) L2 and C2 are necessary to reduce the switching frequency spikes.

APPLICATION INFORMATION (continued)

Fig. 40 - In multiple supplies several L296s can be synchronized as shown.

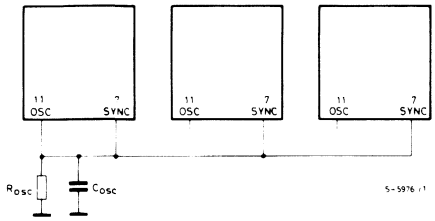


Fig. 41 - Voltage sensing for remote load

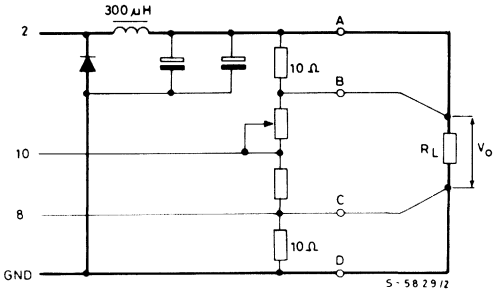


Fig. 42 - A 5.1V/15V/24V multiple supply. Note the synchronization of the three L296s.

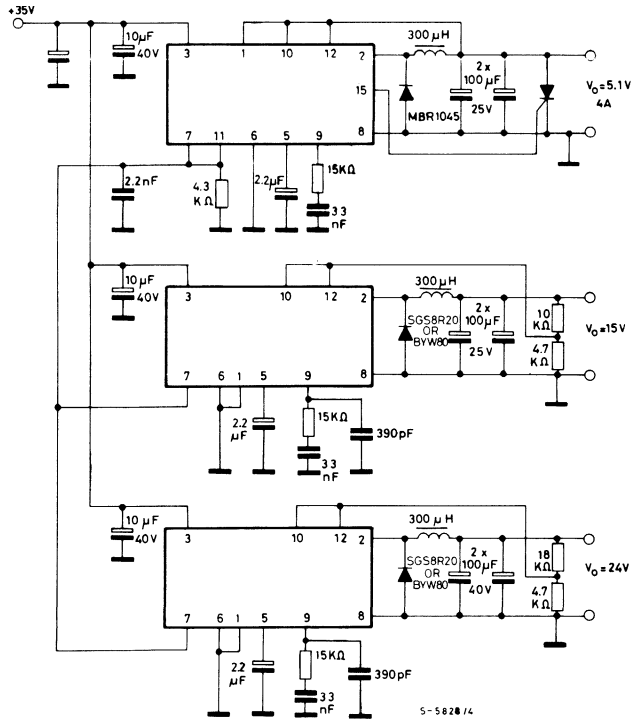
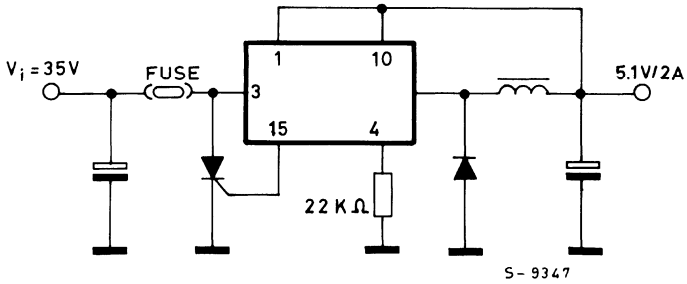


Fig. 43 - 5.1V/2A Power supply using external limiting current resistor and crowbar protection on the supply voltage (L296P only)



SOFT-START AND REPETITIVE POWER-ON

When the device is repetitively powered-on, the soft-start capacitor, C_{ss}, must be discharged rapidly to ensure that each start is "soft". This can be achieved economically using the reset circuit, as shown in Fig. 44.

In this circuit the divider R_1, R_2 connected to pin 12 determines the minimum supply voltage, below which the open collector transistor at the pin 14 output discharges C_{ss}.

The approximate discharge times obtained with this circuit are:

C_{ss}	t_{DIS}
2.2μF	200μs
4.7μF	300μs
10μF	600μs

If these times are still too long, an external PNP transistor may be added, as shown in Fig. 45; with this circuit discharge times of a few microseconds may be obtained.

Fig. 44

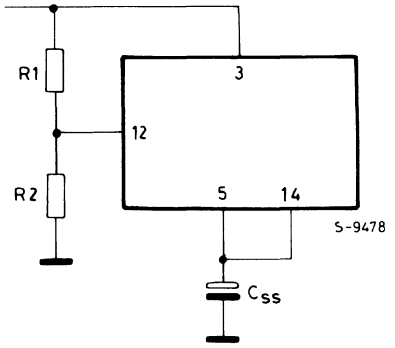
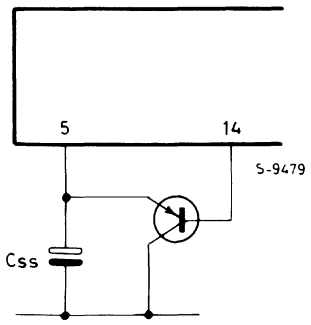


Fig. 45



HOW TO OBTAIN BOTH RESET AND POWER FAIL

Figure 46 illustrates how it is possible to obtain at the same time both the power fail and reset functions simply by adding one diode (D) and one resistor (R).

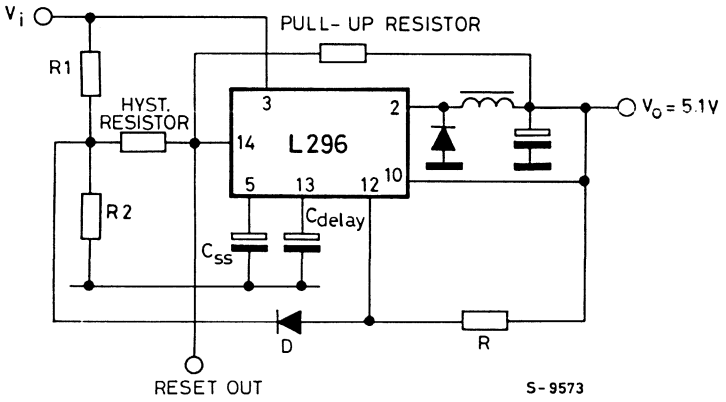
In this case the reset delay time (pin 13) can only start when the output voltage is $V_o \geqslant V_{REF}$ - 100mV and the voltage across R2 is higher than 4.5V.

With the hysteresis resistor it is possible to fix the input pin 12 hysteresis in order to increase immunity to the 100Hz ripple present on the supply voltage.

Moreover, the power fail and reset delay time are automatically locked to the soft start. Soft start and delayed reset are thus two sequential functions.

The hysteresis resistor should be in the range of about 100KΩ and the pull-up resistor of 1 to 2.2KΩ.

Fig. 46



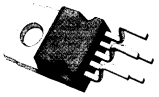
L387A

ADVANCE DATA

VERY LOW DROP 5V REGULATOR

- PRECISE OUTPUT VOLTAGE (5V ± 4%)
- VERY LOW DROPOUT VOLTAGE
- OUTPUT CURRENT IN EXCESS OF 500mA
- POWER-ON, POWER-OFF INFORMATION (RESET FUNCTION)
- HIGH NOISE IMMUNITY ON RESET DELAY CAPACITOR

The L387A is a very low drop voltage regulator in a Pentawatt® package specially designed to provide stabilized 5V supplies in consumer and industrial applications. Thanks to its very low input/output voltage drop this device is very useful in battery powered equipment, reducing consumption and prolonging battery life. A reset output makes the L387A particularly suitable for microprocessor systems. This output provide a reset pulse when power is applied (after an external programmable delay) and goes low when power is removed, inhibiting the microprocessor. An hysteresis on reset delay capacitor raises the immunity to the ground noise.



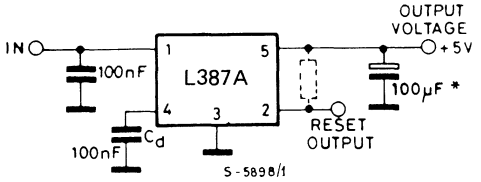
Pentawatt®

ORDERING NUMBER: L387A

ABSOLUTE MAXIMUM RATINGS

V_i	Forward input voltage	35 V
V_i	Reverse input voltage	-18 V
T_{op}	Operating junction temperature	-40 to +125 °C
T_{stg}	Storage temperature	-55 to +150 °C

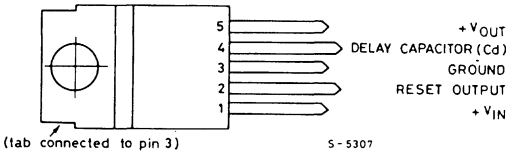
TEST CIRCUIT



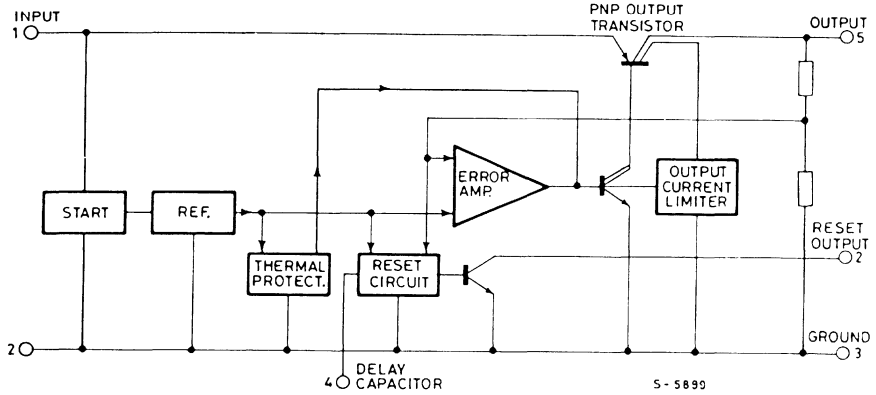
* Min 33µF and max. ESR ⩽ 3Ω over temperature range

L387A

CONNECTION DIAGRAM
(Top view)



BLOCK DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, V_i = 14.4 T_j = 25°C, unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_o	Output voltage	I_o = 5mA to 500mA		4.80	5	5.20	V
V_i	Operating input voltage	(*)				26	V
ΔV_o	Line regulation	V_i = 6V to 26V	I_o = 5mA		5	50	mV
ΔV_o	Load regulation	I_o = 5mA to 500mA			15	60	mV
$V_i - V_o$	Dropout voltage	I_o = 500mA			0.60	0.8	V
I_q	Quiescent current		I_o = 5mA I_o = 150mA I_o = 350mA I_o = 500mA		5 20 60 100	15 35 100 160	mA
		V_i = 6.2V	I_o = 500mA		160	180	
$\frac{\Delta V_o}{\Delta T}$	Temperature output voltage drift				-0.5		mV/°C
SVR	Supply voltage rejection	I_o = 350mA C_o = 100µF	f = 120Hz V_i = 12V ± 5 Vpp		60		dB
I_{sc}	Output short circuit current				0.8	1.5	A
V_R	Reset output voltage	I_R = 16mA	V_o < 4.75V			0.8	V
I_R	Reset output leakage current	V_o in regulation				50	µA
t_d	Delay time for reset output	Cd = 100nF			30		ms
$V_{RT(off)}$	Reset threshold (delay charging current on)			4.75	V_o-0.15	V_o-0.04	V
I_{C4}	Charging current (current generator)	V_4 = 3V		10		30	µA
$V_{RT(on)}$	Reset threshold (low)				$V_{RT(off)}$ -10mV		V
V_4	Comparator threshold (pin 4)	Reset out = "0"		3.2		3.9	V
		Reset out = "1"		3.7		4.3	V
V_H	Hysteresis voltage				500		mV

(*) For a DC voltage 26 < V_i < 35V the device is not operating

Fig. 1 - Dropout Voltage vs. output current

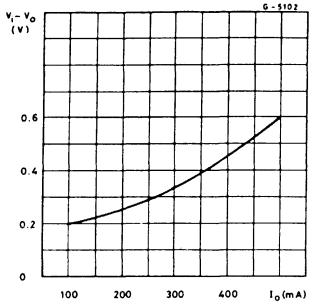


Fig. 2 - Quiescent current vs. output current

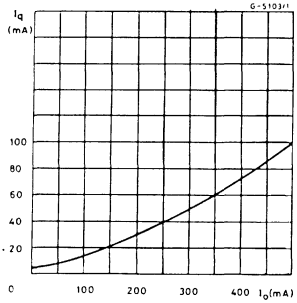
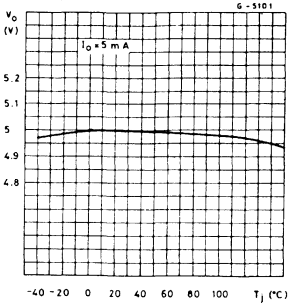


Fig. 3 - Output voltage vs. temperature



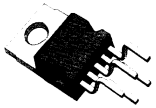
L487

PRELIMINARY DATA

VERY LOW DROP 5V VOLTAGE REGULATOR WITH RESET

- PRECISE OUTPUT VOLTAGE (5V ± 4%)
- VERY LOW DROPOUT VOLTAGE
- OUTPUT CURRENT IN EXCESS OF 500mA
- POWER-ON, POWER-OFF INFORMATION (RESET FUNCTION)
- +80/-80V LOAD DUMP PROTECTION
- OVERVOLTAGE AND REVERSE VOLTAGE PROTECTION
- SHORT CIRCUIT PROTECTION AND THERMAL SHUT-DOWN

The L487 is a monolithic integrated circuit in Pentawatt® package specially designed to provide a stabilized supply voltage for automotive and industrial electronic system. Thanks to its very low voltage drop, in automotive applications the L487 can work correctly even during the cranking phase, when the battery voltage could fall as low as 6V. Furthermore, it incorporates a complete range of protection circuits against the dangerous overvoltages always present on the battery rail of the car. The reset function makes the device particularly suited to supply microprocessor based systems: a pulse is available (after an externally programmable delay) to reset the microprocessor at power-on phase; at power-off, this pulse becomes low inhibiting the microprocessor.



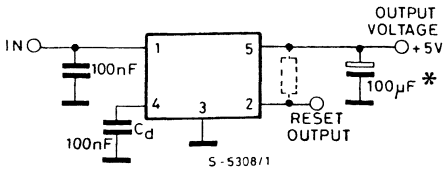
Pentawatt®

ORDERING NUMBER: L487

ABSOLUTE MAXIMUM RATINGS

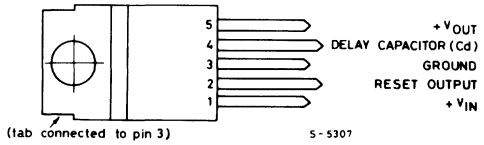
V_i	Forward input voltage	35	V
V_i	Reverse input voltage	-18	V
	Positive transient peak voltage (t = 300 ms)	80	V
	Negative transient peak voltage (t = 100 ms)	-80	V
T_{op}	Operating junction temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

TEST CIRCUIT



* Min. 33µF and max. ESR ⩽ 3Ω over temperature range

CONNECTION DIAGRAM (top view)



BLOCK DIAGRAM

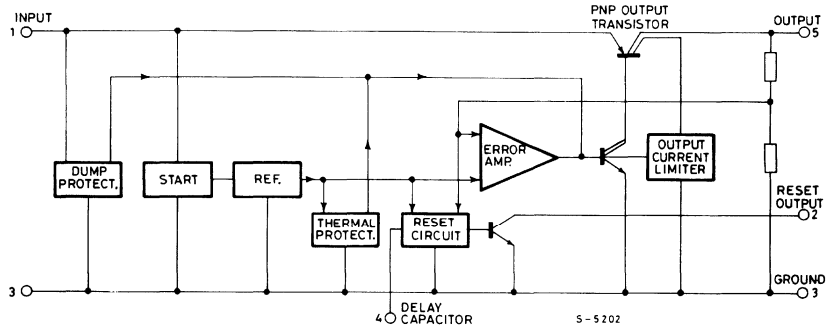


Fig. 1 - Dropout voltage vs. output current

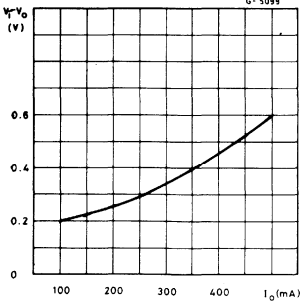


Fig. 2 - Quiescent current vs. output current

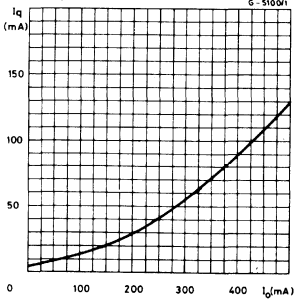
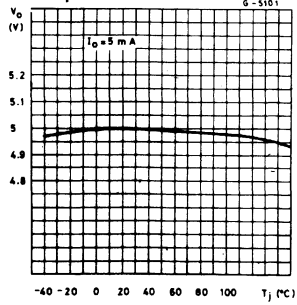


Fig. 3 - Output voltage vs. temperature



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max 4	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $V_I = 14.4V$, $T_{amb} = 25°C$, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_O	Output voltage	I_O = 5mA to 500mA	4.80	5	5.20	V
V_I	Operating input voltage	(*) See note			28	V
ΔV_O	Line regulation	V_I = 6 to 26V I_O = 5mA		5	50	mV
ΔV_O	Load regulation	I_O = 5 to 500mA		15	60	mV
$V_I - V_O$	Dropout voltage	I_O = 500mA		0.6	0.8	V
I_q	Quiescent current	I_O = 0mA I_O = 150mA I_O = 500mA		6 20 130	15 40 210	mA
		V_I = 6.2V I_O = 500mA			250	
$\frac{\Delta V_O}{\Delta T}$	Temperature output voltage drift			-0.5		mV/°C
SVR	Supply voltage rejection	I_O = 350mA f = 120Hz C_O = 100μF V_I = 12V ± 5Vpp		55		dB
I_{sc}	Output short circuit current			0.8		A
V_R	Reset output voltage	I_R = 16mA $V_O \leq 4.75V$			0.8	V
I_R	Reset output leakage current	V_O in regulation			50	μA
t_d	Delay time for reset output	Cd = 100nF		30		ms
$V_{RT(off)}$	Reset threshold (delay charging current on)		4.75	V_O-0.15	V_O-0.04	V
I_{C4}	Charging current (current generator)		10		27	μA
$V_{RT(on)}$	Reset threshold (low)			$V_{RT(off)}$ -10mV		V
V_4	Comparator threshold (pin 4)		3.6		3.95	V

* For a DC input voltage $28 < V_I < 35V$ the device is not operating

L601 L603
L602 L604

DARLINGTON ARRAYS

- EIGHT DARLINGTONS PER PACKAGE
- OUTPUT CURRENT 400mA PER DRIVER (500mA PEAK)
- OUTPUT VOLTAGE 90V ($V_{CE(sus)}$ = 70V)
- INTEGRAL SUPPRESSION DIODES FOR INDUCTIVE LOADS
- OUTPUTS CAN BE PARALLELED FOR HIGHER CURRENT
- TTL / CMOS / PMOS / DTL COMPATIBLE INPUTS
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY LAYOUT

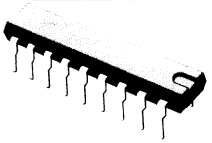
The L601, L602, L603 and L604 are high voltage, high current darlington arrays each containing eight open collector darlington pairs with common emitters. Each channel is rated at 400 mA and can withstand peak currents of 500mA. Suppression diodes are included for inductive oad driving and the inputs are pinned opposite the outputs to simplify board layout.

The four versions interface to all common logic families:

L601	General purpose
L602	14-25V PMOS
L603	5V TTL, CMOS
L604	6 - 15V CMOS, PMOS

These versatile devices are useful for driving a wide range of loads, including solenoids, relays DC motors, LED dispalys, filament lamps, thermal printheads and high power buffers.

The L601, L602, L603 and L604 are supplied in 18 pin plastic DIP packages with a copper leadframe to reduce thermal resistance.



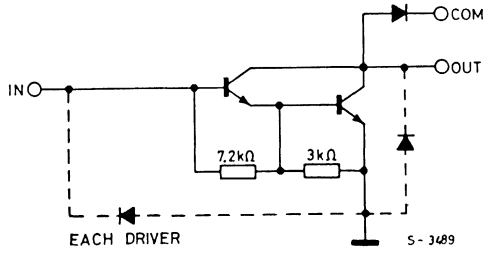
DIP-18 Plastic

ORDERING NUMBERS: L601B, L603B
L602B, L604B

ABSOLUTE MAXIMUM RATINGS

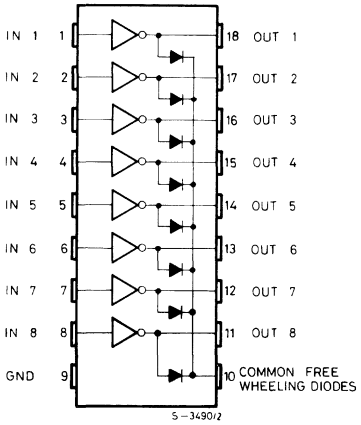
V_{CEX}	Collector emitter voltage (input open)	90	V
I_C	Collector current	0.4	A
I_C	Collector peak current	0.5	A
V_i	Input voltage (for L602, L603 and L604)	30	V
I_i	Input current (for L601 only)	25	mA
P_{tot}	Total power dissipation a T_{amb} = 25°C	1.8	W
T_{op}	Operating junction temperature	-25 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

SCHEMATIC DIAGRAM (L601 – One darlington only)



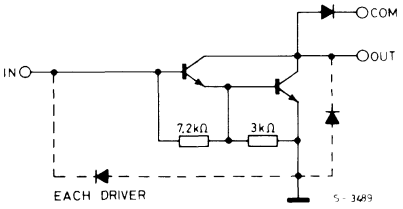
L601 L603
L602 L604

CONNECTION DIAGRAM
(top view)

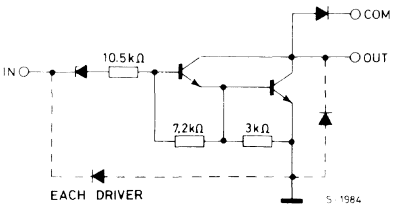


SCHEMATIC DIAGRAMS

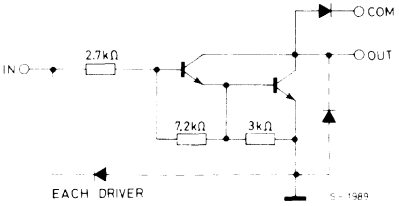
L601



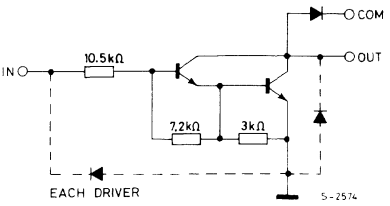
L602



L603



L604



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_{CEX}	Output leakage current	V_{CE}= 90V			10	μA
$V_{CE(sat)}$	Collector emitter saturation voltage	I_C= 300 mA I_B= 500 μA I_C= 200 mA I_B= 350 μA I_C= 100 mA I_B= 250 μA			2 1.7 1.2	V V V
h_{FE}	DC forward current gain (L601 only)	V_{CE}= 3V I_C= 300 mA	1000			–
V_i	Minimum input voltage (ON condition)	V_{CE}= 3V I_C= 300 mA for L602 for L603 for L604			 11.5 2.5 2.5	 V V V
V_i	Maximum input voltage (OFF condition)	V_{CE}= 90V I_C= 25 μA for L601 for L602 for L603 for L604	 0.55 7 0.75 1			 V V V V
I_R	Clamp diode reverse current	V_R= 90V			50	μA
V_F	Clamp diode forward voltage	I_F= 300 mA		2	2.4	V
t_{on}	Turn-on delay	0.5 V_i to 0.5 V_o		0.4		μs
t_{off}	Turn-off delay	0.5 V_i to 0.5 V_o		0.4		μs

L702

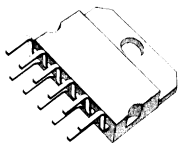
PRELIMINARY DATA

2A QUAD DARLINGTON SWITCH

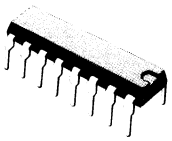
- SUSTAINING VOLTAGE: 70V
- 2A OUTPUT
- HIGH CURRENT GAIN
- IDEAL FOR DRIVING SOLENOIDS, DC MOTORS, STEPPER MOTORS, RELAYS, DISPLAYS, ETC.

The L702 is a monolithic integrated circuit for high current and high voltage switching applications it comprises four darlington transistors with common emitter and open collector suitable for current sinking applications, mounted on the new POWERDIP and Multiwatt® packages.

This circuit reduces components, sizes and costs; it can provide direct interface between low level logic and a variety of high current applications.



Multiwatt-11



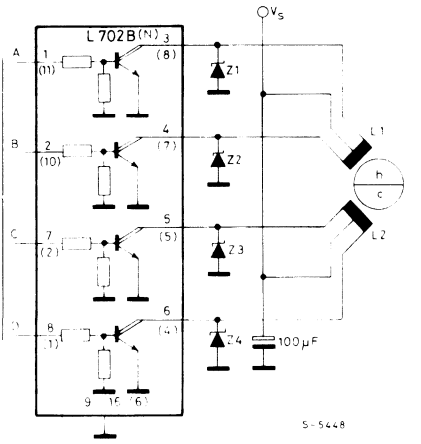
Powerdip 8 + 8

ORDERING NUMBER: L702B - Powerdip
L702N - Multiwatt

ABSOLUTE MAXIMUM RATINGS

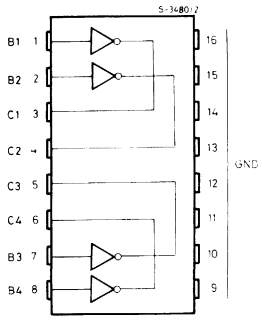
V_{CEX}	Collector-emitter voltage (input open)		90	V
V_i	Input voltage		30	V
I_C	Collector current		3	A
P_{tot}	Total power dissipation at $T_{pin\ 9\ to\ 16} \leqslant 90°C$	Powerdip	4	W
	Total power dissipation at $T_{amb} \leqslant 70°C$	Powerdip	1.1	W
	Total power dissipation at $T_{case} \leqslant 90°C$	Multiwatt	20	W
T_{stg}	Storage temperature		-55 to 150	°C
T_j	Operating junction temperature		-25 to 150	°C

Stepping motor buffer

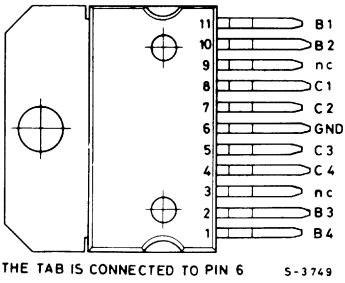


L702

CONNECTION DIAGRAMS (top view)

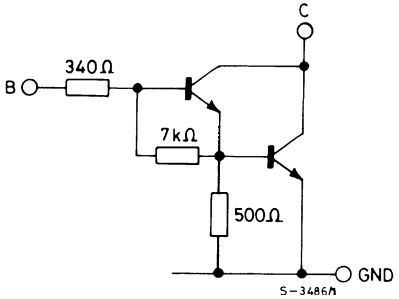


Powerdip



Multiwatt

SCHEMATIC DIAGRAM (each Darlington)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction ambient	Powerdip	max	70	°C/W
$R_{th\ j\text{-}pins\ 9/16}$	Thermal resistance junction pins 9 to 16	Powerdip	max	14	°C/W
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	Multiwatt	max	3	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_{CEX}	Output leakage current	V_{CE} = 90V		10	50	μA
$V_{CE\ (sust)}$	Collector emitter (°) sustaining voltage	I_C = 100 mA	70			V
$V_{CE\ (sat)}$	Collector emitter saturation voltage	I_C = 1.25A I_i = 2 mA		1.3	1.9	V
h_{FE}	DC forward current gain	I_C = 1A V_{CE} = 3V	1000	4000		
I_i	Input current	V_i = 3.75V V_i = 2.4V open collector		7 3	11 6	mA mA
V_i	Input voltage off condition	V_{CE} = 70V $I_C \leq$ 0.1 mA			0.4	V
	on condition	V_{CE} = 3V $I_C \geq$ 1A	2.4			V
t_{on}	Turn on time	V_s = 12V		0.3		μs
t_{off}	Turn off time	R_L = 10 Ω		1		μs

(°) Pulsed: pulse duration = 300 μs, duty cycle = 1.5%.

Fig. 1 - Switching time

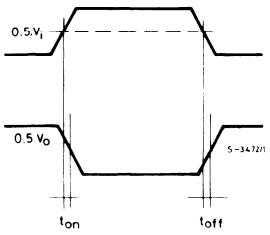


Fig. 2 - t_{on} and t_{off} test circuit

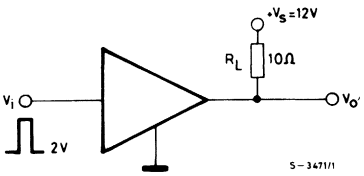


Fig. 3 - Peak collector current vs. duty cycle and number of outputs(L702B only)

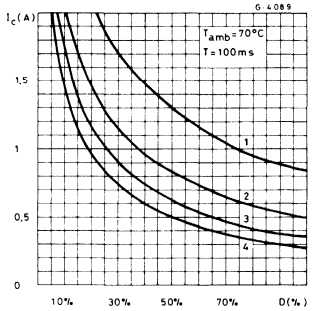


Fig. 4 - Collector emitter saturation voltage vs. collector current

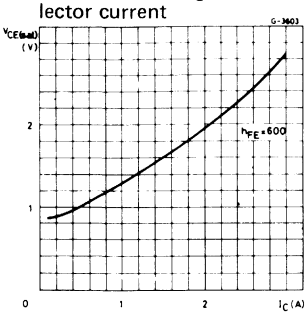


Fig. 5 - Collector current vs. input voltage

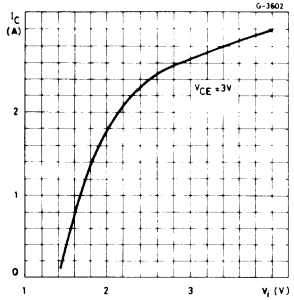


Fig. 6 - Input current vs. input voltage

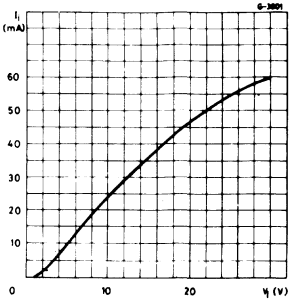


Fig. 7 - Safe operating areas (L702B)

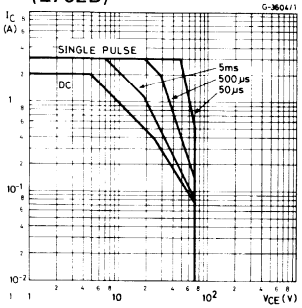


Fig. 8 - Safe operating areas (L702N)

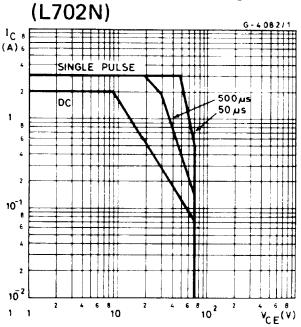
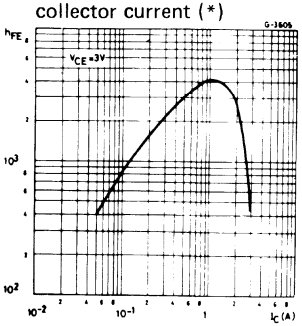


Fig. 9 - DC current gain vs. collector current (*)



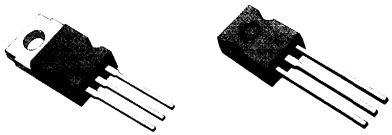
(*) Pulse width = 300 µs, duty cycle 1.5%.

L2605
L2685
L2610

VOLTAGE REGULATORS FOR AUTOMOTIVE AND INDUSTRIAL APPLICATIONS

- OUTPUT VOLTAGE OF 5, 8.5 AND 10V
- OUTPUT CURRENT UP TO 500mA
- NO EXTERNAL COMPONENTS
- LOW DROP-OUT VOLTAGE
- LOAD DUMP VOLTAGE SURGE PROTECTION
- REVERSE VOLTAGE PROTECTION
- SHORT CIRCUIT PROTECTION
- CURRENT LIMITING
- THERMAL SHUTDOWN

The L2600 series of three terminal positive regulators is specially designed to stabilize power supplies car instrumentation in vehicles with 12V battery. They can supply an output current up to 500mA.



TO-220 **SOT-82**

ABSOLUTE MAXIMUM RATINGS

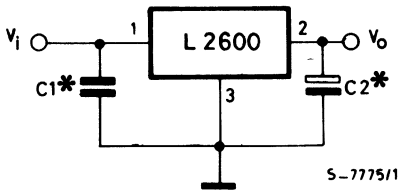
V_i	DC input voltage	35	V
V_i	DC input reverse voltage	-28	V
V_d	Positive transient peak voltage (t = 40 ms, duty cycle = 1%)	+ 100	V
V_d	Negative transient peak voltage (t = 30 ms, duty cycle = 1%)	- 100	V
T_{op}	Operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-65 to 150	°C
P_{tot}	Power dissipation	Internally limited	

ORDERING NUMBERS:

TO-220
- L2605V (V_o = 5V)
- L2685V (V_o = 8.5V)
- L2610V (V_o = 10V)

SOT-82
- L2605X
- L2685X
- L2610X

APPLICATION CIRCUIT

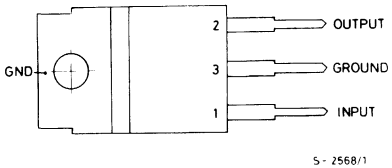


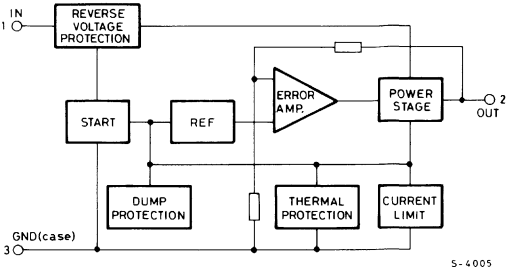
(*) Note - C_1 and C_2 are only nedeed if the load capacitance exceeds 1000pF, Recommended values are $C_1 = 0.1\mu F$ and $C_2 \geq 100\mu F$.

L2605
L2685
L2610

CONNECTION AND BLOCK DIAGRAMS

(top view)





THERMAL DATA

			SOT-82	TO-220
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	8°C/W	4°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100°C/W	50°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_o	Output voltage	I_o = 500 mA	V_i = 12 to 16V (L2605) V_i = 12 to 16V (L2685) V_i = 12 to 16V (L2610)	4.8 8.15 9.55	5 8.5 10	5.2 8.85 10.45	V
V_i	Operating input voltage	see note (°)				28	V
$\frac{\Delta V_o}{V_o}$	Line regulation	I_o = 50 mA	V_i = 12 to 20V		0.05	0.8	%
	Load regulation	V_i = 14V	I_o = 50 to 500 mA		0.3		%
$\Delta V_{i\text{-}o}$	Dropout voltage	I_o = 500 mA				1.9	V
I_d	Quiescent current	I_o = 500 mA			15		mA
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o = 50mA T_{amb} = -12 to 80°C	V_i = 14V		-1		mV/°C
I_{sc}	Output short circuit current	V_i = 14V			900		mA
SVR	Supply voltage rejection	V_i = 16V f = 100Hz	ΔV_i = 2V I_o = 500mA		60		dB
R_o	Output resistance	I_o = 500mA			0.05		Ω
e_N	Output noise voltage	BW = 100Hz to 10KHz			20		μV

(°) Note: For a DC input voltage 28V < V_i < 35V the device is not operating

L2720
L2722

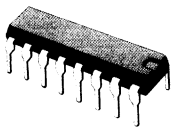
ADVANCE DATA

LOW DROP DUAL POWER OPERATIONAL AMPLIFIERS

- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- LOW INPUT OFFSET VOLTAGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN
- CLAMP DIODE

The L2720 and L2722 are monolithic integrated circuits in powerdip and minidip packages, intended for use as power operational amplifiers in a wide range of applications including servo amplifiers and power supplies. They are particularly indicated for driving, inductive loads, as motor and finds applications in compact-disc, VCR automotive, etc.

The high gain and high output power capability provide superior performance whatever an operational amplifier/power booster combination is required.



Powerdip (8 + 8)

Minidip Plastic

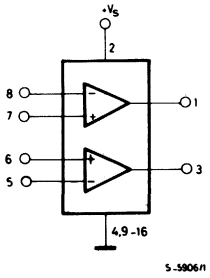
ORDERING NUMBERS:

L2720 L2722

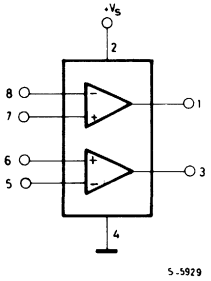
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	28	V
V_s	Peak supply voltage (50ms)	50	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	$\pm V_s$	
I_o	DC output current	1	A
I_p	Peak output current (non repetitive)	1.5	A
P_{tot}	Power dissipation at T_{amb} = 80°C (**L2720**), T_{amb} = 50°C (**L2722**)	1	W
	T_{case} = 75°C (**L2720**)	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

BLOCK DIAGRAMS



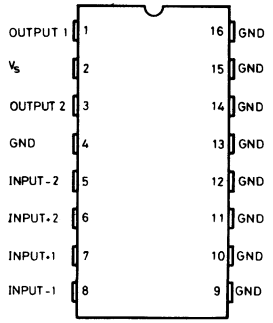
L2720



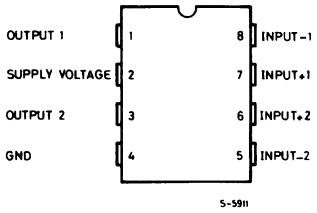
L2722

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

CONNECTION DIAGRAMS
(Top view)

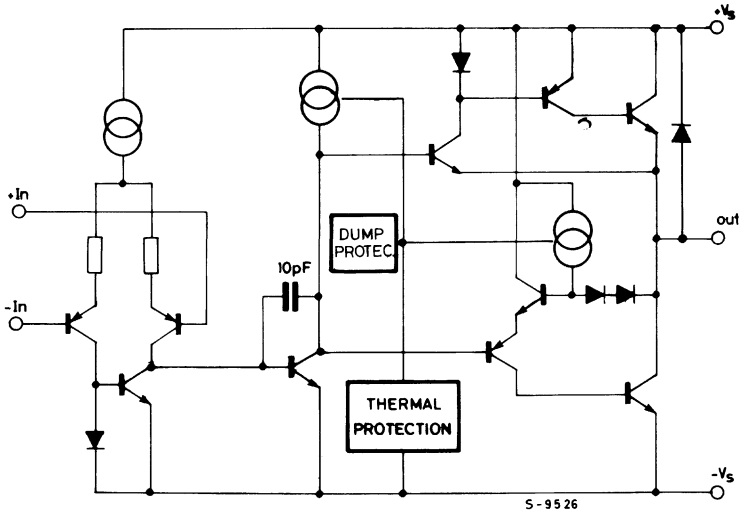


L2720



L2722

SCHEMATIC DIAGRAM (one only)



THERMAL DATA

			Powerdip	Minidip
$R_{th\ j\text{-}case}$	Thermal resistance junction-pins	max	15°C/W	*70°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70°C/W	100°C/W

* Thermal resistance junction-pin 4

ELECTRICAL CHARACTERISTICS ($V_s = 24V$, $T_{amb} = 25°C$ unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_s	Single supply voltage			4		28	V
V_s	Split supply voltage			± 2		± 14	V
I_s	Quiescent drain current	$V_o = \frac{V_s}{2}$	V_s = 24V		10	15	mA
			V_s = 8V		9	15	mA
I_b	Input bias current				0.2	1	μA
V_{os}	Input offset voltage					15	mV
I_{os}	Input offset current				10	50	nA
SR	Slew rate				2		V/μs
B	Gain-bandwidth product				1.2		MHz
R_I	Input resistance			500			KΩ
G_V	O.L. voltage gain	f = 100Hz		70	80		dB
		f = 1KHz			60		dB
e_N	Input noise voltage	B = 22Hz to 22KHz			10		μV
I_N	Input noise current				200		pA
CMR	Common Mode rejection	f = 1KHz		66	84		dB
SVR	Supply voltage rejection	f = 100Hz R_G = 10KΩ V_R = 0.5V	V_s = 24V V_s = ±12V V_s = ± 6V	54	70 75 81		dB dB dB
$V_{DROP\ (HIGH)}$		V_s = ±2.5V to ±12V	I_p = 100mA		0.7		V
			I_p = 500mA		1.0	1.5	V
$V_{DROP\ (LOW)}$			I_p = 100mA		0.3		V
			I_p = 500mA		0.5	1.0	V
C_s	Channel separation	f = 1KHz R_L = 10Ω G_V = 30dB	V_s = 24V		60		dB
			V_s = 6V		60		dB
T_{sd}	Thermal shutdown junction temperature				145		°C

Fig. 1 - Quiescent current vs. supply voltage

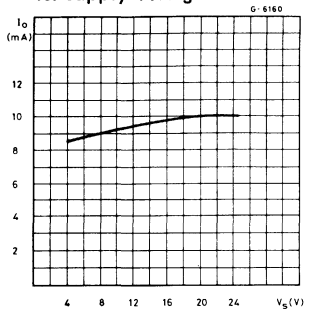


Fig. 2 - Open loop gain vs. frequency

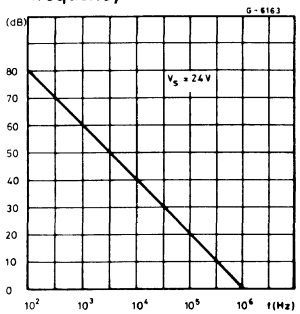


Fig. 3 - Common mode rejection vs. frequency

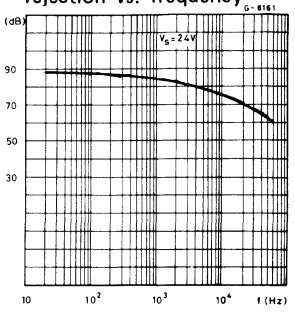


Fig. 4 - Output swing vs. load current (V_s = ± 5V)

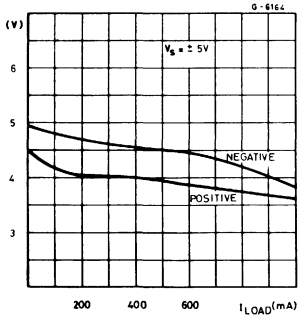


Fig. 5 - Output swing vs. load current (V_s = ± 12V)

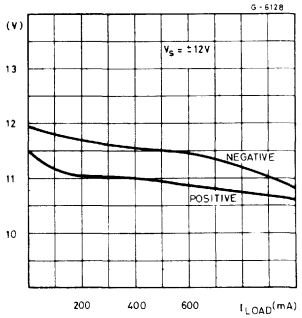


Fig. 6 - Supply voltage rejection vs. frequency

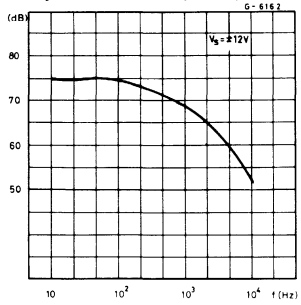
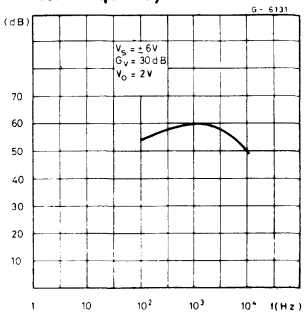


Fig. 7 - Channel separation vs. frequency

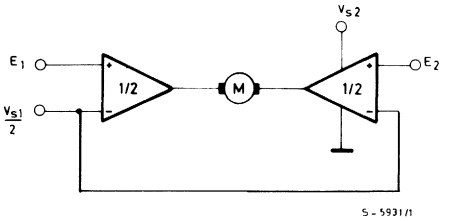


APPLICATION SUGGESTION

In order to avoid possible instability occurring into final stage the usual suggestions for the linear power stages are useful, as for instance:

- layout accuracy;
- A 100nF capacitor corrected between supply pins and ground;
- boucherot cell (0.1 to 0.2μF + 1Ω series) between outputs and ground or across the load.

Fig. 8 - Bidirectional DC motor control with μP compatible inputs



V_{S1} = logic supply voltage

Must be $V_{S2} > V_{S1}$

E1, E2 = logic inputs

Fig. 9 - Servocontrol for compact-disc

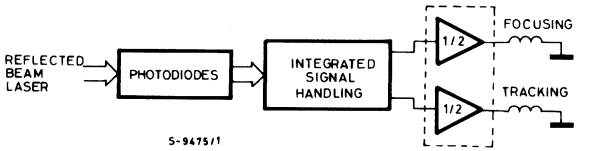


Fig. 10 - Capstan motor control in video recorders

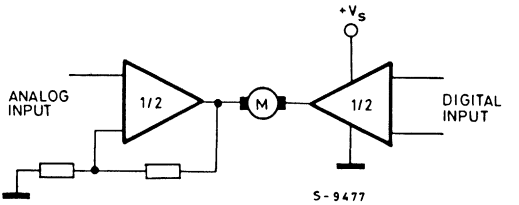
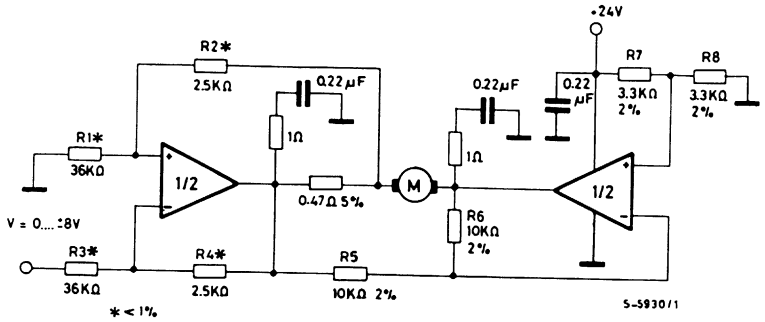


Fig. 11 - Motor current control circuit



Note: The input voltage level is compatible with L291 (5-BIT D/A converter)

Fig. 12 - Bidirectional speed control of DC motors.

For circuit stability ensure that $R_X > \frac{2R3 \circ R1}{R_M}$ where R_M = internal resistance of motor. The voltage available at the terminals of the motor is $V_M = 2\left(V_I - \frac{V_s}{2}\right) + |R_o|.\ I_M$ where $|R_o| = \frac{2R \circ R1}{R_X}$ and I_M is the motor current.

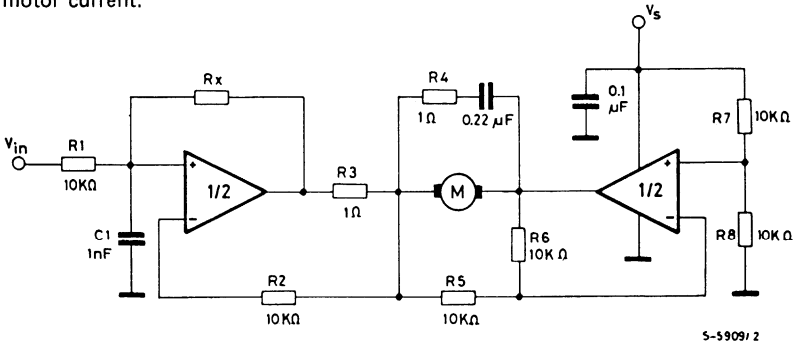
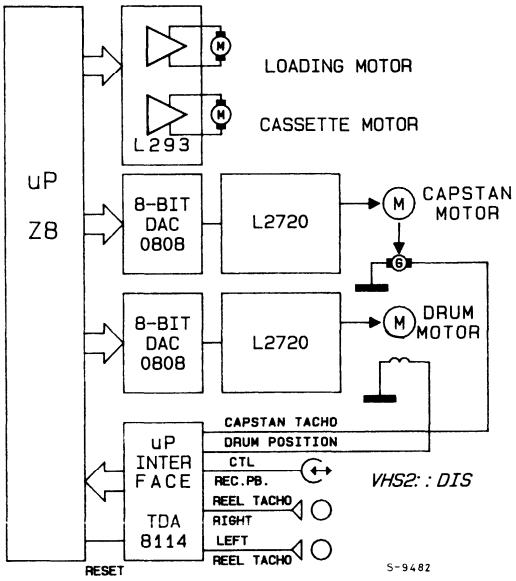


Fig. 13 - VHS-VCR Motor control circuit



L4705
L4785
L4710

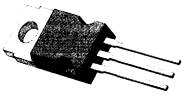
PRELIMINARY DATA

VERY LOW DROP VOLTAGE REGULATORS

- INPUT/OUTPUT DROP TYP. 0.6V
- 500mA OUTPUT CURRENT
- 80V LOAD DUMP PROTECTION
- -80V TRANSIENT PROTECTION
- REVERSE POLARITY PROTECTION
- OVERVOLTAGE PROTECTION
- OUTPUT CURRENT LIMITING
- THERMAL SHUTDOWN

L4700 series voltage regulators feature a very low voltage drop, an output current of 500mA and protection against load dump transients of ± 80V. Available in 5V, 8.5V and 10V (± 4%) versions, these regulators also include reverse polarity protection, overvoltage protection, output current limiting and a thermal shutdown circuit.

L4700 series regulators are specially designed for automotive and industrial applications where the electrical environment is very demanding and low voltage drop is required. For example, the L4705 can be used in 5V automotive applications, continuing to function even when the battery voltage falls to 6V, a common event during starting. Moreover, the L4705 is fully protected against the transients, overvoltages and polarity reversal encountered on the battery rail.



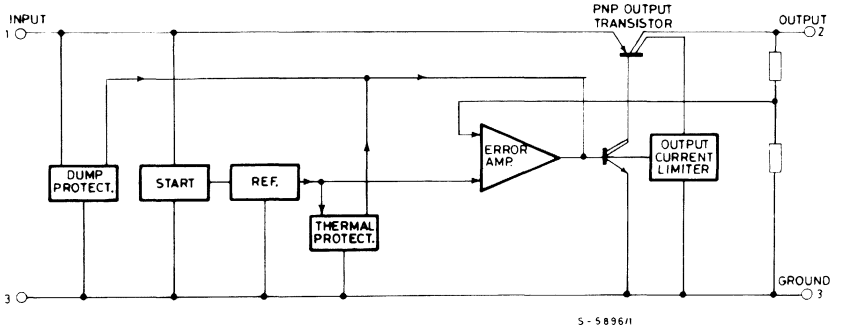
TO-220

ORDERING NUMBER: L4705CV (5V)
L4785CV (8.5V)
L4710CV (10V)

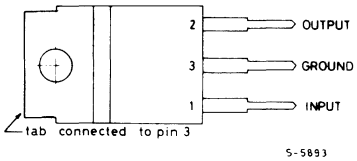
ABSOLUTE MAXIMUM RATINGS

V_i	Forward input voltage	35	V
V_i	Reverse input voltage	-18	V
V_t	Positive transient peak voltage (t = 300 ms)	+ 80	V
V_t	Negative transient peak voltage (t = 100 ms)	-80	V
T_{op}	Operating junction temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

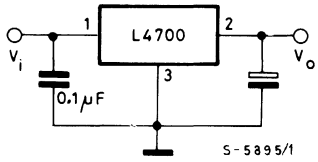
BLOCK DIAGRAM



CONNECTION DIAGRAM (top view)



TEST AND APPLICATION CIRCUIT



The output capacitor is required for stability. Though the 47μF shown is the minimum recommended value, actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) also factors in the IC stability. Since ESR varies from one brand to the next, some bench work may be required to determine the minimum capacitor value to use in production. Worst-case is usually determined at the minimum ambient temperature and maximum load expected.

Output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltages during brief conditions of negative input transients that might be characteristic of a particular system.

Capacitors must also be rated at all ambient temperature expected in the system. Many aluminum type electrolytics will freeze at temperatures less than -30°C, reducing their effective capacitance to zero. To maintain regulator stability down to -40°C, capacitors rated at that temperature (such as tantalums) must be used.

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

ELECTRICAL CHARACTERISTICS (V_i = 14.4V, T_j = 25°C)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_o	Output voltage	I_o = 5 mA to 500 mA	4.80	5	5.20	V
			8.16	8.5	8.84	V
			9.6	10	10.4	V
V_i	Operating input voltage	(*) see note			28	V
$\Delta V_o/V_o$	Line regulation	V_i = 11 to 26V I_o = 5 mA		1		mV/V
$\Delta V_o/V_o$	Load regulation	I_o = 5 to 500 mA		3		mV/V
$V_i - V_o$	Dropout voltage	I_o = 500 mA		0.6	0.9	V
I_q	Quiescent current	I_o = 0 mA		6		mA
		I_o = 150 mA		20	40	mA
		I_o = 500 mA		130		mA
$\frac{\Delta V_o}{\Delta T \cdot V_o}$	Temperature output voltage drift			0.1		$\frac{mV}{°C \cdot V}$
SVR	Supply voltage rejection	I_o = 350 mA f = 120 Hz C_o = 100 μF $V_i = V_o + 3V + 2V_{pp}$		55		dB
I_{sc}	Output short circuit current			800		mA

(*) For a DC input voltage 28V < V_i < 35V the device is not operating.

Fig. 1 - Dropout voltage vs. output current

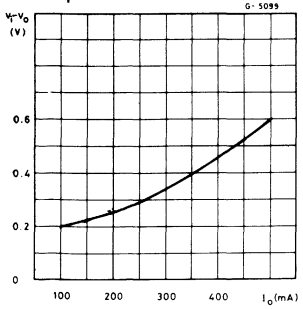


Fig. 2 - Quiescent current vs. output current

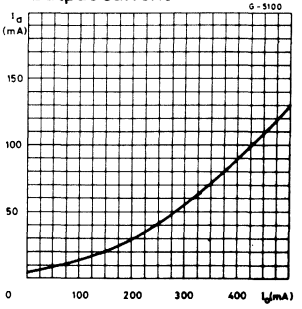
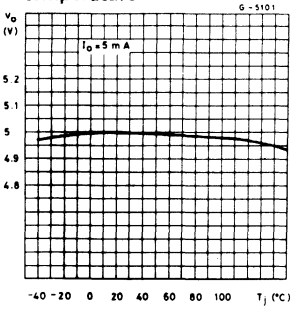


Fig. 3 - Output voltage vs. temperature



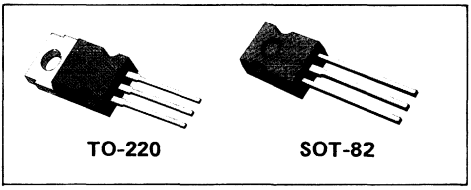
PRELIMINARY DATA

VERY LOW DROP VOLTAGE REGULATORS

- INPUT/OUTPUT DROP TYP. 0.4V
- 400mA OUTPUT CURRENT
- LOW QUIESCENT CURRENT
- 60V LOAD DUMP PROTECTION
- -60V TRANSIENT PROTECTION
- REVERSE POLARITY PROTECTION
- OVERVOLTAGE PROTECTION
- FOLDBACK CURRENT LIMITING
- THERMAL SHUTDOWN

L4800 series devices are voltage regulators with a very low voltage drop (typically 0.4V at full rated current), output current up to 400mA, low quiescent current and comprehensive on-chip protection. These devices are protected against load dump transients of ± 60V, input overvoltage, polarity reversal and overheating. A foldback current limiter protects against load short circuits. Available in 5V, 8.5V, 10V and 12V versions (all ± 4%), these regulators are designed for automotive, industrial and consumer applications where low consumption is particularly important.

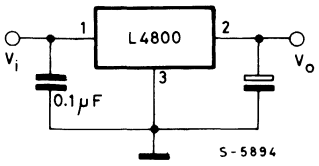
In automotive applications the L4805 is ideal for 5V logic supplies because it functions with battery voltages as low as 5.5V. In battery backup and standby applications the low consumption of these devices extends battery life.



ABSOLUTE MAXIMUM RATINGS

V_i	Forward input voltage	26	V
V_i	Reverse input voltage	-18	V
V_t	Positive transient peak voltage (t = 300 ms)	+60	V
V_t	Negative transient peak voltage (t = 100 ms)	-60	V
T_{op}	Operating junction temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

TEST AND APPLICATION CIRCUIT

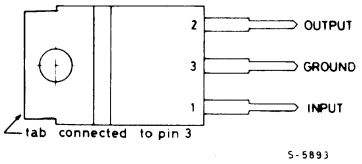


The output capacitor is required for stability. Though the 100µF shown is the minimum recommended value, actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) also factors in the IC stability. Since ESR varies from one brand to the next, some bench work may be required to determine the minimum capacitor value to use in production. Worst-case is usually determined at the minimum ambient temperature and maximum load expected.

Output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltages during brief conditions of negative input transients that might be characteristic of a particular system.

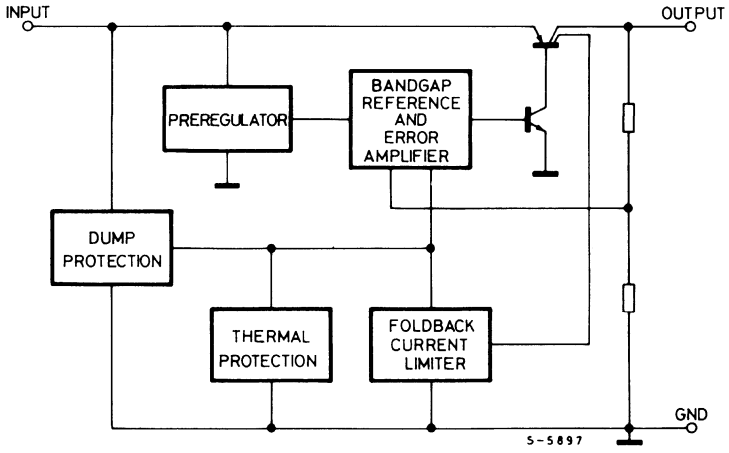
Capacitors must also be rated at all ambient temperature expected in the system. Many aluminum type electrolytics will freeze at temperatures less than -30°C, reducing their effective capacitance to zero. To maintain regulator stability down to -40°C, capacitors rated at that temperature (such as tantalums) must be used.

CONNECTION DIAGRAM (top view)



Ordering Numbers		Output Voltage
TO-220	SOT-82	
L4805CV	L4805CX	5V
L4885CV	L4885CX	8.5V
L4810CV	L4810CX	10V
L4812CV	L4812CX	12V

BLOCK DIAGRAM



THERMAL DATA

			SOT-82	TO-220
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	8°C/W	3°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100°C/W	50°C/W

ELECTRICAL CHARACTERISTICS (V_i = 14.4V, T_j = 25°C)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_o	Output voltage	I_o = 5 mA to 400 mA	4.80	5	5.20	V
			8.16	8.5	8.84	V
			9.6	10	10.4	V
			11.5	12	12.5	V
V_i	Operating input voltage				26	V
$\Delta V_o/V_o$	Line regulation	V_i = 13 to 26V I_o = 5 mA		1	10	mV/V
$\Delta V_o/V_o$	Load regulation	I_o = 5 to 400 mA		3	15	mV/V
V_i-V_o	Dropout voltage	I_o = 400 mA		0.4	0.7	V
		I_o = 150 mA		0.2	0.4	V
I_q	Quiescent current	I_o = 0 mA		0.8	3	mA
		I_o = 150 mA		16	45	mA
		I_o = 400 mA		80	100	mA
$\frac{\Delta V_o}{\Delta T \cdot V_o}$	Temperature output voltage drift			0.1		$\frac{mV}{°C \cdot V}$
SVR	Supply voltage rejection	I_o = 350 mA f = 120 Hz C_o = 100 μF V_i=V_o+3V+2V_{pp}		60		dB
I_o	Max output current			750		mA
I_{sc}	Output short circuit current (fold back condition)			220		mA

Fig. 1 - Dropout voltage vs. output current

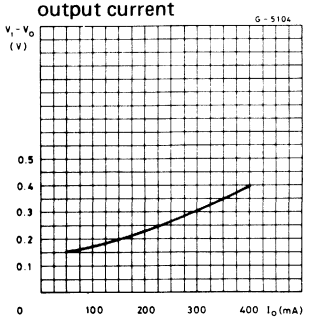


Fig. 2 - Quiescent current vs. output current

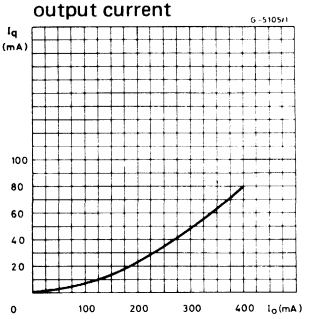


Fig. 3 - Output voltage vs. temperature

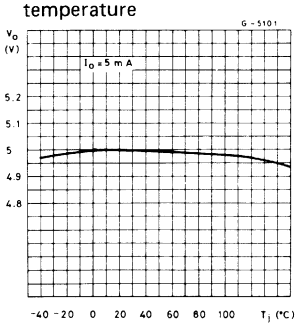


Fig. 4 - Foldback current limiting (L4805)

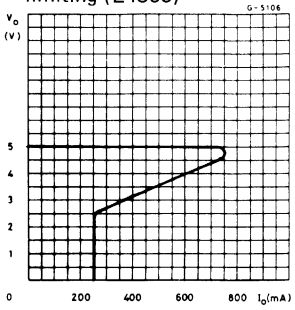
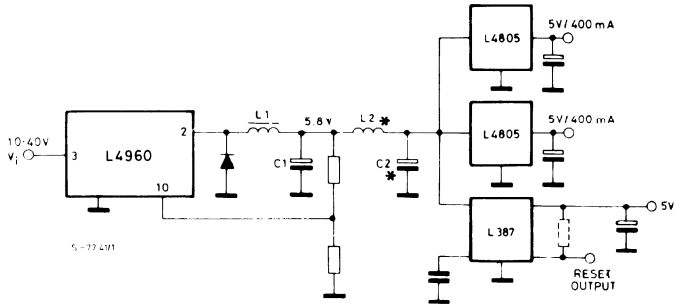


Fig. 5 - Preregulator for distributed supplies



* L2 and C2 are necessary to reduce the switching frequency spikes.

L4901

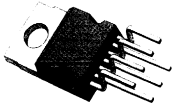
PRELIMINARY DATA

DUAL 5V REGULATOR WITH RESET

- OUTPUT CURRENTS: I_{01} = 300mA
  I_{02} = 400mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- LOW QUIESCENT CURRENT (INPUT 1)
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT HIGH
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4901 is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset and data save functions during switch on/off can be realized.



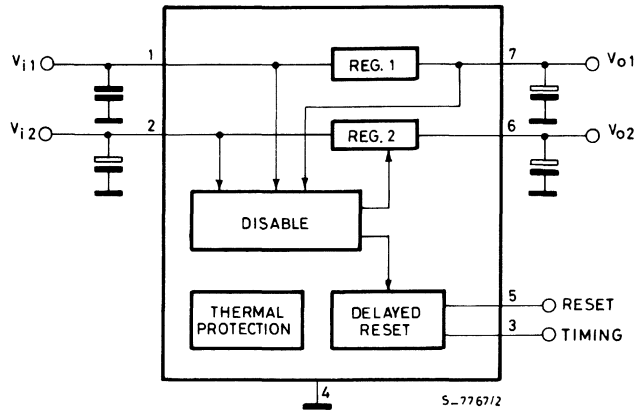
Heptawatt

ORDERING NUMBER: L4901

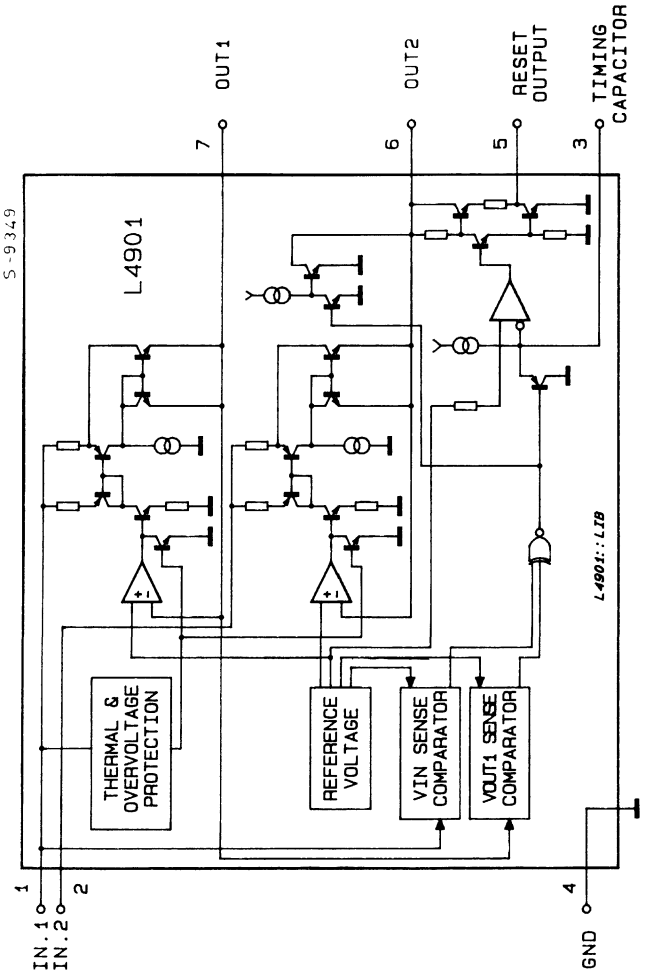
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	24	V
	Transient input overvoltage (t = 40ms)	60	V
I_o	Output current	internally limited	
T_j	Storage and junction temperature	-40 to 150	°C

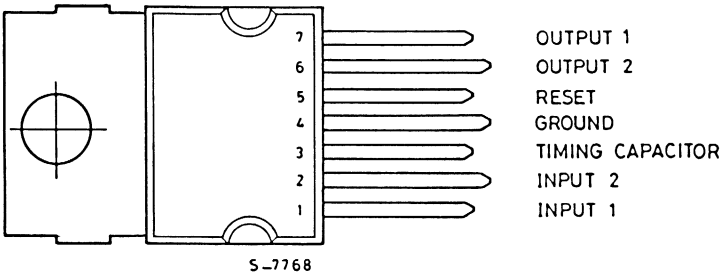
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



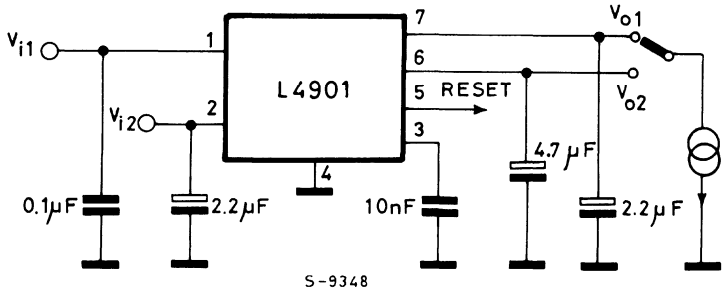
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 300mA regulator input.
2	INPUT 2	400mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 5μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
5	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{5\mu A} \right)$; t_{RD} (ms) = C_t (nF)
6	OUTPUT 2	5V - 400mA regulator output. Enabled if $V_O 1 > V_{RT}$ and $V_{IN2} > V_{IT}$. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
7	OUTPUT 1	5V - 300mA regulator output with low leakage (in switch-OFF condition).

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS (V_{IN} = 14,4V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC operating input voltage				20	V
V_{01}	Output voltage 1	R load 1KΩ	4,95	5.05	5.15	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01}-0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	I_{02} = -5mA		0.1		V
I_{01}	Output current 1	ΔV_{01} = -100mV	300			mA
I_{L01}	Leakage output 1 current	V_{IN} = 0 $V_{01} \leq$ 3V			1	µA
I_{02}	Output current 2	ΔV_{02} = -100mV	400			mA
V_{i01}	Output 1 dropout voltage (*)	I_{01} = 10mA I_{01} = 100mA I_{01} = 300mA		0.7 0.8 1.05	0.8 1 1.25	V V V
V_{IT}	Input threshold voltage		V_{01}+1.2	6.4	V_{01}+1.6	V
V_{ITH}	Input threshold voltage hyst.			250		mV
ΔV_{01}	Line regulation 1	7V < V_{IN} < 18V I_{01} = 5mA		5	50	mV
ΔV_{02}	Line regulation 2	I_{02} = 5mA		5	50	mV
ΔV_{01}	Load regulation 1	V_{IN} = 8V 5mA < I_{01} < 300mA		40	80	mV
ΔV_{02}	Load regulation 2	5mA < I_{02} < 400mA		50	100	mV
I_Q	Quiescent current	0 < V_{IN} < 13V 6.3V < V_{IN} < 13V I_{02} = $I_{01} \leq$ 5mA		4.5 1.6	6 3.5	mA mA
I_{Q1}	Quiescent current 1	6.3V < V_{IN1} < 13V V_{IN2} = 0 $I_{01} \leq$ 5mA I_{02} = 0		0.6	0.9	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RT}	Reset threshold voltage		V_{02}-0.15	4.9	V_{02}-0.05	V
V_{RTH}	Reset threshold hysteresis			50	160	mV
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	6	10	14	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	-20°C ≤ T_{amb} ≤ 140°C	-0.8	0.3	+0.8	mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	-20°C ≤ T_{amb} ≤ 140°C	-0.8	0.3	+0.8	mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R = 0.5V I_o = 100mA	54	84		dB
SVR2	Supply voltage rejection		50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4901 makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with separate inputs plus a reset output for the data save function.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs:

- an input overvoltage
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:

- 5V internal reference without voltage divider between the output and the error comparator;
- very low drop series regulator element utilizing current mirrors;

permit high output impedance and then very low leakage current error even in power down condition.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery. The V_{01}

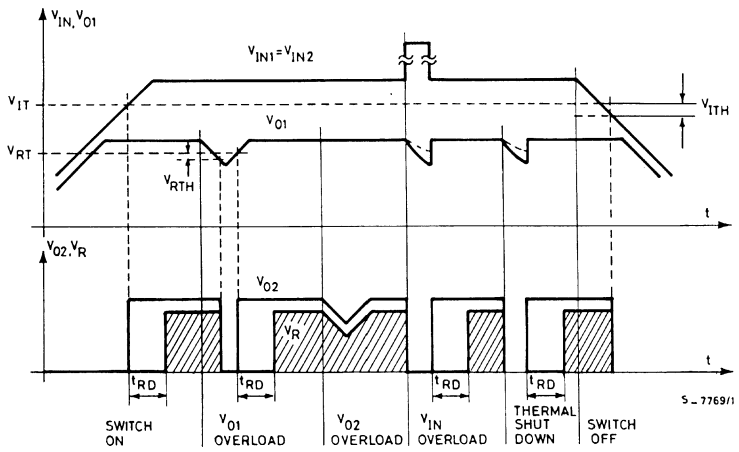
CIRCUIT OPERATION (continued)

regulator also features low consumption (0.6mA typ.) to minimize battery drain in applications where the V_1 regulator is permanently connected to a battery supply.

The V_{02} output can supply other non essential 5V circuits wich may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

Fig. 1



APPLICATION SUGGESTIONS

Fig. 2 shows an application circuit for a μP system typically used in trip computers or in car radios with programmable tuning.

Reg. 1 is permanently connected to a battery and supplies a CMOS time-of-day clock and a CMOS microcomputer chip with volatile memory.

Reg. 2 may be switched OFF when the system is inactive.

Fig. 4 shows the L4901 with a back up battery on the V_{01} output to maintain a CMOS time-of-day clock and a stand by type N-MOS μP. The reset output makes sure that the RAM is forced into the low consumption stand by state, so the access to memory is inhibit and the back up battery voltage cannot drop so low that memory contents are corrupted.

In this case the main on-off switch disconnects both regulators from the supply battery.

The L4901 is also ideal for microcomputer systems using battery backup CMOS static RAMs. As shown in fig. 5 the reset output is used both to disable the μP and, through the address decoder M74HC138, to ensure that the RAMS are disabled as soon as the main supply starts to fall.

Another interesting application of the L4901 is in μP system with shadow memories. (see fig. 6)

When the input voltage goes below V_{IT}, the reset output enables the execution of a routine that saves the machine's state in the shadow RAM (xicor x 2201 for example).

Thanks to the low consumption of the Reg. 1 a 680μF capacitor on its input is sufficient to provide enough energy to complete the operation. The diode on the input guarantees the supply of the equipment even if a short circuit on V_I occurs.

APPLICATION SUGGESTION (continued)

Fig. 2

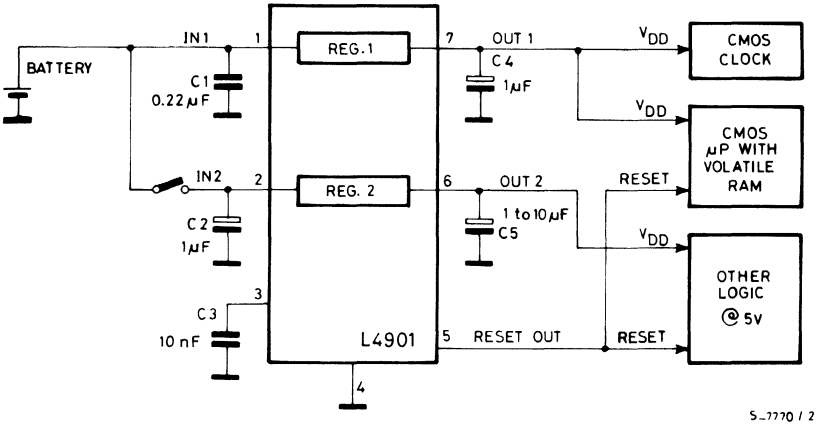
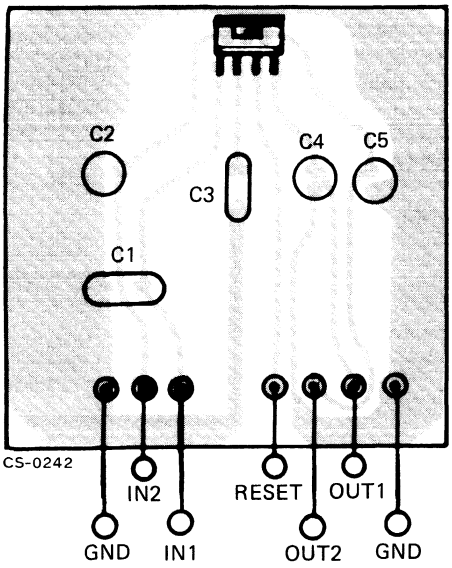


Fig. 3 - P.C. board component layout of fig. 2 (1 : 1 scale)



APPLICATION SUGGESTION (continued)

Fig. 4

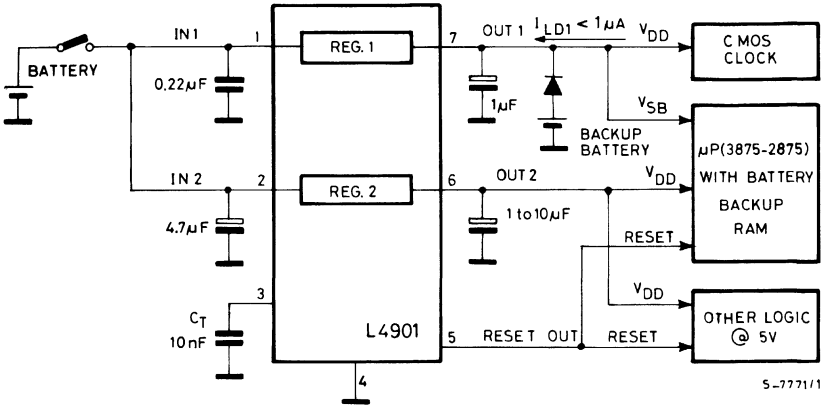
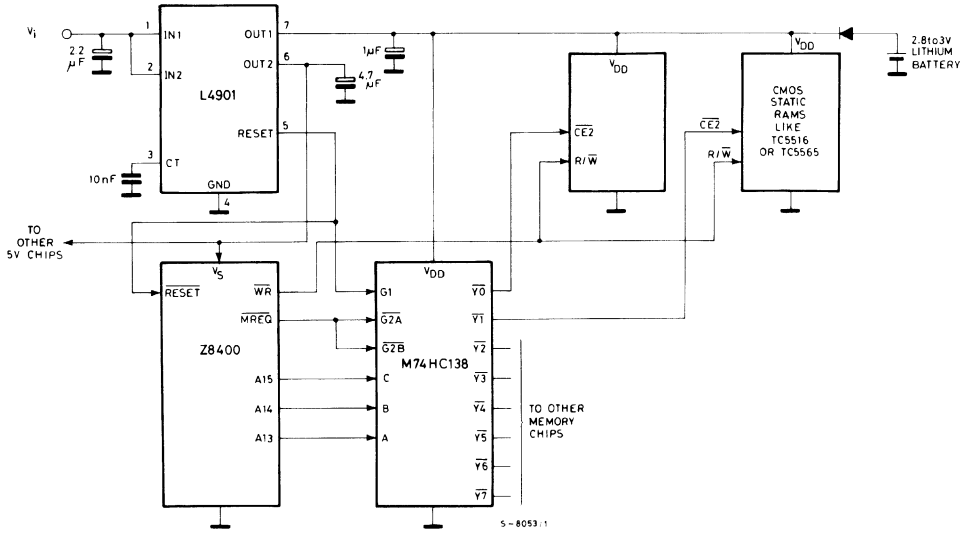


Fig. 5



APPLICATION SUGGESTION (continued)

Fig. 6

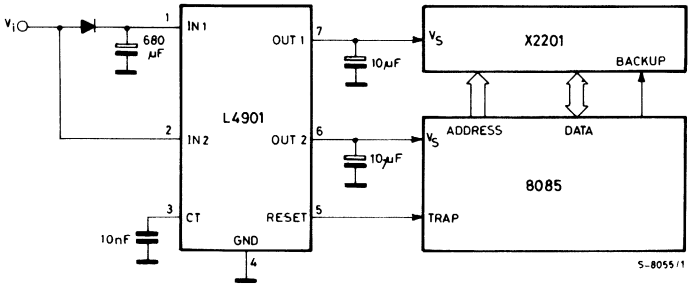


Fig. 7 - Quiescent current (Reg. 1) vs. output current

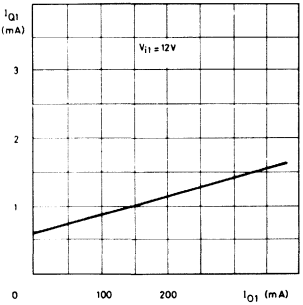


Fig. 8 - Quiescent current (Reg. 1) vs. input voltage

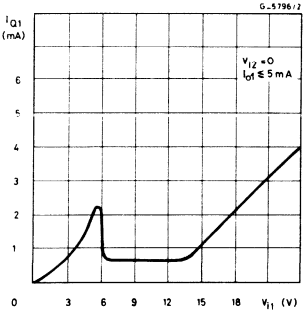


Fig. 9 - Total quiescent current vs. input voltage

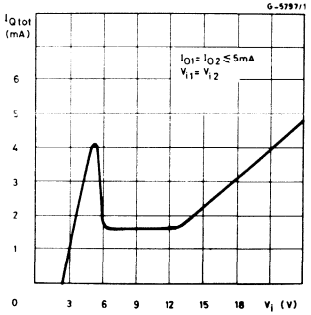


Fig. 10 - Regulator 1 output current and short circuit current vs. input voltage

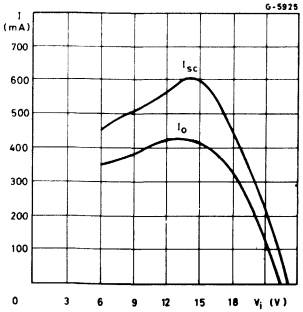


Fig. 11 - Regulator 2 output current and short circuit current vs. input voltage

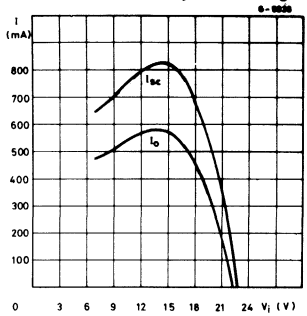
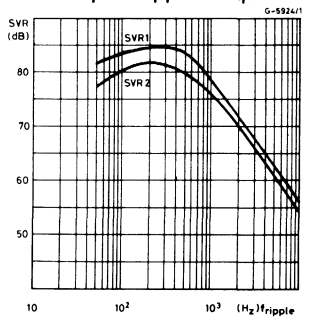


Fig. 12 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence



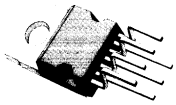
L4902

PRELIMINARY DATA

DUAL 5V REGULATOR WITH RESET AND DISABLE FUNCTIONS

- OUTPUT CURRENTS: I_{01} = 300mA
  I_{02} = 400mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- OUTPUT 2 DISABLE LOGICAL INPUT
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- RESET OUTPUT HIGH
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4902 is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.
Reset and data save functions and remote switch on/off control can be realized.



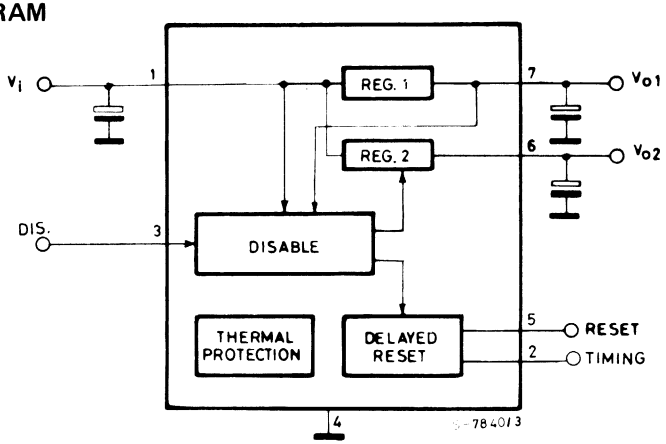
Heptawatt

ORDERING NUMBER: L4902

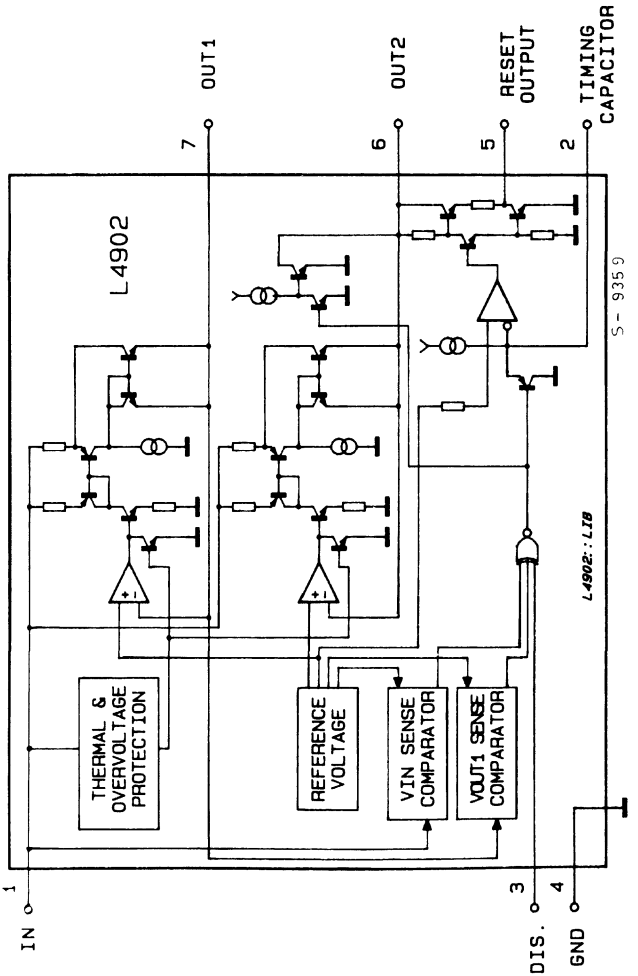
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	24	V
	Transient input overvoltage (t = 40ms)	60	V
I_o	Output current	internally limited	
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

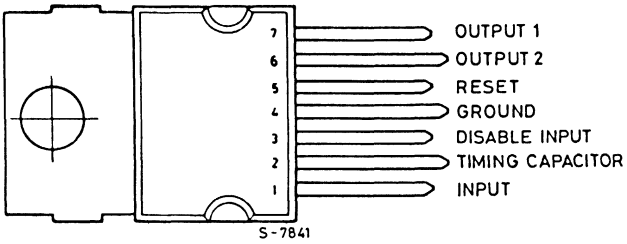
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



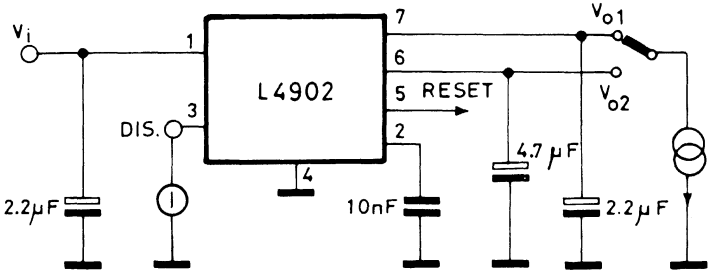
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Regulators common input.
2	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 5μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
3	V_{02} DISABLE INPUT	A high level ($> V_{DT}$) disable output Reg. 2.
4	GND	Common ground.
5	RESET OUTPUT	When pin 2 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{5\mu A}\right)$; t_{RD} (ms) = C_t (nF).
6	OUTPUT 2	5V - 400mA regulator output. Enabled if $V_O 1 > V_{RT}$. DISABLE INPUT $< V_{DT}$ and $V_{IN} > V_{IT}$. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
7	OUTPUT 1	5V - 300mA. Low leakage (in switch-OFF condition) output.

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS (V_{IN} = 14.4V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC operating input voltage				20	V
V_{O1}	Output voltage 1	R load 1KΩ	4.95	5.05	5.15	V
V_{O2H}	Output voltage 2 HIGH	R load 1KΩ	V_{O1}-0.1	5	V_{O1}	V
V_{O2L}	Output voltage 2 LOW	I_{O2} = -5mA		0.1		V
I_{O1}	Output current 1 max.	ΔV_{O1} = -100mV	300			mA
I_{LO1}	Leakage output 1 current	V_{IN} = 0 $V_{O1} \leq$ 3V			1	µA
I_{O2}	Output current 2 max.	ΔV_{O2} = -100mV	400			mA
V_{iO1}	Output 1 dropout voltage (*)	I_{O1} = 10mA I_{O1} = 100mA I_{O1} = 300mA		0.7 0.8 1.05	0.8 1 1.25	V V V
V_{IT}	Input threshold voltage		V_{O1}+1.2	6.4	V_{O1}+1.6	V
V_{iTH}	Input threshold voltage hysteresis			250		mV
ΔV_{O1}	Line regulation 1	7V < V_{IN} < 18V I_{O1} = 5mA		5	50	mV
ΔV_{O2}	Line regulation 2	I_{O2} = 5mA		5	50	mV
ΔV_{O1}	Load regulation 1	V_{IN} = 8V 5mA < I_{O1} < 300mA		40	80	mV
ΔV_{O2}	Load regulation 2	5mA < I_{O2} < 400mA		50	100	mV
I_Q	Quiescent current	0 < V_{IN} < 13V 6.3V < V_{IN} < 13V V_{O2} LOW 6.3V < V_{IN} < 13V V_{O2} HIGH I_{O1} = $I_{O2} \leq$ 5mA		4.5 2.7 1.6	6 4 3.5	mA mA mA
V_{RT}	Reset threshold voltage		V_{O2}-0.15	4.9	V_{O2}-0.05	V
V_{RTH}	Reset threshold hysteresis			50	160	mV

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	6	10	14	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
V_{DT}	V_{02} disable threshold voltage			1.25	2.4	V
I_D	V_{02} disable input current	$V_D \leq 0.4V$ $V_D \geq 2.4V$		-100 -2		μA μA
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 140°C$	-0.8	0.3	0.8	mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 140°C$	-0.8	0.3	0.8	mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R = 0.5V I_o = 100mA	54	84		dB
SVR2	Supply voltage rejection		50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4902 makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with common inputs plus a reset output for the data save function and a Reg. 2 disable input.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs:
- a high level ($> V_{DT}$) is applied on pin 3;
- an input overvoltage;
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:
- 5V internal reference without voltage divider between the output and the error comparator
- very low drop series regulator element utilizing current mirrors

permit high output impedance and then very low leakage current even in power down condition.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery.

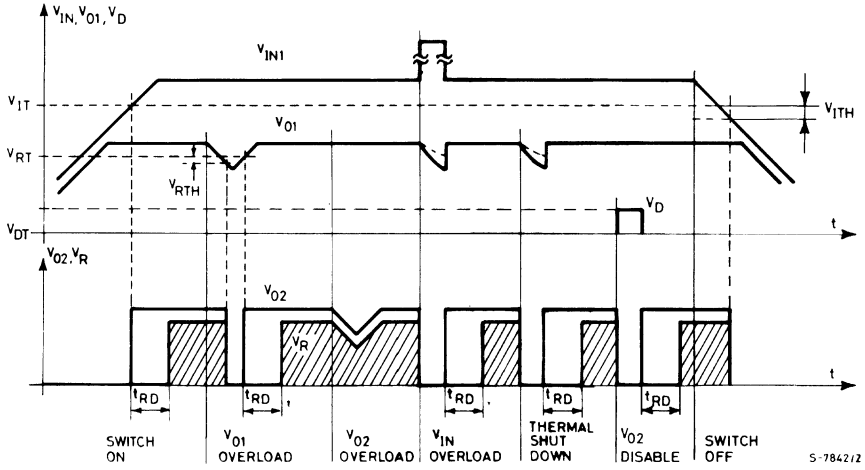
CIRCUIT OPERATION (continued)

The V_{02} output can supply other non essential 5V circuits wich may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

The disable function can be used for remote on/off control of circuits connected to the V_{02} output.

Fig. 1



APPLICATION SUGGESTION

Fig. 2 illustrates how the L4902's disable input may be used in a CMOS μComputer application.

The V_{01} regulator (low consumption) supply permanently a CMOS time of day clock and a CMOS μcomputer chip with volatile memory. V_{02} output, supplying non-essential circuits, is turned OFF under control of a μP unit.

Configurations of this type are used in products where the OFF switch is part of a keyboard scanned by a micro which operates continuously even in the OFF state.

Another application for the L4902 is supplying a shadow-ram microcomputer chip (SGS M38SH72 for exemple) where a fast NV memory is backed up on chip by a EEPROM when a low level on the reset output occurs.

By adding two CMOS-SCHMIDT-TRIGGER and few external components, also a watch dog function may be realized (see fig. 5). During normal operation the microsystem supplies a periodical pulse waveform; if an anomalous condition occours (in the program or in the system), the pulses will be absent and the disable input will be activated after a settling time determined by R1 C1. In this condition all the circuitry connected to V_{02} will be disabled, the system will be restarted with a new reset front.

The disable of V_{02} prevent spurious operation during microprocessor malfunctioning.

APPLICATION SUGGESTION (continued)

Fig. 2

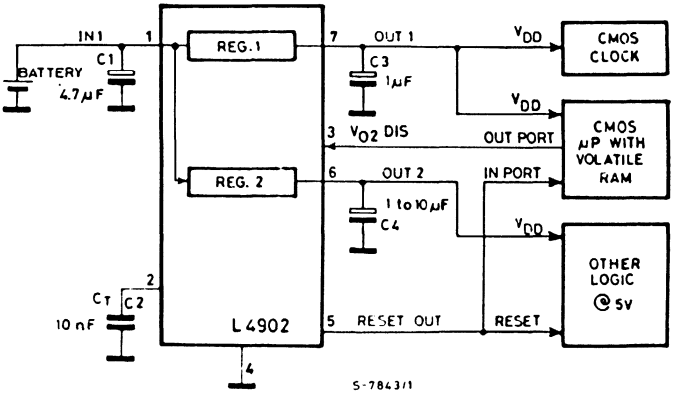
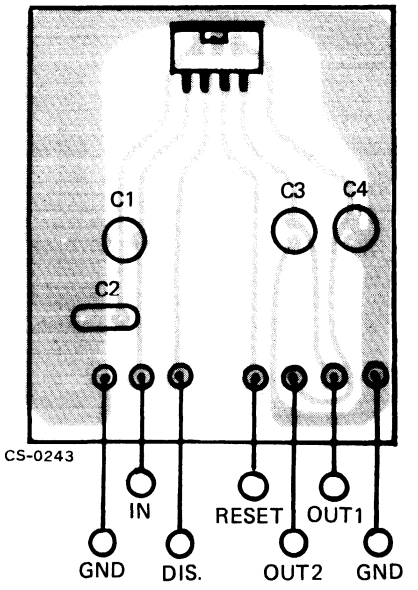


Fig. 3 - P.C. board and component layout of the circuit of Fig. 2 (1 : 1 scale)



APPLICATION SUGGESTION (continued)

Fig. 4

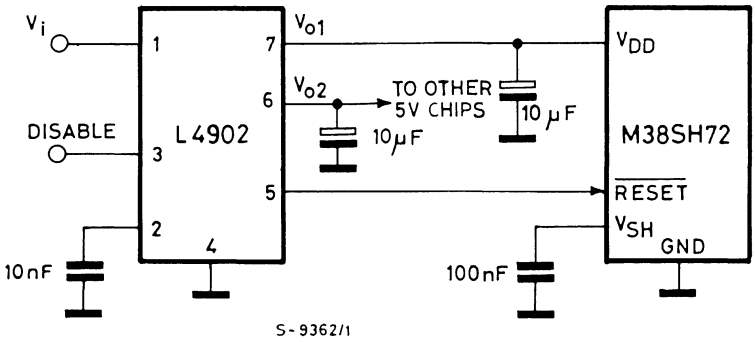
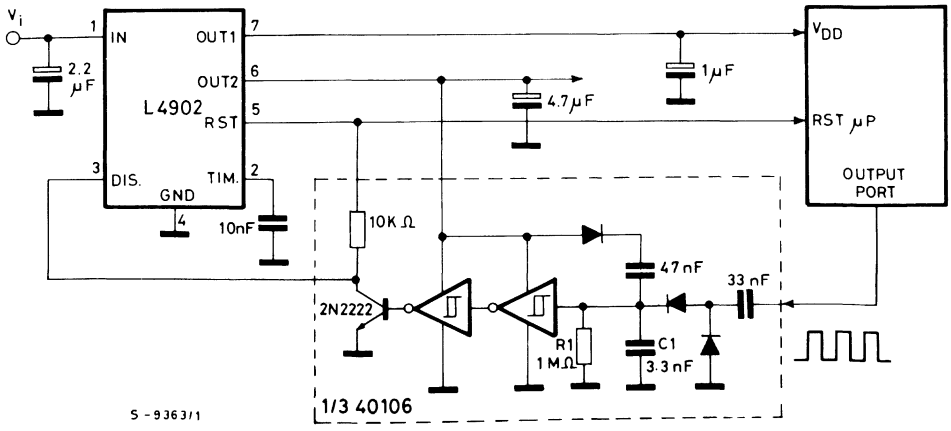


Fig. 5



APPLICATION SUGGESTION (continued)

Fig. 6 - Quiescent current vs. output current

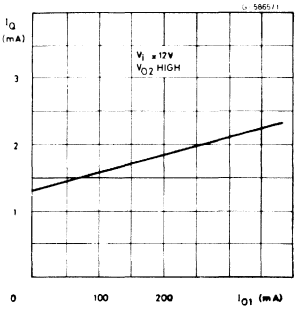


Fig. 7 - Quiescent current vs. input voltage

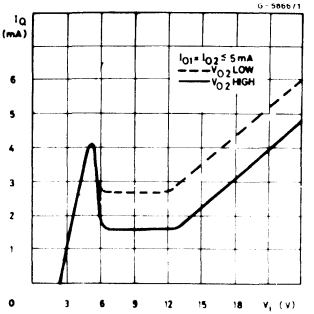


Fig. 8 - Regulator 1 output current and short circuit current vs. input voltage

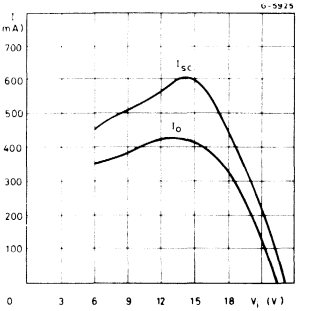


Fig. 9 - Regulator 2 output current and short circuit current vs. input voltage

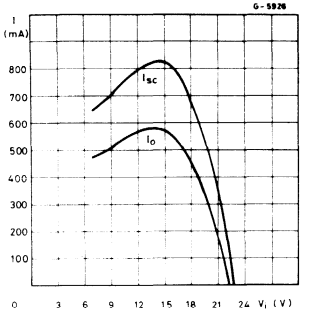
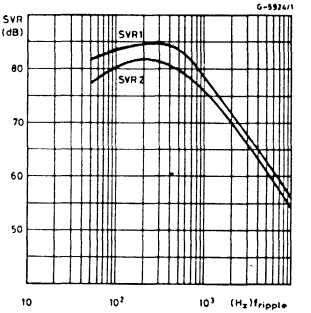


Fig. 10 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence



L4903

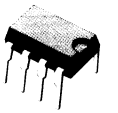
ADVANCE DATA

DUAL 5V REGULATOR WITH RESET AND DISABLE FUNCTIONS

- OUTPUT CURRENTS: I_{01} = 50mA
  I_{02} = 100mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- OUTPUT 2 DISABLE LOGICAL INPUT
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT LOW
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4903 is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset, data save functions and remote switch on/off control can be realized.



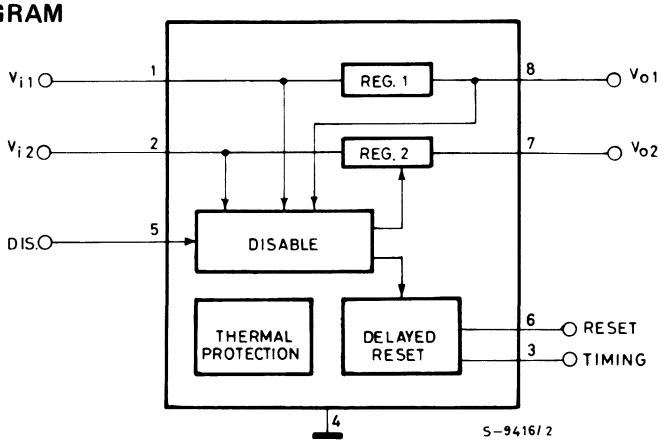
Minidip Plastic

ORDERING NUMBER: L4903

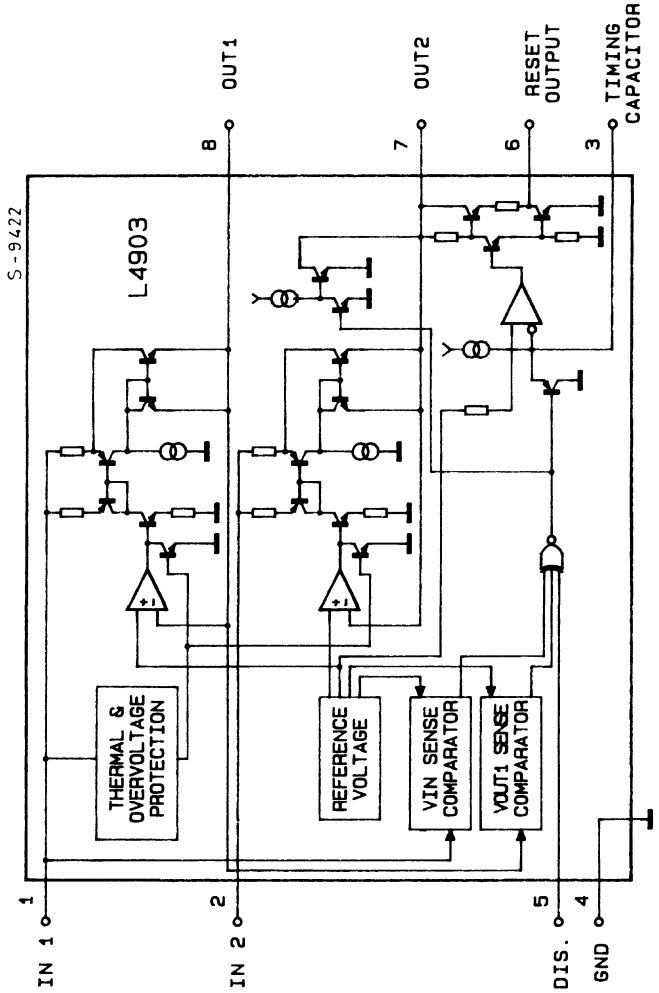
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	24	V
V_t	Transient input overvoltage (t = 40ms)	60	V
P_{tot}	Power dissipation at T_{amb} = 50°C	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

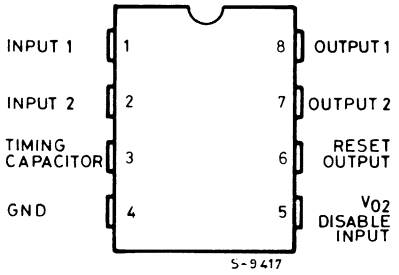
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



PIN FUNCTIONS

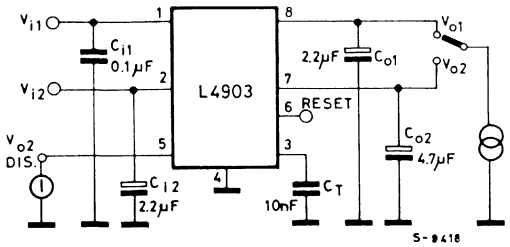
N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 50mA regulator input.
2	INPUT 2	100mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 5μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
5	V_{02} DISABLE INPUT	A high level ($> V_{DT}$) disable output Reg. 2.
6	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched low. Therefore $t_{RD} = C_t (\frac{5V}{5\mu A})$; t_{RD} (ms) = C_t (nF).
7	OUTPUT 2	5V - 100mA regulator output. Enabled if $V_O 1 > V_{RT}$. DISABLE INPUT $< V_{DT}$ and $V_{IN\,2} > V_{IT}$. If Reg. 2 is switched OFF the C_{02} capacitor is discharged.
8	OUTPUT 1	5V - 50mA regulator output with low leakage in switch-OFF condition.

THERMAL DATA

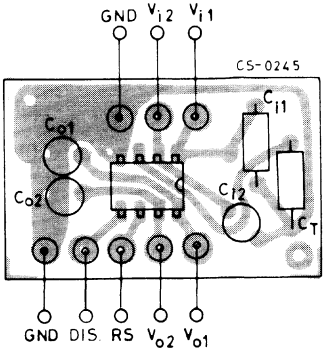
$R_{th\,j\text{-}pin}$	Thermal resistance junction-pin 4	max	70	°C/W
$R_{th\,j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

L4903

TEST CIRCUIT



P.C. board and components layout of the test circuit (1 : 1 scale)



ELECTRICAL CHARACTERISTICS (V_{IN} = 14,4V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC operating input voltage				20	V
V_{01}	Output voltage 1	R load 1KΩ	4.95	5.05	5.15	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01}-0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	I_{02} = -5mA		0.1		V
I_{01}	Output current 1 max. (*)	ΔV_{01} = -100mV	50			mA
I_{L01}	Leakage output 1 current	V_{IN} = 0 $V_{01} \leq$ 3V			1	µA
I_{02}	Output current 2 max. (*)	ΔV_{02} = -100mV	100			mA
V_{i01}	Output 1 dropout voltage (*)	I_{01} = 10mA I_{01} = 50mA		0.7 0.75	0.8 0.9	V V
V_{IT}	Input threshold voltage		V_{01}+1.2	6.4	V_{01}+1.6	V
V_{ITH}	Input threshold voltage hysteresis			250		mV
ΔV_{01}	Line regulation 1	7V < V_{IN} < 18V I_{01} = 5mA		5	50	mV
ΔV_{02}	Line regulation 2	I_{02} = 5mA		5	50	mV
ΔV_{01}	Load regulation 1	V_{IN1} = 8V 5mA < I_{01} < 50mA		5	20	mV
ΔV_{02}	Load regulation 2	5mA < I_{02} < 100mA		10	50	mV
I_Q	Quiescent current	0 < V_{IN} < 13V 6.3V < V_{IN} < 13V V_{02} LOW 6.3V < V_{IN} < 13V V_{02} HIGH I_{01} = $I_{02} \leq$ 5mA		4.5 2.7 1.6	6 4 3.5	mA mA mA
I_{Q1}	Quiescent current 1	6.3V < V_{IN1} < 13V V_{IN2} = 0 I_{01} < 5mA I_{02} = 0		0.6	0.9	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RT}	Reset threshold voltage		V_{02}-0.4	4.7	V_{02}-0.2	V
V_{RTH}	Reset threshold hysteresis			50	160	mV
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	6	10	14	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
V_{DT}	V_{02} disable threshold voltage			1.25	2.4	V
I_D	V_{02} disable input current	$V_D \leq 0.4V$ $V_D \geq 2.4V$		-100 -2		μA μA
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 140°C$	-0.8	0.3	0.8	mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 140°C$	-0.8	0.3	0.8	mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R = 0.5V I_o = 50mA	54	84		dB
SVR2	Supply voltage rejection	I_o = 100mA	50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current conditions.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4903 makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with separate inputs plus a reset output for the data save function and Reg. 2 disable input.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) goes low after a programmable time T_{RD} (timing capacitor).

V_{02} is switched at low level and V_R at high level when one of the following conditions occurs:

- a high level ($> V_{DT}$) is applied on pin 5;
- an input overvoltage;
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:

- 5V internal reference without voltage divider between the output and the error comparator
- very low drop series regulator element utilizing current mirrors

permit high output impedance and then very low leakage current even in power down conditions.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery.

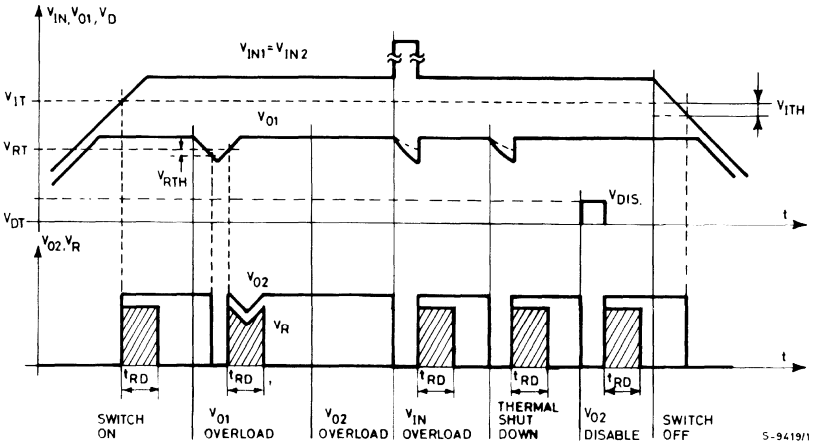
CIRCUIT OPERATION (continued)

The V_{02} output can supply other non essential 5V circuits wich may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

The disable function can be used for remote on/off control of circuits connected to the V_{02} output.

Fig. 1



APPLICATION SUGGESTION

Fig. 2 illustrates how the L4903's disable input may be used in a CMOS μComputer application.

The V_{01} regulator (low consumption) supply permanently a CMOS time of day clock and a CMOS μcomputer chip with volatile memory. V_{02} output, supplying non-essential circuits, is turned OFF under control of a μP unit.

Configurations of this type are used in products where the OFF switch is part of a keyboard scanned by a micro which operates continuously even in the OFF state.

Fig. 2

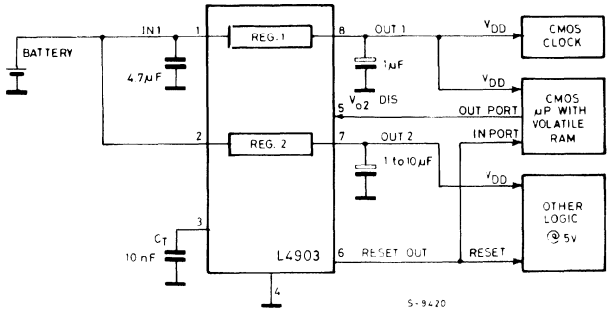


Fig. 3 - Quiescent current (Reg. 1) vs. output current

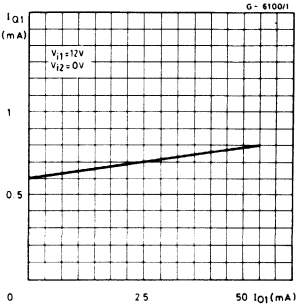


Fig. 4 - Quiescent current (Reg. 1) vs. input voltage

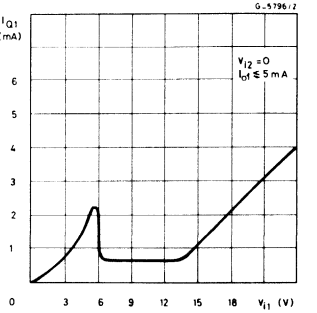


Fig. 5 - Total quiescent current vs. input voltage

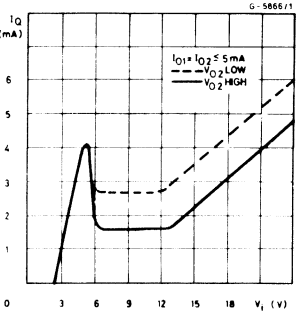
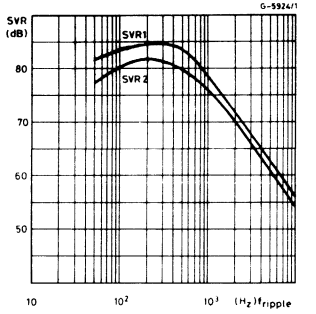


Fig. 6 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence



L4904

ADVANCE DATA

DUAL 5V REGULATOR WITH RESET

- OUTPUT CURRENTS: I_{01} = 50mA
  I_{02} = 100mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- LOW QUIESCENT CURRENT (INPUT 1)
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT HIGH
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4904 is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset and data save functions during switch on/off can be realized.

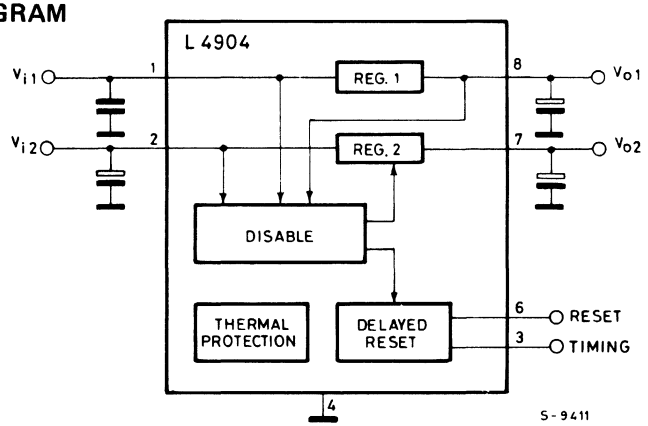
Minidip Plastic

ORDERING NUMBER: L4904

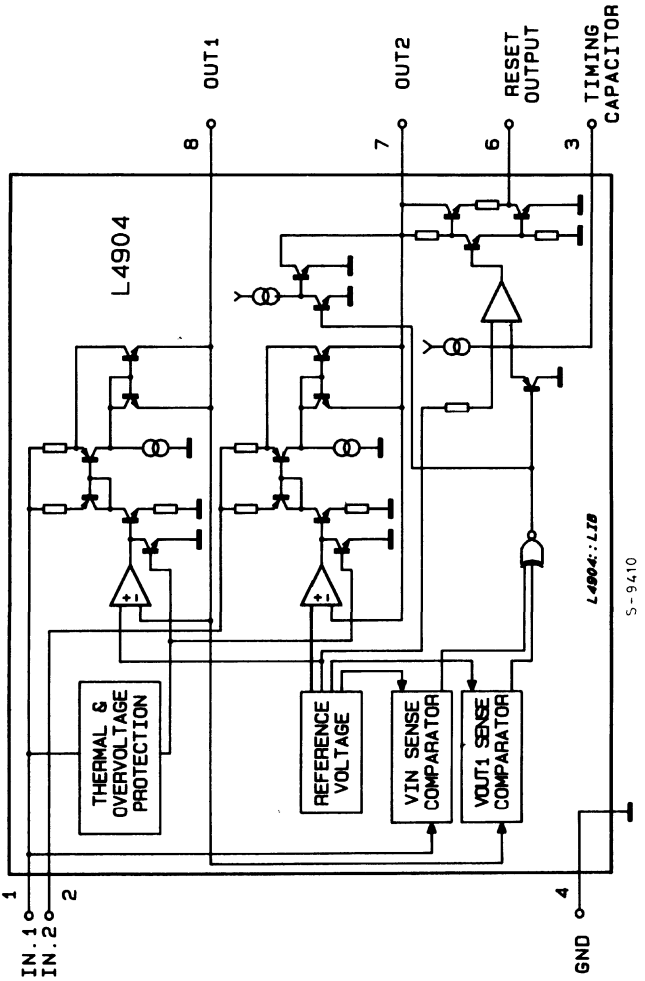
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	24	V
	Transient input overvoltage (t = 40ms)	60	V
I_o	Output current	internally limited	
P_{tot}	Power dissipation at T_{amb} = 50°C	1	W
T_j	Storage and junction temperature	-40 to 150	°C

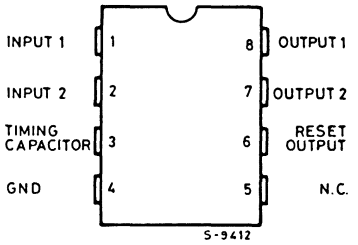
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



PIN FUNCTIONS

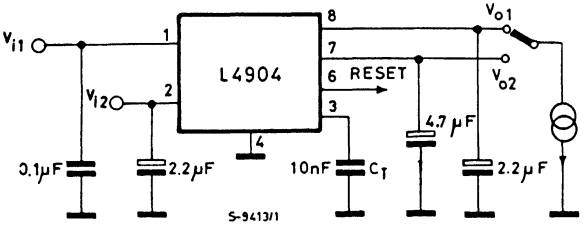
N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 50mA regulator input.
2	INPUT 2	100mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 5μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
6	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{5\mu A} \right)$; t_{RD} (ms) = C_t (nF).
7	OUTPUT 2	5V - 100mA regulator output. Enabled if $V_O 1 > V_{RT}$ and $V_{IN\,2} > V_{IT}$. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
8	OUTPUT 1	5V - 50mA regulator output with low leakage in switch-OFF condition.

THERMAL DATA

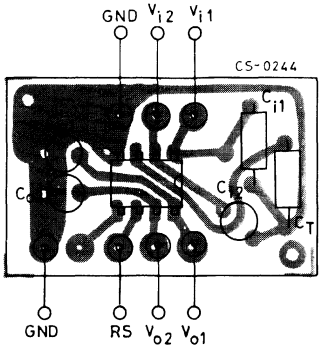
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

L4904

TEST CIRCUIT



P.C. board and components layout of the test circuit (1 : 1 scale)



ELECTRICAL CHARACTERISTICS (V_{IN} = 14.4V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC operating input voltage				20	V
V_{01}	Output voltage 1	R load 1KΩ	4.95	5.05	5.15	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01} -0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	I_{02} = -5mA		0.1		V
I_{01}	Output current 1	ΔV_{01} = -100mV	50			mA
I_{L01}	Leakage output 1 current	V_{IN} = 0 $V_{01} \leq$ 3V			1	μA
I_{02}	Output current 2	ΔV_{02} = -100mV	100			mA
V_{I01}	Output 1 dropout voltage (*)	I_{01} = 10mA I_{01} = 50mA		0.7 0.75	0.8 0.9	V V
V_{IT}	Input threshold voltage		V_{01} +1.2	6.4	V_{01} +1.6	V
V_{ITH}	Input threshold voltage hyst.			250		mV
ΔV_{01}	Line regulation	7V < V_{IN} < 18V I_{01} = 5mA		5	50	mV
ΔV_{02}	Line regulation 2	I_{02} = 5mA		5	50	
ΔV_{01}	Load regulation 1	V_{IN} = 8V 5mA < I_{01} < 50mA		5	20	mV
ΔV_{02}	Load regulation 2	5mA < I_{02} < 100mA		10	50	
I_Q	Quiescent current	0 < V_{IN} < 13V 6.3V < V_{IN} < 13V I_{02} = $I_{01} \leq$ 5mA		4.5 1.6	6 3.5	mA mA
I_{Q1}	Quiescent current 1	6.3V < V_{IN1} < 13V V_{IN2} = 0 $I_{01} \leq$ 5mA I_{02} = 0		0.6	0.9	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RT}	Reset threshold voltage		V_{02}-0.15	4.9	V_{02}-0.05	V
V_{RTH}	Reset threshold hysteresis			50	160	mV
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02} -1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	6	10	14	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	-20°C ⩽ T_{amb} ⩽ 140°C	-0.8	0.3	+0.8	mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	-20°C ⩽ T_{amb} ⩽ 140°C	-0.8	0.3	+0.8	mV/°C
SVR1	Supply voltage rejection	f = 100Hz, V_R = 0.5V, I_o = 50mA	54	84		dB
SVR2	Supply voltage rejection	f = 100Hz, V_R = 0.5V, I_o = 100mA	50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4904 makes it very easy to supply such equipments; it provides two voltage regulators (booth 5V high precision) with separate inputs plus a reset output for the data save function.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs:

- an input overvoltage
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:

- 5V internal reference without voltage divider between the output and the error comparator;
- very low drop series regulator element utilizing current mirrors;

permit high output impedance and then very low leakage current even in power down conditions.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery. The V_{01} regulator also features low consumption (0.6mA

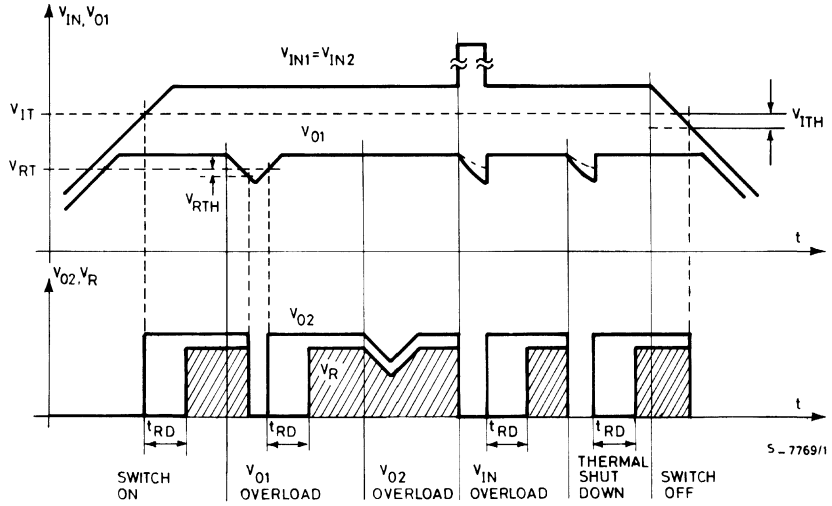
CIRCUIT OPERATION (continued)

typ.) to minimize battery drain in applications where the V_1 regulator is permanently connected to a battery supply.

The V_{02} output can supply other non essential 5V circuits which may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

Fig. 1



APPLICATION SUGGESTIONS

Fig. 2 shows an application circuit for a μP system.

Reg. 1 is permanently connected to a battery and supplies a CMOS time-of-day clock and a CMOS microcomputer chip with volatile memory.

Reg. 2 may be switched OFF when the system is inactive.

Fig. 3 shows the L4904 with a back up battery on the V_{01} output to maintain a CMOS time-of-day clock and a stand by type C-MOS μP. The reset output makes sure that the RAM is forced into the low consumption stand by state, so the access to memory is inhibit and the back up battery voltage cannot drop so low that memory contents are corrupted.

In this case the main on-off switch disconnects both regulators from the supply battery.

APPLICATION SUGGESTIONS (continued)

Application Circuits of a Microprocessor system (Fig. 2) or with data save battery (Fig. 3). The reset output provide delayed rising front at the turn-off of the regulator 2.

Fig. 2

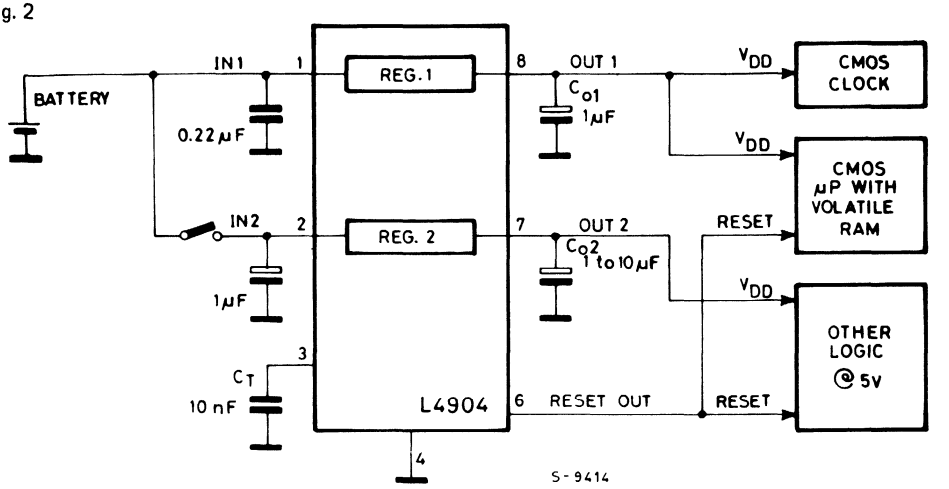
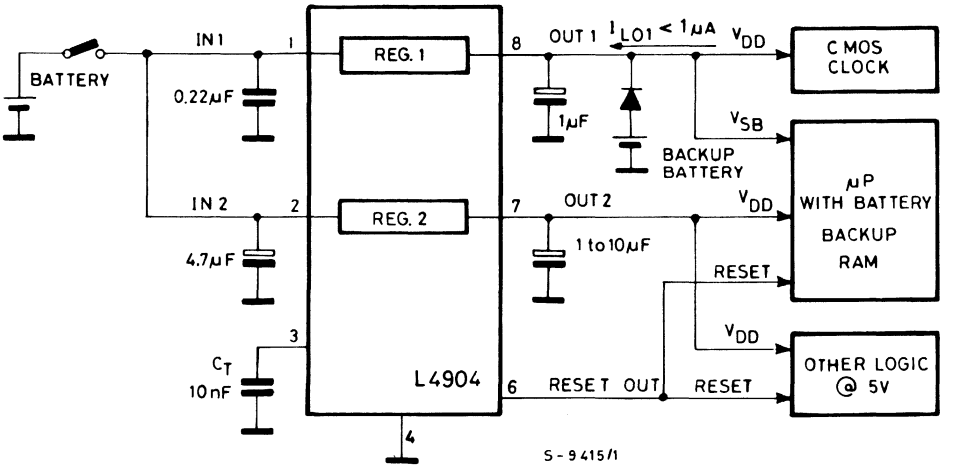


Fig. 3



APPLICATION SUGGESTIONS (continued)

Fig. 4 - Quiescent current (Reg. 1) vs. output current

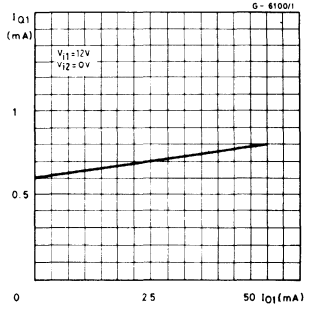


Fig. 5 - Quiescent current (Reg. 1) vs. input voltage

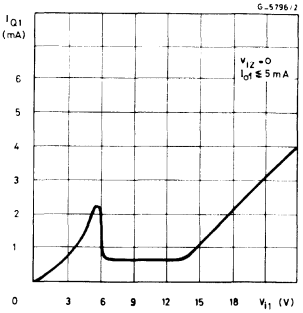


Fig. 6 - Total quiescent current vs. input voltage

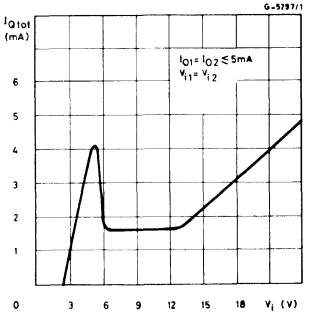
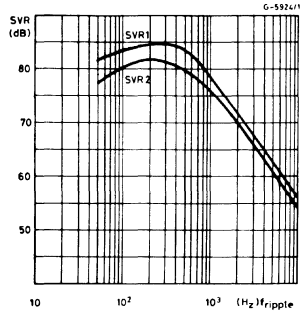


Fig. 7 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence



L4915

ADVANCE DATA

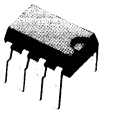
ADJUSTABLE VOLTAGE REGULATOR PLUS FILTER

- OUTPUT VOLTAGE ADJUSTABLE FROM 4 TO 11V
- HIGH OUTPUT CURRENT
- HIGH RIPPLE REJECTION
- HIGH LOAD REGULATION
- HIGH LINE REGULATION
- SHORT CIRCUIT PROTECTION
- THERMAL SHUT DOWN WITH HYSTERESIS
- DUMP PROTECTION

This circuit combines both a filter and a voltage regulator in order to provide a high ripple rejection over a wide input voltage range.

A supervisor low-pass loop of the element prevents the output transistor from saturation at low input voltage.

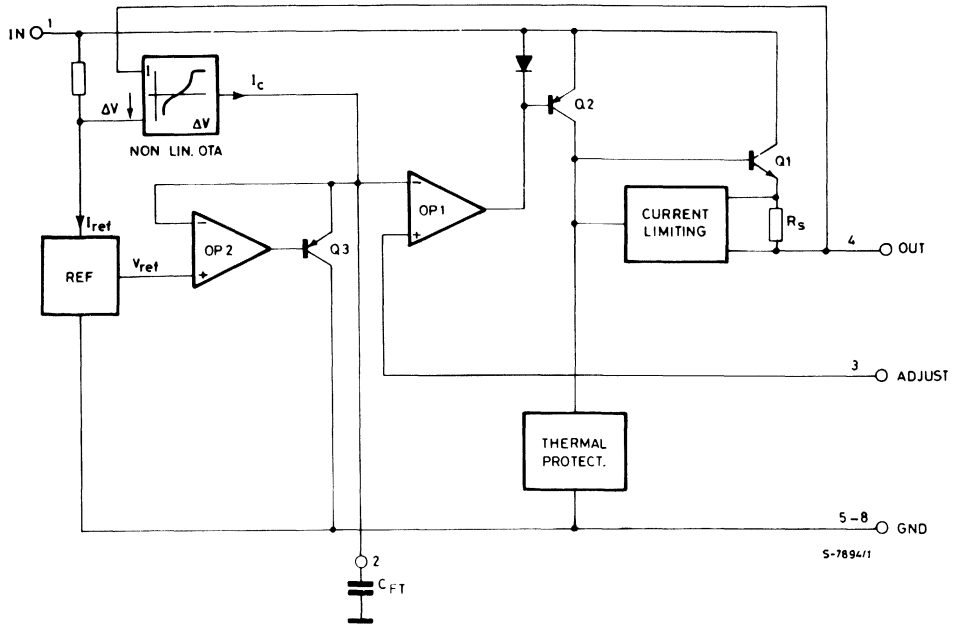
The non linear behaviour of this control circuitry allows a fast settling of the filter.



Power Minidip
(4 + 4)

ORDERING NUMBER: L4915

BLOCK DIAGRAM



L4915

ABSOLUTE MAXIMUM RATINGS

V_s	Peak input voltage (300ms)	40	V
V_s	DC input voltage	28	V
I_o	Output current	internally limited	
P_{tot}	Power dissipation	internally limited	
T_{stg}	Storage and junction temperature	-40 to 150	°C

CONNECTION DIAGRAM
(Top view)

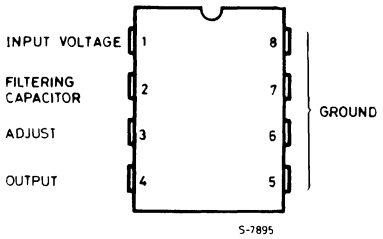
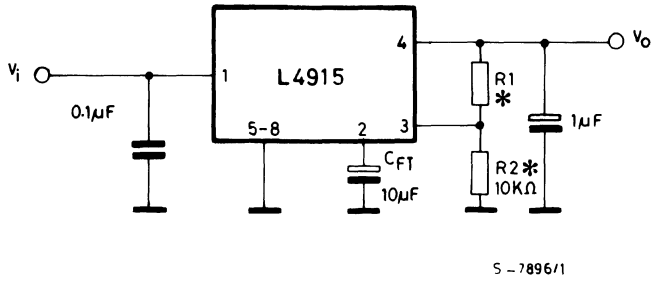


Fig. 1 - Application circuit



$$*\text{OUTPUT VOLTAGE } V_O = \frac{2.5(R1 + R2)}{R2}$$

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W
$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins	max	20	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_i = 13.5V, circuit of Fig. 1, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Input voltage				20	V
V_o	Output voltage	V_i = 6 to 18V I_o = 5 to 150mA	4		11	V
$\Delta V_{i/o}$	Controlled input-output dropout voltage	I_o = 5 to 150mA		1.6	2.1	V
ΔV_o	Line regulation	V_i = 12 to 18V I_o = 10mA			40	mV
ΔV_o	Load regulation	I_o = 5 to 150mA t_{on} = 30μs $t_{off} \geq$ 1ms			100	mV
ΔV_o	Load regulation	V_o = 8.5V I_o = 5 to 150mA t_{on} = 30μs $t_{off} \geq$ 1ms		100	250	mV
I_q	Quiescent current	I_o = 5mA		1	2	mA
ΔI_q	Quiescent current change	V_i = 6 to 18V V_o = 8.5V I_o = 0 to 150mA		0.05		mA
I_{AD}	Adjust input current			40		nA
$\frac{\Delta V_o}{\Delta T}$	Output voltage shift	I_o = 10mA		1.2		mV/°C
SVR	Supply voltage rejection	V_{iac} = 0.5V f = 100Hz I_o = 150mA V_o = 8.5V Regulator		70		dB
		filter		35 (*)		dB
I_{SC}	Short circuit current		200	300		mA
T_{on}	Switch on time	I_o = 150mA V_o = 8.5V Filter		500 (*)		ms
		regulator		300		ms
T_j	Thermal shutdown junction temperature			145		°C

(*) Depending of the C_{FT} capacitor.

PRINCIPLE OF OPERATION

During normal operation input voltage upper than $V_{IN\,MIN} = V_{OUT\,NOM} + \Delta V_{I/O}$). The device works as a normal voltage regulator built around the OP1 of the block diagram.
The series pass element use a PNP-NPN connection to reduce the dropout. The reference voltage of the OP1 is derived from V_{REF} through the OP2 and Q3, acting as an active zener diode of value V_{REF}.
In this condition the device works in the range (1) of the characteristic of the non linear drop control unit (see fig. 3).
The output voltage is fixed to its nominal value:

$$V_{OUT\,NOM} = V_{REF}\ (1 + \frac{R1}{R2}) =$$

$$V_{CFT}\ (1 + \frac{R1}{R2})$$

The ripple rejection is quite high (70dB) and independent from C_{FT} value.
On the usual voltage regulators, when the input voltage goes below the nominal value, the regulation transistors (series element) saturate and bring the system out regulation making it very sensible to every variation of the input voltage.
On the contrary, a control loop on the L4915 consents to avoid the saturation of the series element by regulating the value of the reference voltage of the OP1 (pin 2). In fact, whenever the input voltage decreases below ($V_{IM\,IN}$ the supervisor loop, utilizing a non linear OTA, forces by discharging C_{FT}. So, during the static mode, when the input voltage goes below V_{MIN} the drop out is kept fixed to about 1.6V. In this condition the device works as a low pass filter in the range (2) of the OTA characteristic.
The ripple rejection is externally adjustable acting on C_{FT} as follows:

$$SVRR\ (jw) = \frac{V_i\ (jw)}{V_{out}\ (kw)} =$$

$$1 + \frac{10^{-6}}{\frac{gm}{jwC_{FT}}\ (1 + \frac{R1}{R2})}$$

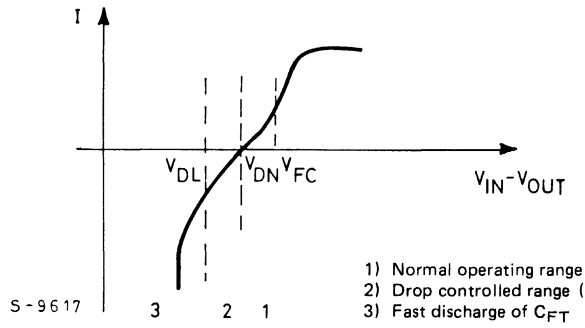
Where:
$gm = 2 \cdot 10^{-5}\ \Omega^{-1}$ = OTA'S typical transconductance value on linear region

$\frac{R1}{R2}$ = fixed ratio

C_{FT} = value of capacitor in μF

The reaction time of the supervisor loop is given by the transconductance of the OTA and by C_{FT}.
When the value of the ripple voltage is so high and its negative peak is fast/enough to determine an istantaneous decrease of the dropout till 1.2V, the OTA works in a higher transconductance condition [range (3) of the characteristic] and discharge the capacitor rapidously.
If the ripple frequency is high enough the capacitor won't charge itself completely, and the output voltage reaches a small value allowing a better ripple rejection; the device's again working as a filter (fast transient range).
With C_{FT} = 10μF; f = 100Hz a SVR of 30 is obtained.

Fig. 3 - Nonliner transfer characteristic of the drop control unit



1) Normal operating range (high ripple rejection)
2) Drop controlled range (medium ripple rejection)
3) Fast discharge of C_{FT}

Fig. 4 - Supply voltage rejection vs. input voltage

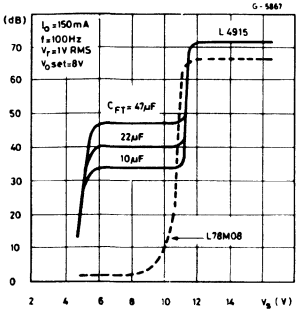


Fig. 5 - Supply voltage rejection vs. frequency

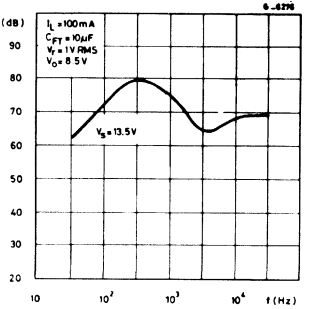


Fig. 6 - V_O vs. supply voltage (V_O = 8.5V)

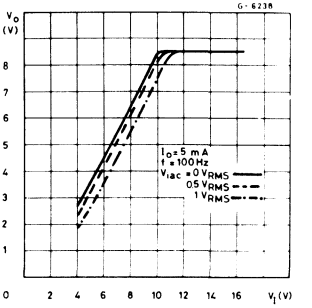


Fig. 7 - Quiescent current vs. input voltage (V_O = 8.5V)

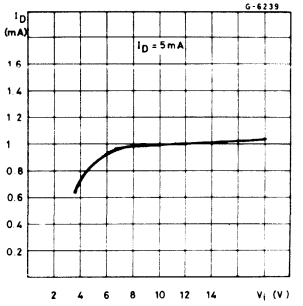
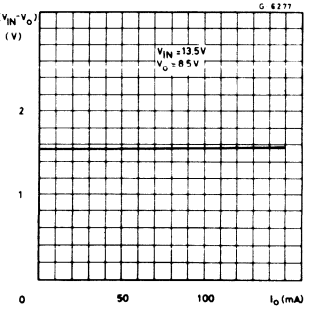


Fig. 8 - Dropout vs. load current



L4916

PRELIMINARY DATA

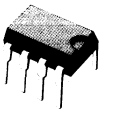
VOLTAGE REGULATOR PLUS FILTER

- FIXED OUTPUT VOLTAGE 8.5V
- 200mA OUTPUT CURRENT
- HIGH RIPPLE REJECTION
- HIGH LOAD REGULATION
- HIGH LINE REGULATION
- SHORT CIRCUIT PROTECTION
- THERMAL SHUT DOWN WITH HYSTERESIS
- DUMP PROTECTION

This circuit combines both a filter and a voltage regulator in order to provide a high ripple rejection over a wider input voltage range.

A supervisor low-pass loop of the element prevents the output transistor from saturation at low input voltages.

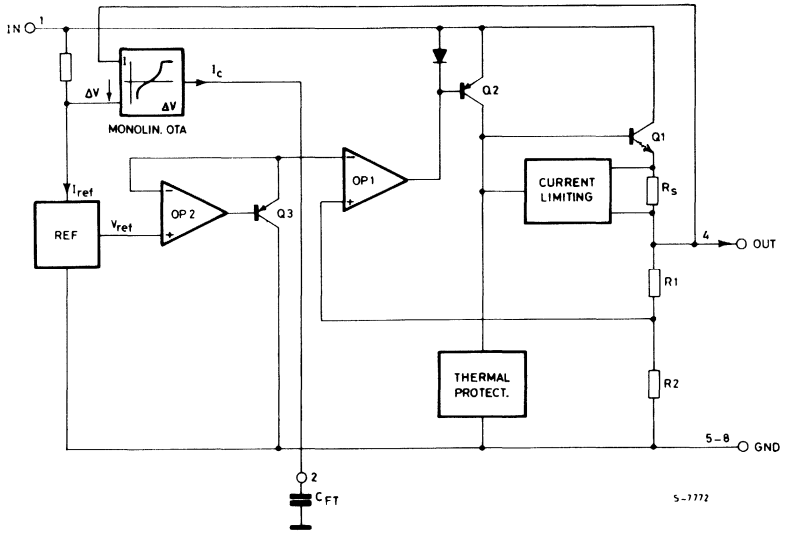
The non linear behaviour of this control circuitry allows a fast settling of the filter.



Power Minidip
(4 + 4)

ORDER CODE: L4916

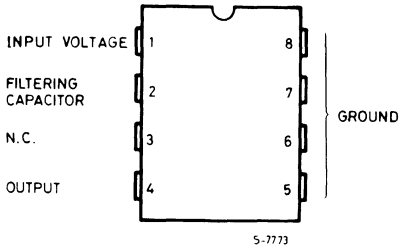
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_s	Peak input voltage (300 ms)	40	V
V_s	DC input voltage	28	V
I_o	Output current	internally limited	
P_{tot}	Power dissipation	internally limited	
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

CONNECTION DIAGRAM (top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W
$R_{th\ j\text{-}pins}$	Thermal resistance junction pins	max	20	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_i = 13.5V unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Input voltage				20	V
V_o	Output voltage	V_i = 12 to 18V I_o = 5 to 150 mA	8.1	8.5	8.9	V
$\Delta V_{i/o}$	Controlled input-output dropout voltage	V_i = 5 to 10V I_o = 5 to 150 mA		1.6	2.1	V
ΔV_o	Line regulation	V_i = 12 to 18V I_o = 10 mA		10		mV
ΔV_o	Load regulation	I_o = 5 to 150 mA t_{on} = 30 μs t_{off} = $\geqslant$ 1 ns		30	250	mV
ΔV_o	Load regulation	V_i = 8.5V I_o = 5 to 150 mA t_{on} = 30 μs t_{off} $\geqslant$ 1 ms		50		mV
I_D	Quiescent current	I_o = 5 mA		1.3	2	mA
ΔI_D	Quiescent current change	V_i = 6 to 18V I_o = 0 to 150 mA		0.05		mA
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o = 10 mA		1.2		mV/°C
SVR	Supply voltage rejection	V_{iac} = 0.5V C_{FT} = 10 μF f = 100 Hz I_o = 150 mA V_{IDC} = 12 to 18V V_{IDC} = 6 to 11V		70(**) 35(*)		dB dB
I_{SC}	Short circuit current		220	300		mA
T_{on}	Switch on time	I_o = 150 mA V_i = 5 to 11V C_{FT} = 10 μF V_i = 11 to 18V		500(*) 300		ms ms
T_j	Thermal shutdown junction temperature			145		°C

(*) Depending of the C_{FT} capacitor.
(**) Independent from C_{FT}.

Fig. 1 - Application circuit

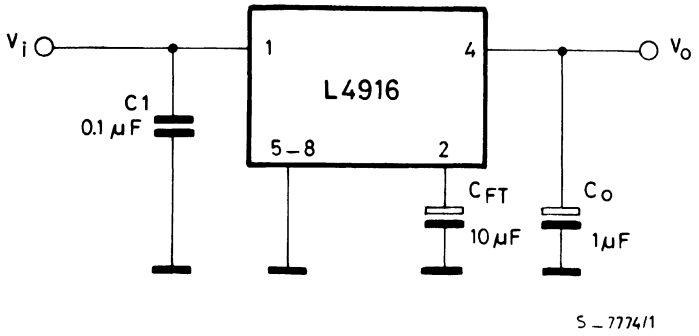
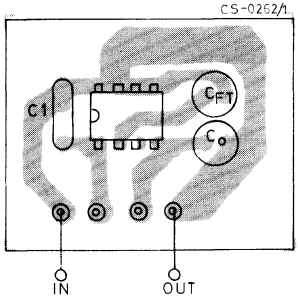


Fig. 2 - P.C. board and component layout of fig. 1 (1 : 1 scale)



PRINCIPLE OF OPERATION

During normal operation (input voltage upper than $V_{IN\ MIN} = V_{OUT\ NOM} + \Delta V_{I/O}$). The device works as a normal voltage regulator built around the OP1 of the block diagram.
The series pass element use a PNP-NPN connection to reduce the dropout. The reference voltage of the OP1 is derived from V_{REF} trough the OP2 and Q3, acting as an active zener diode of value V_{REF}.
In this condition the device works in the range (1) of the characteristic of the non linear drop control unit (see fig. 3).
The output voltage is fixed to its nominal value:

$$V_{OUT\ NOM} = V_{REF}\ (1 + \frac{R1}{R2}) =$$

$$V_{CFT}\ (1 + \frac{R1}{R2})$$

$$\frac{R1}{R2} = \text{FIXED RATIO} = 2.4$$

The ripple rejection is quite high (70 dB) and independent from C_{FT} value.
On the usual voltage regulators, when the input voltage goes below the nominal value, the regulation transistors (series element) saturate and bring the system out regulation making it very sensible to every variation of the input voltage.
On the contrary, a control loop on the L4916 consents to avoid the saturation of the series element by regulating the value of the reference voltage of the OP1 (pin 2). In fact, whenever the input voltage decreases below V_{IMIN} the supervisor loop, utilizing a non linear OTA, forces by discharging C_{FT}. So, during the static mode, when the input voltage goes below V_{MIN} the drop out is kept fixed to about 1.6V. In this condition the device works as a low pass filter in the range (2) of the OTA characteristic.
The ripple rejection is externallay adjustable acting on C_{FT} as follows:

$$SVRR\ (jw) = \frac{V_I\ (jw)}{V_{out}\ (kw)} =$$

$$1 + \frac{10^{-6}}{\frac{gm}{jwC_{FT}}\ (1 + \frac{R1}{R2})}$$

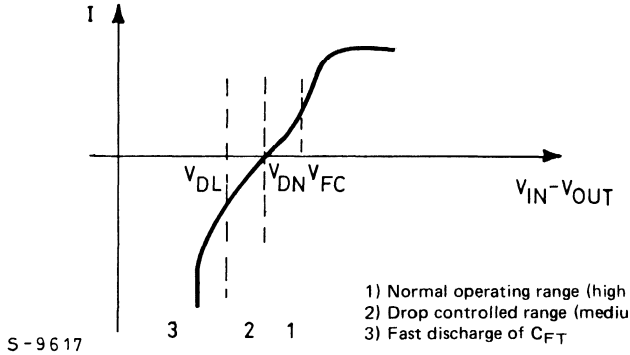
Where:
$gm = 2 \cdot 10^{-5}\ \Omega^{-1}$ = OTA'S typical transconductance value on linear region

$\frac{R1}{R2}$ = fixed ratio

C_{FT} = value of capacitor in μF

The reaction time of the supervisor loop is given by the transconductance of the OTA and by C_{FT}.
When the value of the ripple voltage is so high and its negative peak is fast/enough to determine an istantaneous decrease of the dropout till 1.2V, the OTA works in a higher transconductance condition [range (3) of the characteristic] and discharge the capacitor rapidously.
If the ripple frequency is high enough the capacitor won't charge itself completely, and the output voltage reaches a small value allowing a better ripple rejection; the device's again working as a filter (fast transient range).
With $C_{FT} = 10\ \mu F$; f = 100 Hz a SVR of 30 is obtained.

Fig. 3 - Nonliner transfer characteristic of the drop control unit



1) Normal operating range (high ripple rejection)
2) Drop controlled range (medium ripple rejection)
3) Fast discharge of C_{FT}

Fig. 4 - Supply voltage rejection vs. input voltage

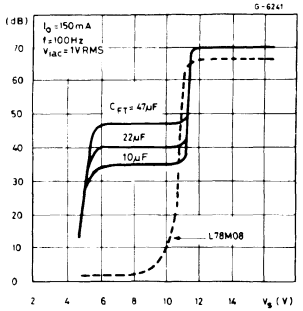


Fig. 5 - Supply voltage rejection vs. frequency

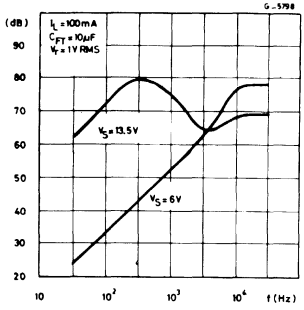


Fig. 6 - V_o vs. supply voltage

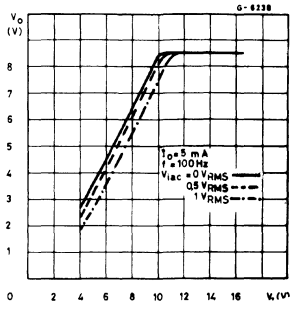


Fig. 7 - Quiescent current vs. input voltage

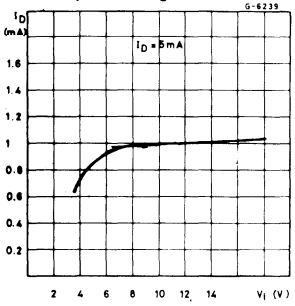


Fig. 8 - Dropout vs. load current

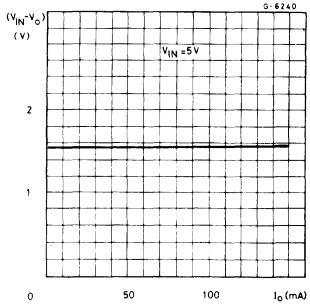
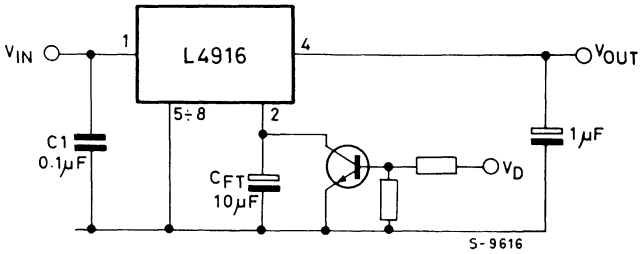


Fig. 9 - Inhibit function realized on C_{FT} pin.



L4918

ADVANCE DATA

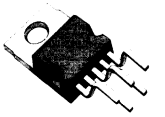
VOLTAGE REGULATORS PLUS FILTER

- FIXED OUTPUT VOLTAGE 8.5V
- 200mA OUTPUT CURRENT
- HIGH RIPPLE REJECTION
- HIGH LOAD REGULATION
- HIGH LINE REGULATION
- SHORT CIRCUIT PROTECTION
- THERMAL SHUT DOWN WITH HYSTERESIS
- DUMP PROTECTION

The L4918 combines both a filter and a voltage regulator in order to provide a high ripple rejection over a wider input voltage range.

A supervisor low-pass loop of the element prevents the output transistor from saturation at low input voltages.

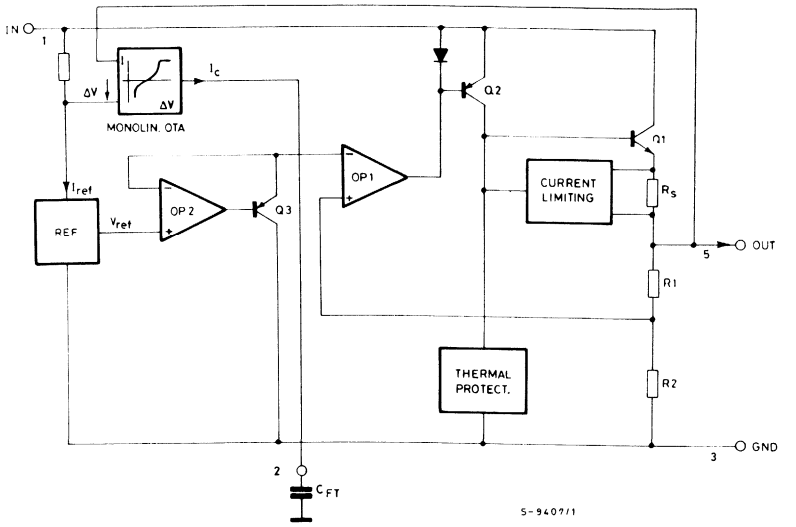
The non linear behaviour of this control circuitry allows a fast setting of the filter.



Pentawatt®

ORDERING NUMBERS: L4918

BLOCK DIAGRAM



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

L4918

ABSOLUTE MAXIMUM RATINGS

V_s	Peak input voltage (300ms)	40	V
V_s	DC voltage	28	V
V_s	Operating supply voltage	20	V
I_o	Output current	internally limited	
P_{tot}	Power dissipation	internally limited	
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

CONNECTION DIAGRAM
(Top view)

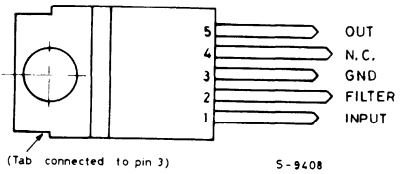
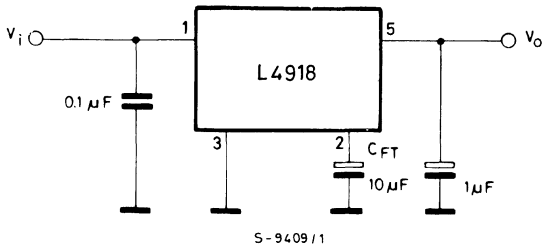


Fig. 1 - Application circuit



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	—
$R_{th\ j\text{-}case}$	Thermal resistance junction case	max	4°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_I = 13.5V unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output voltage	V_I = 12 to 18V I_o = 5 to 150mA	8.1	8.5	8.9	V
$\Delta V_{I/O}$	Controlled input-output dropout voltage	V_I = 5 to 10V I_o = 5 to 150mA		1.6	2.1	V
ΔV_o	Line regulation	V_I = 12 to 18V I_o = 10mA		10	40	mV
ΔV_o	Load regulation	I_o = 5 to 150mA t_{on} = 30μs t_{off} = ⩾ 1ns		30	250	mV
ΔV_o	Load regulation	V_I = 8.5V I_o = 5 to 150mA t_{on} = 30μs t_{off} = ⩾ 1ms		50	100	mV
I_D	Quiescent current	I_o = 5mA		1.0	2	mA
ΔI_D	Quiescent current change	V_I = 6 to 18V I_o = 0 to 150mA		0.05		mA
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o = 10mA		1.2		mV/°C
SVR	Supply voltage rejection	V_{Iac} = 0.5V C_{FT} = 10μF f = 100Hz I_o = 150mA V_{IDC} = 12 to 18V V_{IDC} = 6 to 11V		70 (**) 35 (*)		dB dB
I_{SC}	Short circuit current		200	300		mA
T_{on}	Switch on time	I_o = 150mA V_I = 5 to 11V C_{FT} = 10μF V_I = 11 to 18V		500 (*) 300		ms ms
T_{JSD}	Thermal shut down			150		°C

(*) Depending of the C_{FT} capacitor
(**) Independent from C_{FT}

PRINCIPLE OF OPERATION

During normal operation (input voltage upper than $V_{IN\ MIN} = V_{OUT\ NOM} + \Delta V_{I/O}$). The device works as a normal voltage regulator built around the OP1 of the block diagram.
The series pass element use a PNP-NPN connection to reduce the dropout. The reference voltage of the OP1 is derived from V_{REF} trough the OP2 and Q3, acting as an active zener diode of value V_{REF}.
In this condition the device works in the range (1) of the characteristic of the non linear drop control unit (see fig.).
The output voltage is fixed to its nominal value:

$$V_{OUT\ NOM} = V_{REF}\ (1 + \frac{R1}{R2}) =$$

$$V_{CFT}\ (1 + \frac{R1}{R2})$$

$$\frac{R1}{R2} = \text{FIXED RATIO} = 2.4$$

The ripple rejection is quite high (70 dB) and independent from C_{FT} value.
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$$SVRR\ (jw) = \frac{V_I\ (jw)}{V_{out}\ (kw)} =$$

$$1 + \frac{10^{-6}}{\frac{gm}{jwC_{FT}}\ (1 + \frac{R1}{R2})}$$

Where:
$gm = 2 \cdot 10^{-5}\ \Omega^{-1}$ = OTA'S typical transconductance value on linear region

$\frac{R1}{R2}$ = fixed ratio

C_{FT} = value of capacitor in μF

The reaction time of the supervisor loop is given by the tranconductance of the OTA and by C_{FT}. When the value of the ripple voltage is so high and its negative peak is fast/enough to determine an istantaneous decrease of the dropout till 1.2V, the OTA works in a higher transconductance condition [range (3) of the characteristic] and discharge the capacitor rapidously.
If the ripple frequency is high enough the capacitor won't charge itself completely, and the output voltage reaches a small value allowing a better ripple rejection; the device's again working as a filter (fast transient range).
With C_{FT} = 10 μF; f = 100 Hz a SVR of 30 is obtained.

Fig. 2 - Supply voltage rejection vs. frequency

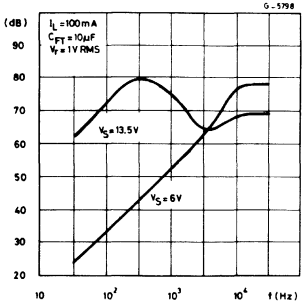


Fig. 3 - Supply voltage rejection vs. input voltage

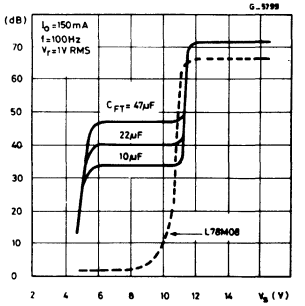
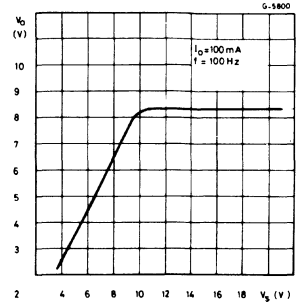


Fig. 4 - Output voltage vs input voltage



L4920
L4921

PRELIMINARY DATA

VERY LOW DROP ADJUSTABLE REGULATOR

- VERY LOW DROP VOLTAGE
- ADJUSTABLE OUTPUT VOLTAGES FROM 1.25V TO 20V
- 400mA OUTPUT CURRENT
- LOW QUIESCENT CURRENT
- OVERVOLTAGE AND REVERSE VOLTAGE PROTECTION
- +60/-60 TRANSIENT PEAK VOLTAGE
- SHORT CIRCUIT PROTECTION WITH FOLDBACK CHARACTERISTICS
- THERMAL SHUT-DOWN

The L4920 and L4921 are adjustable voltage regulators with a very low voltage drop (0.4V typ. at 0.4A), low quiescent current and comprehensive on-chip protection.

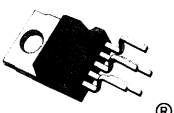
These devices are protected against load dump transients of ± 60V, input overvoltage, polarity reversal and over heating.

A foldback current limiter protects against load short circuits.

The output voltage is adjustable through an external divider from 1.25V to 20V. The minimum operating input voltage is 5.2V.

These regulators are designed for automotive, industrial and consumer applications where low consumption is particularly important.

In battery backup and standby applications the low consumption of these devices extends battery life.



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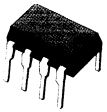
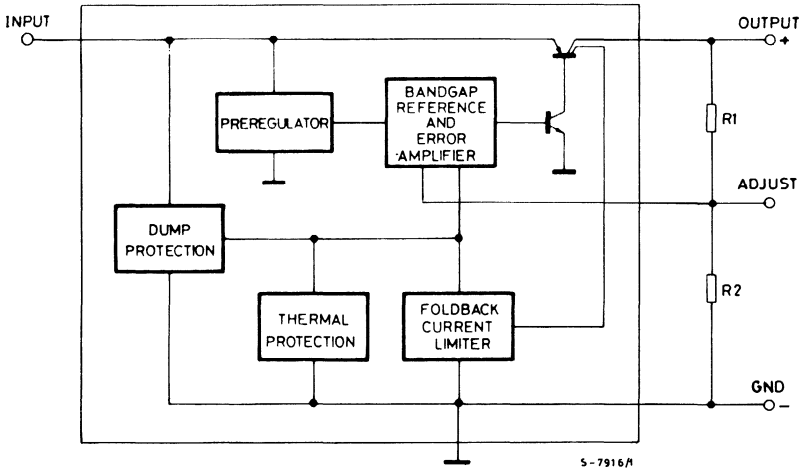


Minidip (4 + 4)

ORDERING NUMBERS:

L4920 L4921

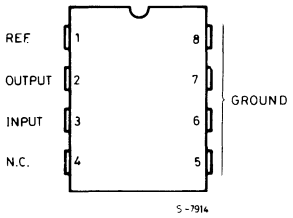
BLOCK DIAGRAM



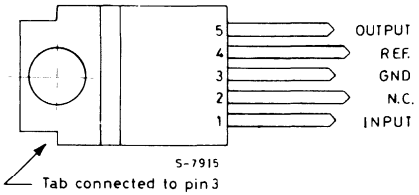
ABSOLUTE MAXIMUM RATINGS

V_i	DC input operating voltage	26	V
V_t	Positive transient peak voltage (t = 300ms 1% duty cycle)	+60	V
V_t	Negative transient peak voltage (t = 100ms 1% duty cycle)	-60	V
V_i	Reverse input voltage	-18	V
T_{stg}	Storage temperature	-55 to 150	°C
T_{op}	Operating junction temperature	-40 to 150	°C

CONNECTION DIAGRAMS (top view)

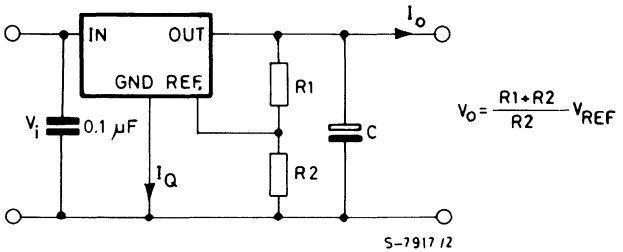


Minidip



Pentawatt

APPLICATION CIRCUIT



C = 100μF is required for stability (ESR ≤ 3Ω over T range)
R2 = 6.2KΩ.

THERMAL DATA

			Minidip (4 + 4)	Pentawatt
$R_{th\ j\text{-}amb}$	Thermal resistance junction ambient	max	80°C/W	60°C/W
$R_{th\ j\text{-}pins}$	Thermal resistance junction pins	max	15°C/W	–
$R_{th\ j\text{-}case}$	Thermal resistance junction case	max	–	4°C/W

ELECTRICAL CHARACTERISTICS (For V_i = 14.4V V_o = 5V; T_j = 25°C; C = 100μF; R2 = 6.2KΩ unless otherwise noted)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	Operating input voltage	$V_o \geq 4.5V$ I_o = 400mA	V_o+0.7		26	V
		$V_{REF} \leq V_o < 4.5V$ I_o = 400mA	5.2		26	V
V_{REF}	Reference voltage	5.2V < V_i < 26V $I_o \leq$ 400mA (*)	1.20	1.25	1.30	V
ΔV_o	Line regulation	V_o + 1V < V_i < 26V $V_o \geq 4.5V$ I_o = 5mA		1	10	mV/V_o
ΔV_o	Load regulation	5mA < I_o < 400mA (*) $V_o \geq 4.5V$		3	15	mV/V_o
V_D	Dropout voltage	I_o = 10mA I_o = 150mA I_o = 400mA		0.05 0.2 0.4	 0.4 0.7	V V V
I_D	Quiescent current	I_o = 0mA V_o + 1V < V_i < 26V		0.8	3	mA
		I_o = 400mA (*) V_o + 1V < V_i < 26V		65	100	mA
I_o	Maximum output current			650	900	mA
I_{OSC}	Short circuit output current (*)		200	350	500	mA
V_R	Reverse polarity input voltage (DC)	$V_o \geq$ -1.5V $R_L \leq 500\Omega$			-18	V

(*) Foldback protection

Fig. 1 - Output voltage vs. temperature

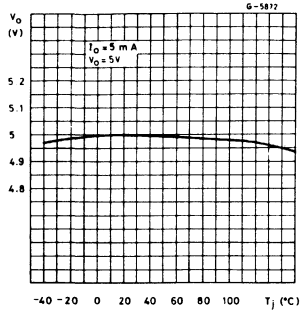


Fig. 2 - Foldback current limiting

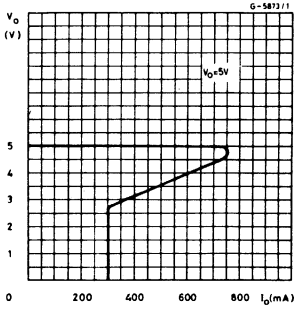
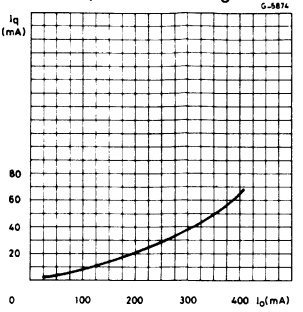


Fig. 3 - Quiescent current vs. output current (V_o = 5V)



APPLICATION INFORMATION

1) The L4920 and L4921 have $V_{REF} \cong 1.25V$. Then the output voltage can be set down to V_{REF} but V_I must be greater than 5.2V.
2) As the regulator reference voltage source works in closed loop, the reference voltage may change in foldback condition.
3) For applications with high V_i the total power dissipation of the device with respect to the thermal resistance of the package may be limiting the application. The total power dissipation is:

$$P_{tot} = V_i I_q + (V_i - V_o) I_o$$

A typical curve giving the quiescent current I_q as a function of the output current I_o is shown in fig. 3.

L4940

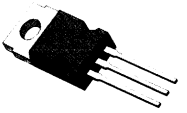
ADVANCE DATA

VERY LOW DROP 1.5A REGULATOR

- PRECISE 5V OUTPUT (± 2%)
- LOW DROPOUT VOLTAGE (400mV TYP. AT 1A)
- VERY LOW QUIESCENT CURRENT
- THERMAL SHUT DOWN
- SHORT CIRCUIT CURRENT LIMITER
- OVERVOLTAGE PROTECTION
- REVERSE POLARITY PROTECTION

The L4940 is a very low input/output voltage drop, low quiescent current and high output current capability IC particularly useful in applications such as battery powered systems where power dissipation is a design constraint.

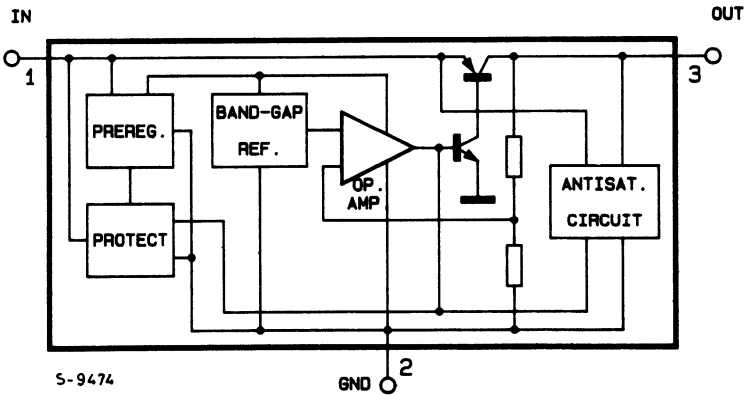
Standard regulator features such as thermal shut down, current limiter and overvoltage protection are also provided.



TO-220

ORDERING NUMBER: L4940BV

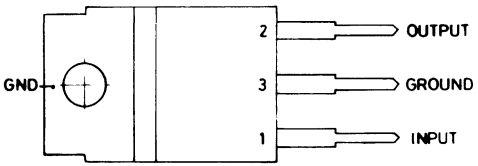
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

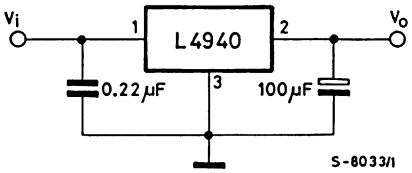
V_i	Forward input voltage (R_O = 100Ω)	40	V
V_i	Reverse input voltage (R_O = 100Ω)	-15	V
T_{op}	Operating junction temperature range	-40 to 125	°C
T_j	Maximum junction temperature	150	°C
T_{stg}	Storage temperature range	-65 to 150	°C

CONNECTION DIAGRAM (top view)



S-2568/1

TEST AND APPLICATION CIRCUIT



S-8033/1

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

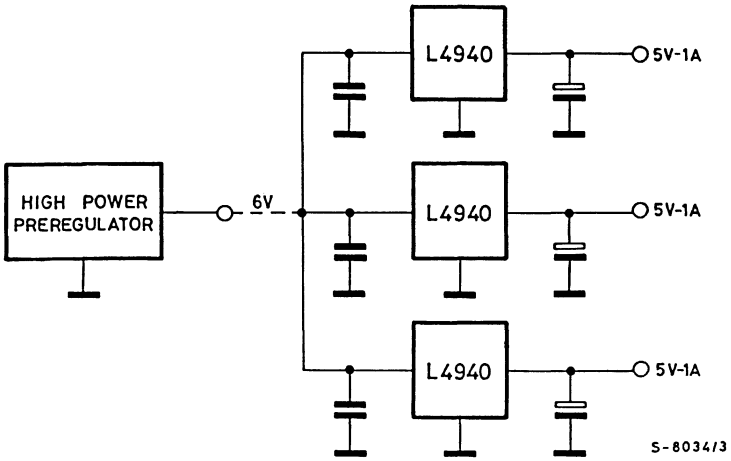
ELECTRICAL CHARACTERISTICS (V_i = 14V, T_j = 25°C)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_O	Output voltage	I_O = 5mA	4.9	5	5.1	V
V_O	Output voltage	V_i = 6V to 14V I_O = 5mA to 1A	4.8	5	5.2	V
V_i	Operating input voltage	(*) See note			18	V
V_O	Line regulation	6V ≤ V_i ≤ 18V I_O = 5mA		5		mV
V_O	Load regulation	I_O = 50mA to 1A		15		mV
I_d	Quiescent current	6V ≤ V_i ≤ 16V I_O = 5mA		5		mA
		I_O = 1A		50		
V_i-V_O	Dropout voltage	I_O = 1A		400		mV
		I_O = 100mA		100		
$\Delta V_O/\Delta T$	Output voltage drift			1		mV/°C
SVR	Supply voltage rejection	f = 120Hz I_O = 0.5A		74		dB
I_O	Current limit			1.3		A
Z_O	Output impedance	I_O = 200mA f = 120Hz		30		mΩ
E_N	Output noise voltage	f = 100Hz to 100KHz I_O = 10mA		100		μV rms

(*) For a DC input voltage 16V < V_i < 40V the device is not operating

APPLICATION INFORMATION

Fig. 1 - Distributed supply with on-card L4940 low-drop regulators



Advantages of this application are:

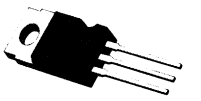
- Card isolation
- Thermal and short-circuit protection
- High efficiency (80%), like switching regulators, but without radiation and intermodulation problems

VERY LOW DROP 1A REGULATOR

- PRECISE 5V OUTPUT (± 2%)
- LOW DROPOUT VOLTAGE (450mV TYP. AT 1A)
- VERY LOW QUIESCENT CURRENT
- THERMAL SHUT DOWN
- SHORT CIRCUIT CURRENT LIMITER
- OVERVOLTAGE PROTECTION
- REVERSE POLARITY PROTECTION

The L4941 is a very low input/output voltage drop, low quiescent current and high output current capability IC particularly useful in applications such as battery powered systems where power dissipation is a design constraint.

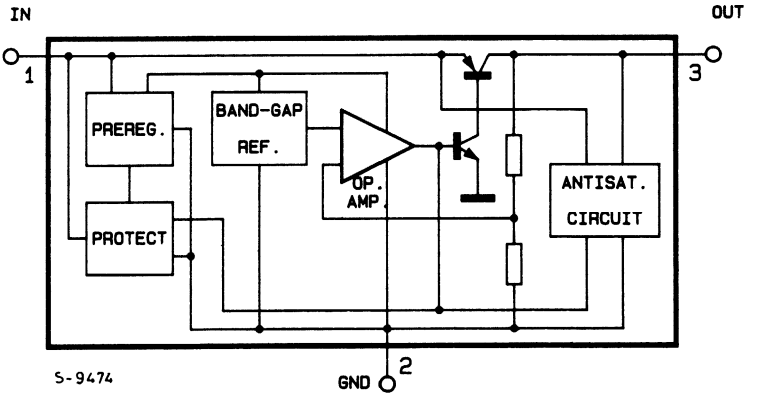
Standard regulator features such as thermal shut down, current limiter and overvoltage protection are also provided.



TO-220

ORDERING NUMBER: L4941BV

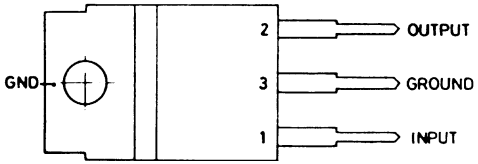
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

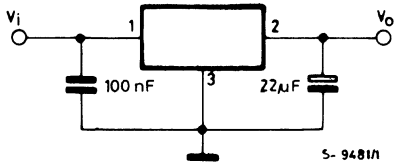
V_i	Forward input voltage (R_O = 100Ω)	40	V
V_i	Reverse input voltage (R_O = 100Ω)	-15	V
T_{op}	Operating junction temperature range	-40 to 125	°C
T_j	Maximum junction temperature	150	°C
T_{stg}	Storage temperature range	-65 to 150	°C

CONNECTION DIAGRAM
(Top view)



S-2568/1

TEST AND APPLICATION CIRCUIT



S-9481/1

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

ELECTRICAL CHARACTERISTICS (V_I = 14V, T_j = 25°C)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_O	Output voltage	I_O = 5mA	4.9	5	5.1	V
V_O	Output voltage	V_i = 6V to 14V I_O = 5mA to 1A	4.8	5	5.2	V
V_i	Operating input voltage	(*) See note			16	V
V_O	Line regulation	6V ≤ V_i ≤ 16V I_O = 5mA		5	25	mV
V_O	Load regulation	I_O = 50mA to 1A		15	35	mV
I_d	Quiescent current	6V ≤ V_i ≤ 16V I_O = 5mA		3.5	10	mA
		I_O = 1A		20	50	
V_i-V_O	Dropout voltage	I_O = 1A		450	700	mV
		I_O = 100mA		150	250	
$\Delta V_O/\Delta T$	Output voltage drift			0.6		mV/°C
SVR	Supply voltage rejection	f = 120Hz I_O = 0.5A	60			dB
I_O	Current limit			1.3		A
Z_O	Output impedance	I_O = 200mA f = 120Hz		30		mΩ
E_N	Output noise voltage	f = 100Hz to 100KHz I_O = 10mA		100		μV rms

(*) For a DC input voltage 16V < V_i < 40V the device is not operating

Fig. 1 - Dropout output voltage vs. current

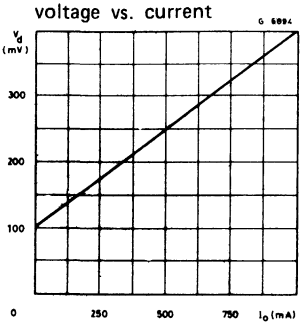


Fig. 2 - Quiescent current vs. output current

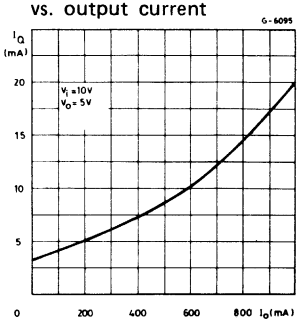


Fig. 3 - Quiescent current vs. load current

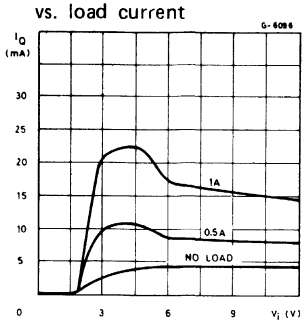


Fig. 4 - Low voltage behaviour

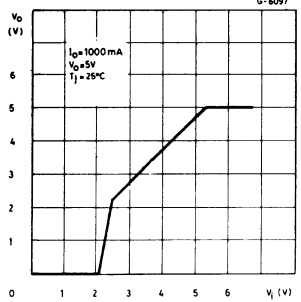


Fig. 5 - Output at voltage extremes

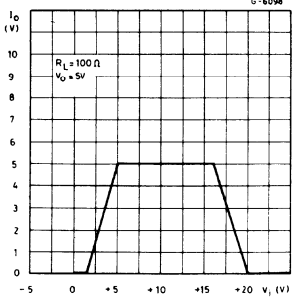
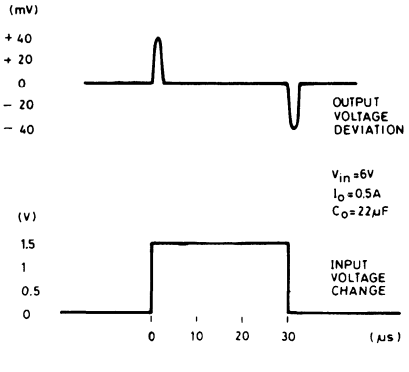
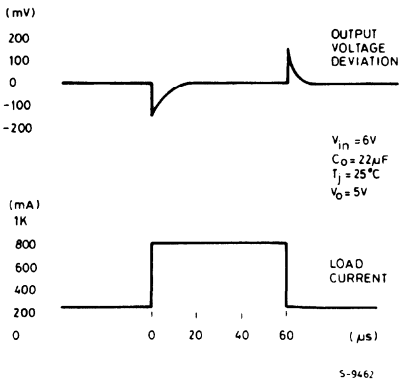


Fig. 6 - Line transient response



S-9461

Fig. 7 - Load transient response



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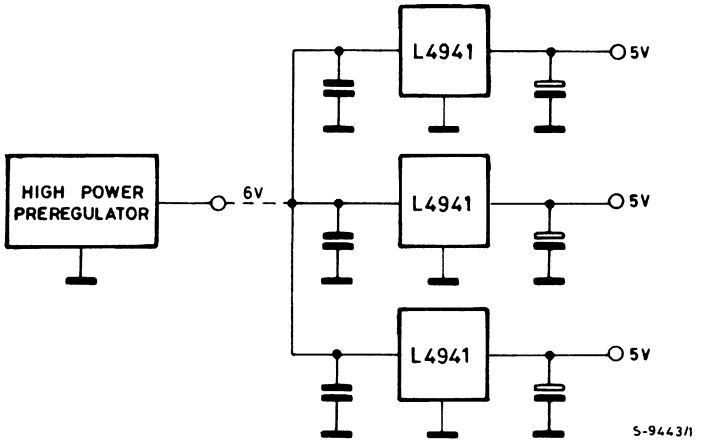
APPLICATION INFORMATION

Fig. 8 - Distributed supply with on-card L4941 low-drop regulators



Advantages of this application are:

- Card isolation
- Thermal and short-circuit protection
- High efficiency (80%), like switching regulators, but without radiation and intermodulation problems

L4960

PRELIMINARY DATA

2.5A POWER SWITCHING REGULATOR

- 2.5A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- PRECISE (± 2%) ON-CHIP REFERENCE
- HIGH SWITCHING FREQUENCY
- VERY HIGH EFFICIENCY (UP TO 90%)
- VERY FEW EXTERNAL COMPONENTS
- SOFT START
- INTERNAL LIMITING CURRENT
- THERMAL SHUTDOWN

The L4960 is a monolithic power switching regulator delivering 2.5A at a voltage variable from 5V to 40V in step down configuration.

Features of the device include current limiting, soft start, thermal protection and 0 to 100% duty cycle for continuous operation mode.

The L4960 is mounted in a Heptawatt plastic power package and requires very few external components.

Efficient operation at switching frequencies up to 150KHz allows a reduction in the size and cost of external filter components.

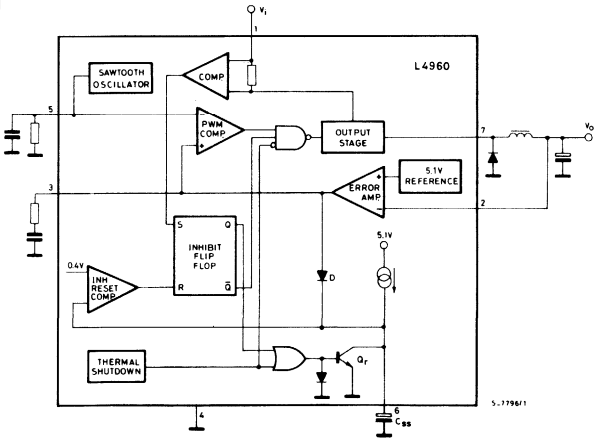
Heptawatt

ORDERING NUMBER: L4960 (Vertical)
L4960H (Horizontal)

ABSOLUTE MAXIMUM RATINGS

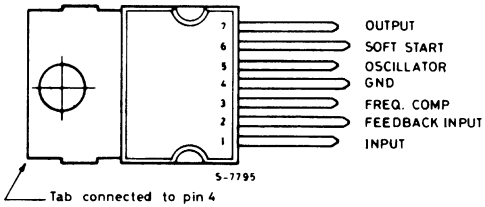
V_1	Input voltage	50	V
$V_1 - V_7$	Input to output voltage difference	50	V
V_7	Negative output DC voltage	-1	V
	Negative output peak voltage at t = 0.1μs; f = 100KHz	-5	V
V_3, V_6	Voltage at pin 3 and 6	5.5	V
V_2	Voltage at pin 2	7	V
I_3	Pin 3 sink current	1	mA
I_5	Pin 5 source current	20	mA
P_{tot}	Power dissipation at $T_{case} \leqslant 90°C$	15	W
T_j, T_{stg}	Junction and storage temperature	-40 to 150	°C

BLOCK DIAGRAM



L4960

CONNECTION DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50	°C/W

PIN FUNCTIONS

N°	NAME	FUNCTION
1	SUPPLY VOLTAGE	Unregulated voltage input. An internal regulator powers the internal logic.
2	FEEDBACK INPUT	The feedback terminal of the regulation loop. The output is connected directly to this terminal for 5.1V operation; it is connected via a divider for higher voltages.
3	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
4	GROUND	Common ground terminal.
5	OSCILLATOR	A parallel RC network connected to this terminal determines the switching frequency.
6	SOFT START	Soft start time constant. A capacitor is connected between this terminal and ground to define the soft start time constant. This capacitor also determines the average short circuit output current.
7	OUTPUT	Regulator output.

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $T_j = 25°C$, $V_I = 35V$, unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTICS							
V_o	Output voltage range	$V_I = 46V$	$I_o = 1A$	V_{ref}		40	V
V_I	Input voltage range	$V_o = V_{ref}$ to 36V	$I_o = 2.5A$	9		46	V
ΔV_o	Line regulation	$V_I = 10V$ to 40V	$V_o = V_{ref}$ $I_o = 1A$		15	50	mV
ΔV_o	Load regulation	$V_o = V_{ref}$	$I_o = 0.5A$ to 2A		10	30	mV
V_{ref}	Internal reference voltage (pin 2)	$V_I = 9V$ to 46V	$I_o = 1A$	5	5.1	5.2	V
$\frac{\Delta V_{ref}}{\Delta T}$	Average temperature coefficient of refer. voltage	$T_j = 0°C$ to 125°C $I_o = 1A$			0.4		mV/°C
V_d	Dropout voltage	$I_o = 2A$			1.4	3	V
I_{om}	Maximum operating load current	$V_I = 9V$ to 46V $V_o = V_{ref}$ to 36V		2.5			A
I_{7L}	Current limiting threshold (pin 7)	$V_I = 9V$ to 46V $V_o = V_{ref}$ to 36V		3		4.5	A
I_{SH}	Input average current	$V_I = 46V$; output short-circuit			30	60	mA
η	Efficiency	f = 100KHz	$V_o = V_{ref}$		75		%
		$I_o = 2A$	$V_o = 12V$		85		%
SVR	Supply voltage ripple rejection	$\Delta V_I = 2V_{rms}$ $f_{ripple} = 100Hz$ $V_o = V_{ref}$	$I_o = 1A$	50	56		dB
f	Switching frequency			85	100	115	KHz
$\frac{\Delta f}{\Delta V_I}$	Voltage stability of switching frequency	$V_I = 9V$ to 46V			0.5		%
$\frac{\Delta f}{\Delta T_j}$	Temperature stability of switching frequency	$T_j = 0°C$ to 125°C			1		%
f_{max}	Maximum operating switching frequency	$V_o = V_{ref}$	$I_o = 2A$	120	150		KHz
T_{sd}	Thermal shutdown junction temperature				150		°C

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
DC CHARACTERISTICS							
I_{1Q}	Quiescent drain current	100% duty cycle pins 5 and 7 open	V_I = 46V		30	40	mA
		0% duty cycle			15	20	mA
$-I_{7L}$	Output leakage current	0% duty cycle				1	mA
SOFT START							
I_{6SO}	Source current			100	130	150	μA
I_{6SI}	Sink current			50	70	120	uA
ERROR AMPLIFIER							
V_{3H}	High level output voltage	V_2 = 4.7V	I_3 = 100μA	3.5			V
V_{3L}	Low level output voltage	V_2 = 5.3V	I_3 = 100μA			0.5	V
I_{3SI}	Sink output current	V_2 = 5.3V		100	150		μA
$-I_{3SO}$	Source output current	V_2 = 4.7V		100	150		μA
I_2	Input bias current	V_2 = 5.2V			2	10	μA
G_v	DC open loop gain	V_3 = 1V to 3V		46	55		dB
OSCILLATOR							
$-I_5$	Oscillator source current			5			mA

CIRCUIT OPERATION (refer to the block diagram)

The L4960 is a monolithic stepdown switching regulator providing output voltages from 5.1V to 40V and delivering 2.5A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1V on-chip reference (zener zap trimmed to ± 2%).

This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage.

The gain and frequency stability of the loop can be adjusted by an external RC network connected to pin 3. Closing the loop directly gives an output voltage of 5.1V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor C_{ss} and allowed to rise, linearly, as this capacitor is charged by a constant current source. Output overload protection is provided in the form of a current limiter. The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4V.

The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network. The thermal overload circuit disables circuit operation when the junction temperature reaches about 150°C and has hysteresis to prevent unstable conditions.

Fig. 1 - Soft start waveforms

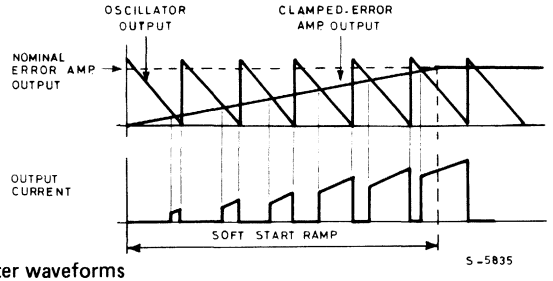


Fig. 2 - Current limiter waveforms

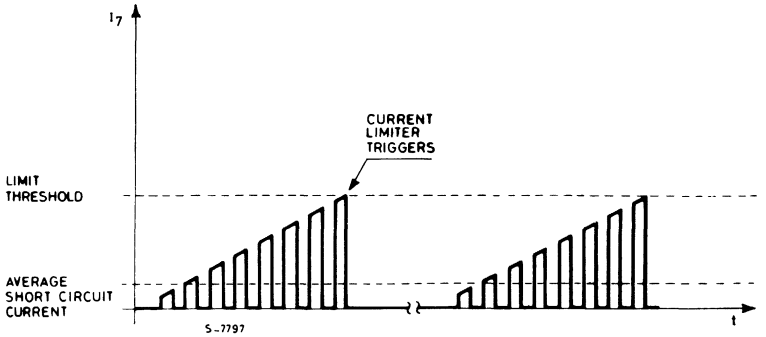
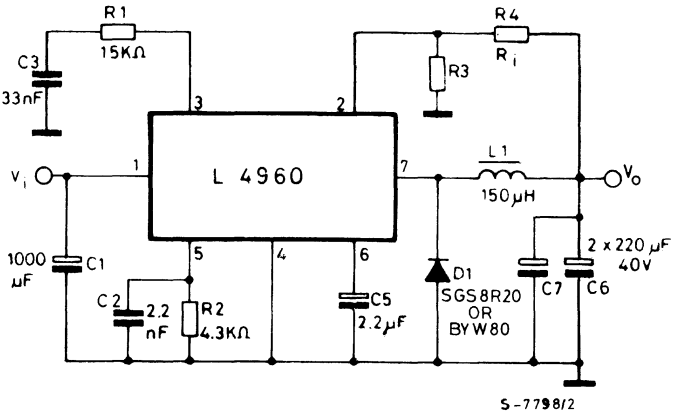


Fig. 3 - Test and application circuit



C6, C7: EKR (ROE)
L1 = 150μH at 5A (COGEMA 946042)
CORE TYPE: MAGNETICS 58206-A2 MPP
N° TURNS 45, WIRE GAUGE: 0.8mm (20 AWG)

Fig. 4 - Quiescent drain current vs. supply voltage (0% duty cycle)

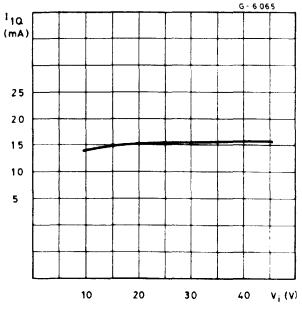


Fig. 5 - Quiescent drain current vs. supply voltage (100% duty cycle)

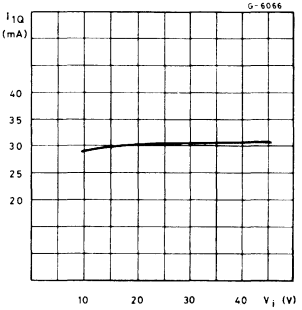


Fig. 6 - Quiescent drain current vs. junction temperature (0% duty cycle)

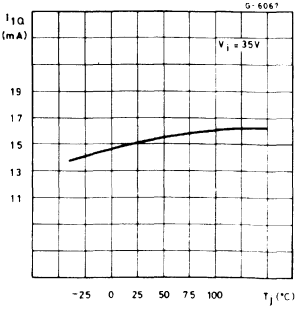


Fig. 7 - Quiescent drain current vs. junction temperature (100% duty cycle)

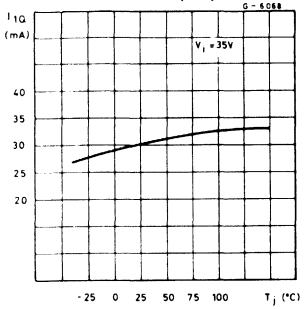


Fig. 8 - Reference voltage (pin 2) vs. V_i

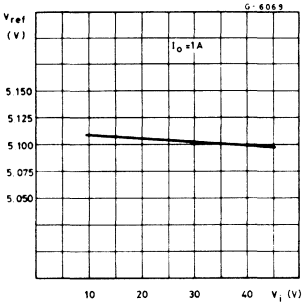


Fig. 9 - Reference voltage vs. junction temperature (pin 2)

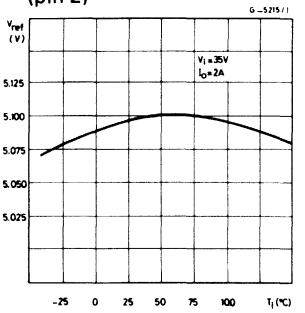


Fig. 10 - Open loop frequency and phase responde of error amplifier

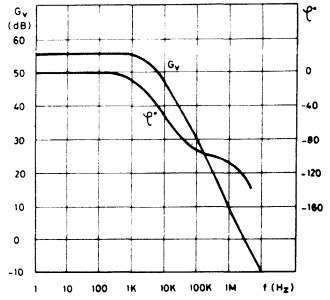


Fig. 11 - Switching frequency vs. input voltage

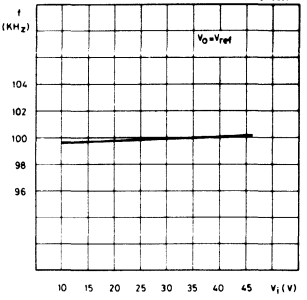


Fig. 12 - Switching frequency vs. junction temperature

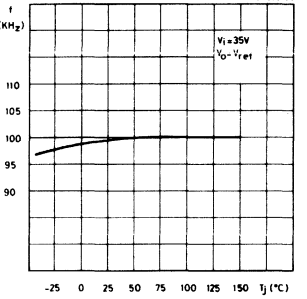


Fig. 13 - Switching frequency vs. R2 (see test circuit)

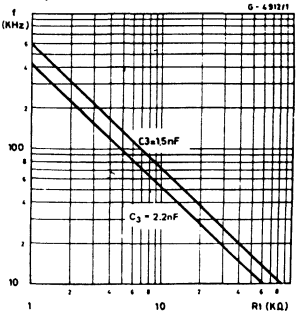


Fig. 14 - Line transient response

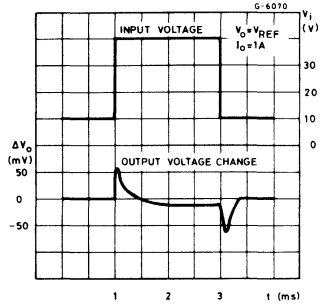


Fig. 15 - Load transient response

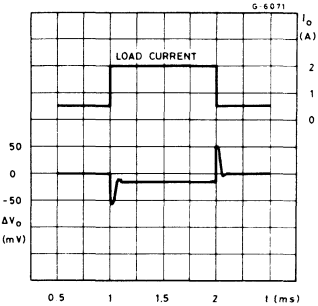


Fig. 16 - Supply voltage ripple rejection vs. frequency

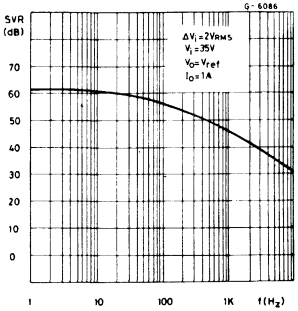


Fig. 17 - Dropout voltage between pin 1 and pin 7 vs. current at pin 7

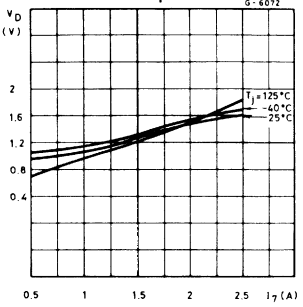


Fig. 18 - Dropout voltage between pin 1 and 7 vs. junction temperature

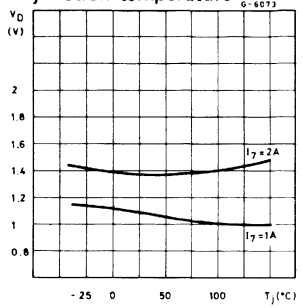


Fig. 19 - Power dissipation derating curve

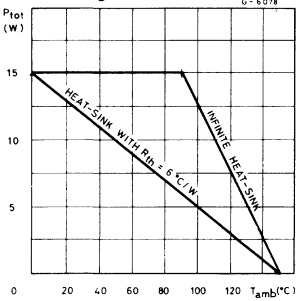


Fig. 20 - Efficiency vs. output current

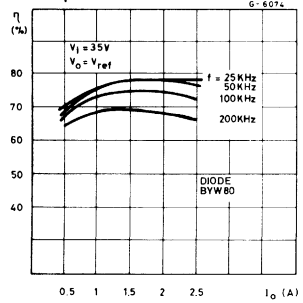


Fig. 21 - Efficiency vs. output current

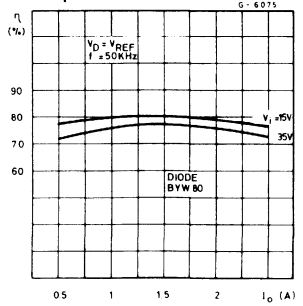


Fig. 22 - Efficiency vs. output current

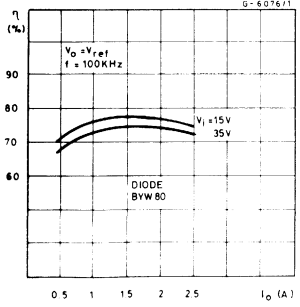
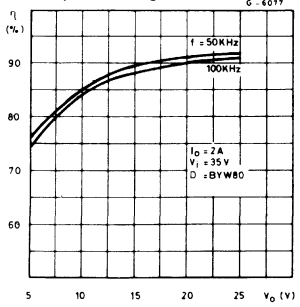
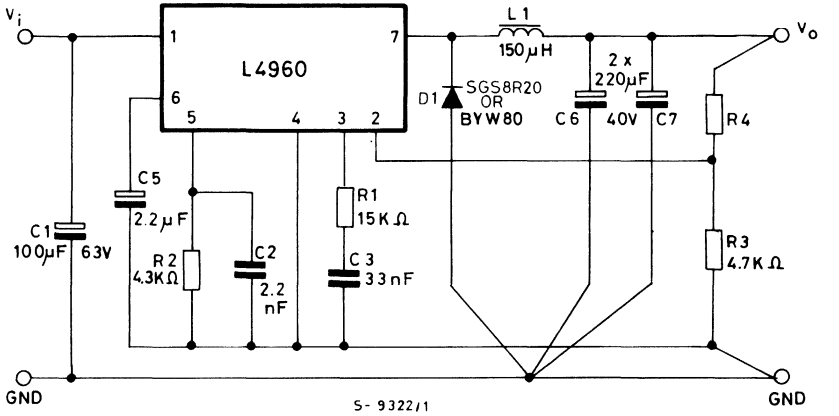


Fig. 23 - Efficiency vs. output voltage



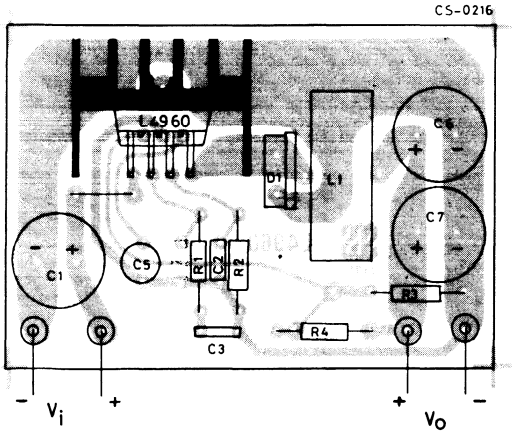
APPLICATION INFORMATION

Fig. 24 - Typical application circuit



C_1, C_6, C_7: EKR (ROE)
D_1: BYW80 OR 5A SCHOTTKY DIODE
SUGGESTED INDUCTOR: L_1 = 150µH at 5A
CORE TYPE: MAGNETICS 58206 - A2 - MPP
N° TURNS: 45, WIRE GAUGE: 0.8mm (20 AWG), COGEMA 946042
U15/GUP15: N° TURNS: 60, WIRE GAUGE: 0.8mm (20 AWG), AIR GAP: 1mm, COGEMA 969051.

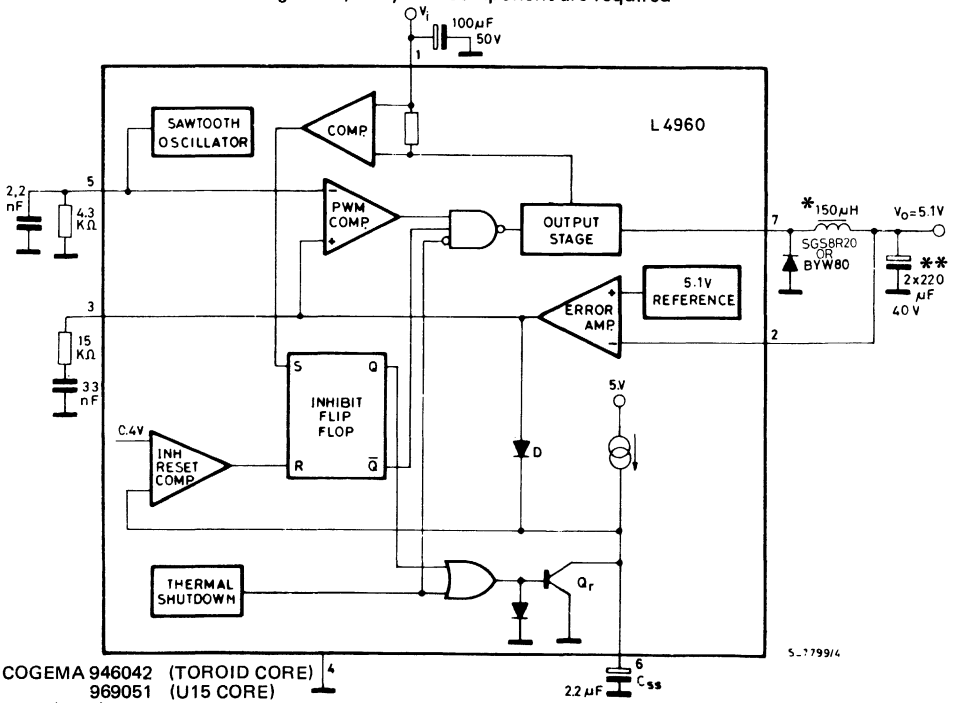
Fig. 25 - P.C. board and component layout of the Fig. 24 (1 : 1 scale)



Resistor values for standard output voltages		
V_o	R3	R4
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

APPLICATION INFORMATION (continued)

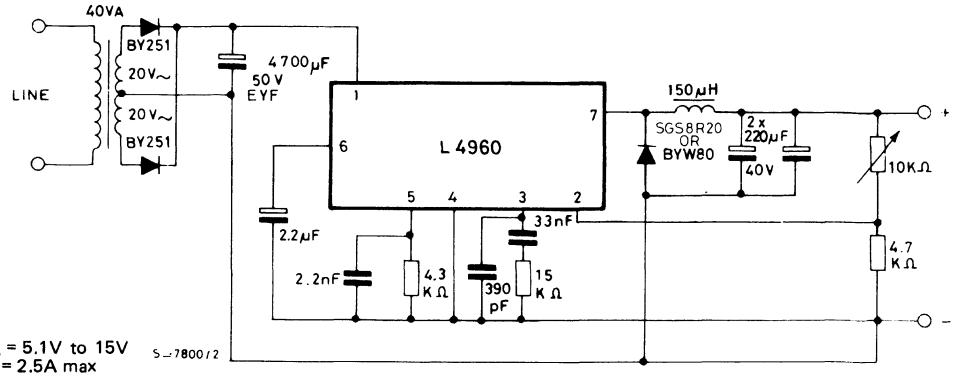
Fig. 26 - A minimal 5.1V fixed regulator; Very few component are required



* COGEMA 946042 (TOROID CORE)
969051 (U15 CORE)

** EKR (ROE)

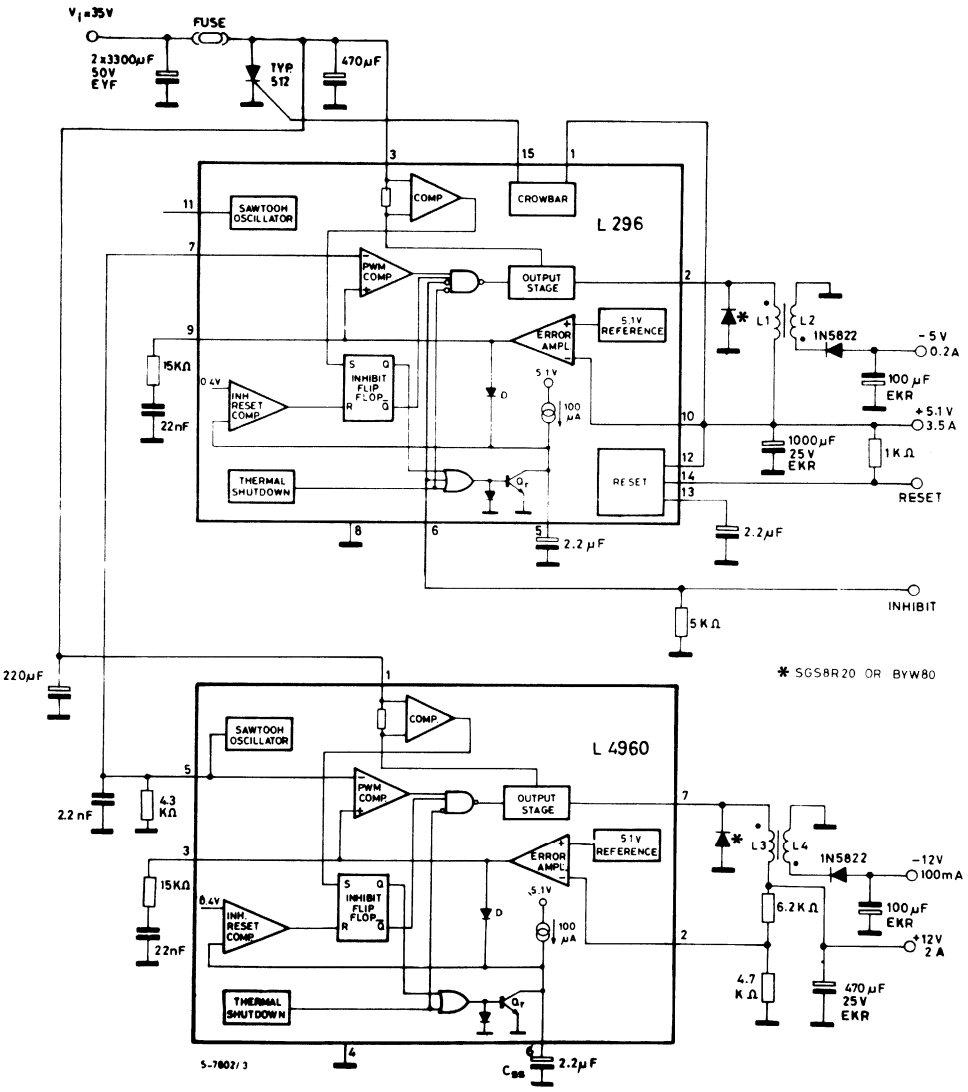
Fig. 27 - Programmable power supply



V_o = 5.1V to 15V
I_o = 2.5A max
Load regulation (1A to 2A) = 10mV (V_o = 5.1V)
Line regulation (220V ± 15% and to I_O = 1A) = 15mV (V_o = 5.1V)

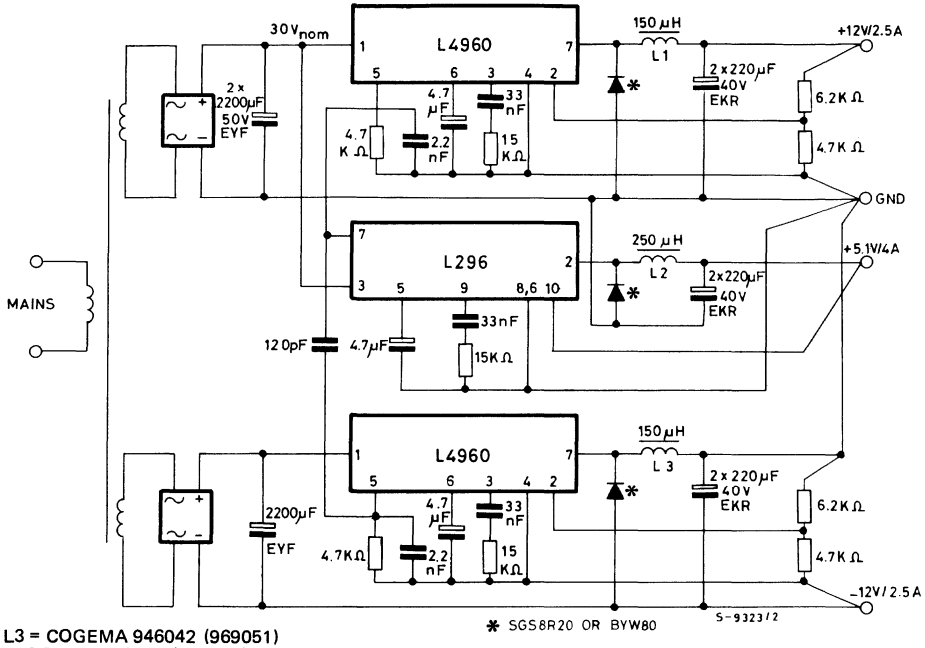
APPLICATION INFORMATION (continued)

Fig. 28 - Microcomputer supply with + 5.1V, -5V, +12V and -12V outputs



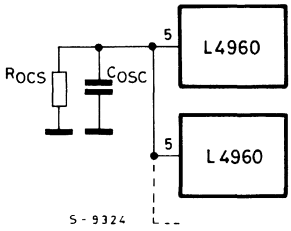
APPLICATION INFORMATION (continued)

Fig. 29 - DC-DC converter 5.1V/4A, ± 12V/2.5A; a suggestion how to synchronize a negative output



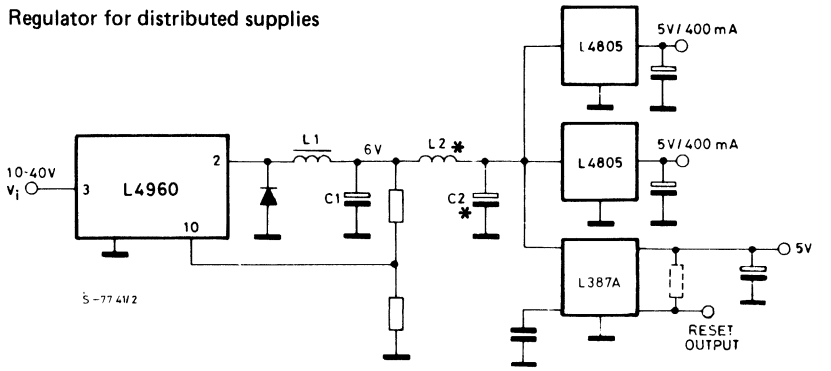
L1, L3 = COGEMA 946042 (969051)
L2 = COGEMA 946044 (946045)
D_1, D_2, D3 = SGS8R20 or BYW80

Fig. 30 - In multiple supplies several L4960s can be synchronized as shown



APPLICATION INFORMATION (continued)

Fig. 31 - Regulator for distributed supplies

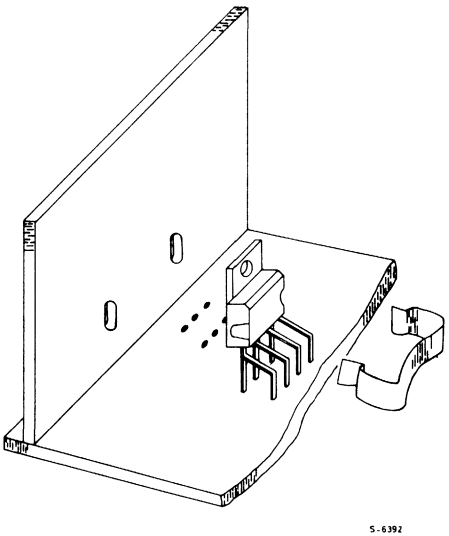


* L2 and C2 are necessary to reduce the switching frequency spikes when linear regulators are remote from L4960

MOUNTING INSTRUCTION

The power dissipated in the circuit must be removed by adding an external heatsink.
Thanks to the Heptawatt package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact, no electrical isolation is needed between the two surfaces.

Fig. 32 - Mounting example



L4962

PRELIMINARY DATA

1.5A POWER SWITCHING REGULATOR

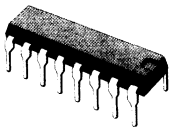
- 1.5A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- PRECISE (± 2 %) ON-CHIP REFERENCE
- HIGH SWITCHING FREQUENCY
- VERY HIGH EFFICIENCY (UP TO 90%)
- VERY FEW EXTERNAL COMPONENTS
- SOFT-START
- INTERNAL LIMITING CURRENT
- THERMAL SHUTDOWN

The L4962 is a monolithic power switching regulator delivering 1.5A at a voltage veriable from 5V to 40V in step down configuration.

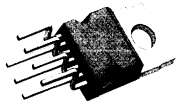
Features of device include current limiting, soft start, thermal protection and 0 to 100% duty cycle for continuous operating mode.

The L4962 is mounted in a 16-lead Powerdip plastic package and Heptawatt package and requires very few external components.

Efficient operation at switching frequencies up to 150KHz allows a reduction in the size and cost of external filter components.



Powerdip
(12 + 2 + 2)



Heptawatt

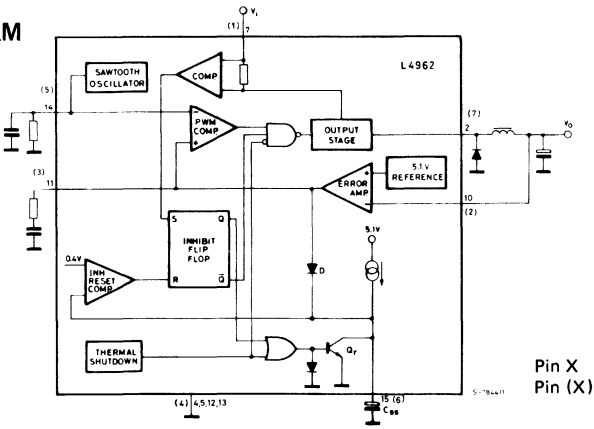
ORDERING NUMBER:

L4962 (12 + 2 + 2 Powerdip)
L4962E (Heptawatt)
L4962EH (Horizontal Heptawatt)

ABSOLUTE MAXIMUM RATINGS

V_7	Input voltage	50	V
$V_7 - V_2$	Input to output voltage difference	50	V
V_2	Negative output DC voltage	-1	V
	Output peak voltage at t = 0.1μs, f = 100KHz	-5	V
V_{11}, V_{15}	Voltage at pin 11, 15	5.5	V
V_{10}	Voltage at pin 10	7	V
I_{11}	Pin 11 sink current	1	mA
I_{14}	Pin 14 source current	20	mA
P_{tot}	Power dissipation at $T_{pins} \leqslant 90°C$ (Powerdip)	4.3	W
	$T_{case} \leqslant 90°C$ (Heptawatt)	15	W
T_j, T_{stg}	Junction and storage temperature	-40 to 150	°C

BLOCK DIAGRAM

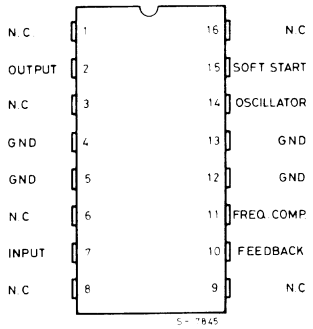


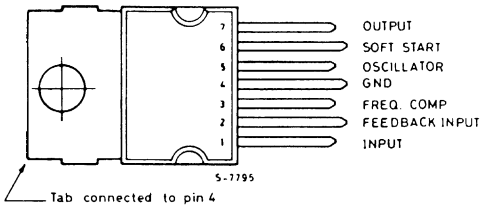
Pin X = Powerdip
Pin (X) = Heptawatt

L4962

CONNECTION DIAGRAMS

(Top view)





THERMAL DATA

			Heptawatt	Powerdip
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4°C/W	–
$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins	max	–	14°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50°C/W	80°C/W*

* Obtained with the GND pins soldered to printed circuit with minimized copper area.

PIN FUNCTIONS

HEPTAWATT	POWERDIP	NAME	FUNCTION
1	7	SUPPLY VOLTAGE	Unregulated voltage input. An internal regulator powers the internal logic.
2	10	FEEDBACK INPUT	The feedback terminal of the regulation loop. The output is connected directly to this terminal for 5.1V operation; it is connected via a divider for higher voltages.
3	11	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
4	4, 5, 12, 13	GROUND	Common ground terminal.
5	14	OSCILLATOR	A parallel RC network connected to this terminal determines the switching frequency. This pin must be connected to pin 7 input when the internal oscillator is used.
6	15	SOFT START	Soft start time constant. A capacitor is connected between this terminal and ground to define the soft start time constant. The capacitor also determines the average short circuit output current.
7	2	OUTPUT	Regulator output.
	1, 3, 6, 8, 9, 16		N.C.

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_j = 25°C, V_I = 35V, unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTICS							
V_o	Output voltage range	V_I = 46V	I_o = 1A	V_{ref}		40	V
V_I	Input voltage range	$V_o = V_{ref}$ to 36V	I_o = 1.5A	9		46	V
ΔV_o	Line regulation	V_I = 10V to 40V $V_o = V_{ref}$	I_o = 1A		15	50	mV
ΔV_o	Load regulation	$V_o = V_{ref}$	I_o = 0.5A to 1.5A		8	20	mV
V_{ref}	Internal reference voltage (pin 10)	V_I = 9V to 46V	I_o = 1A	5	5.1	5.2	V
$\frac{\Delta V_{ref}}{\Delta T}$	Average temperature coefficient of refer. voltage	T_j = 0°C to 125°C I_o = 1A			0.4		mV/°C
V_d	Dropout voltage	I_o = 1.5A			1.5	2	V
I_{om}	Maximum operating load current	V_i = 9V to 46V $V_o = V_{ref}$ to 36V		1.5			A
I_{2L}	Current limiting threshold (pin 2)	V_I = 9V to 46V $V_o = V_{ref}$ to 36V		2		3.3	A
I_{SH}	Input average current	V_I = 46V; output short-circuit			15	30	mA
η	Efficiency	f = 100KHz	$V_o = V_{ref}$		70		%
		I_o = 1A	V_o = 12V		80		%
SVR	Supply voltage ripple rejection	$\Delta V_I = 2V_{rms}$ f_{ripple} = 100Hz $V_o = V_{ref}$	I_o = 1A	50	56		dB
f	Switching frequency			85	100	115	KHz
$\frac{\Delta f}{\Delta V_I}$	Voltage stability of switching frequency	V_I = 9V to 46V			0.5		%
$\frac{\Delta f}{\Delta T_j}$	Temperature stability of switching frequency	T_j = 0°C to 125°C			1		%
f_{max}	Maximum operating switching frequency	$V_o = V_{ref}$	I_o = 1A	120	150		KHz
T_{sd}	Thermal shutdown junction temperature				150		°C

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
DC CHARACTERISTICS							
I_{7Q}	Quiescent drain current	100% duty cycle pins 2 and 14 open	V_I = 46V		30	40	mA
		0% duty cycle			15	20	mA
$-I_{2L}$	Output leakage current	0% duty cycle				1	mA
SOFT START							
I_{15SO}	Source current			100	130	160	μA
I_{15SI}	Sink current			50	70	120	μA
ERROR AMPLIFIER							
V_{11H}	High level output voltage	V_{10} = 4.7V	I_{11} = 100μA	3.5			V
V_{11L}	Low level output voltage	V_{10} = 5.3V	I_{11} = 100μA			0.5	V
I_{11SI}	Sink output current	V_{10} = 5.3V		100	150		μA
$-I_{11SO}$	Source output current	V_{10} = 4.7V		100	150		μA
I_{10}	Input bias current	V_{10} = 5.2V			2	10	μA
G_v	DC open loop gain	V_{11} = 1V to 3V		46	55		dB
OSCILLATOR							
$-I_{14}$	Oscillator source current			5			mA

CIRCUIT OPERATION (refer to the block diagram)

The L4962 is a monolithic stepdown switching regulator providing output voltages from 5.1V to 40V and delivering 1.5A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1V on-chip reference (zener zap trimmed to ± 2%).

This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage.

The gain and frequency stability of the loop can be adjusted by an external RC network connected to pin 11. Closing the loop directly gives an output voltage of 5.1V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor C_{ss} and allowed to rise, linearly, as this capacitor is charged by a constant current source. Output overload protection is provided in the form of a current limiter. The load current is sensed by a internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4V.

The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network. The thermal overload circuit disables circuit operation when the junction temperature reaches about 150°C and has hysteresis to prevent unstable conditions.

Fig. 1 - Soft start waveforms

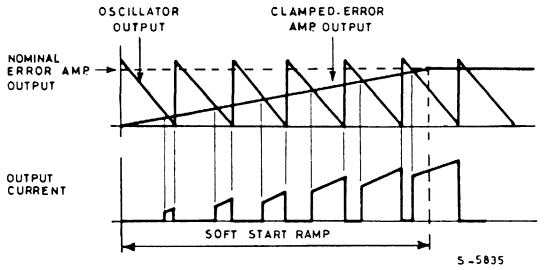


Fig. 2 - Current limiter waveforms

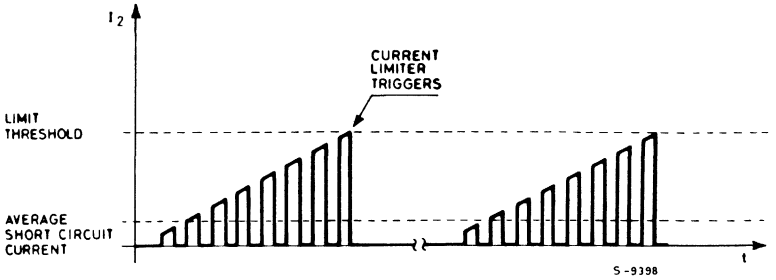
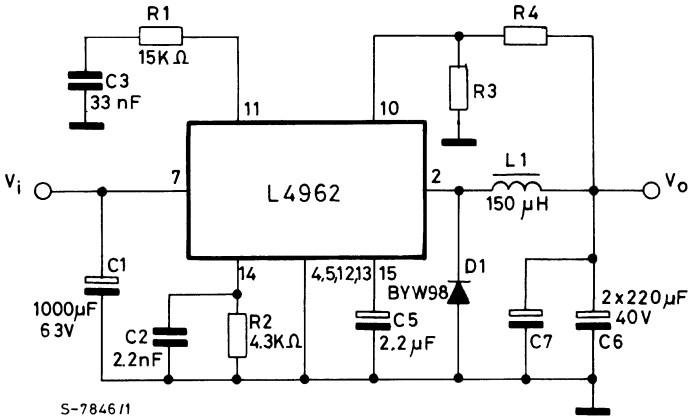


Fig. 3 - Test and application circuit (Powerdip)



1) D_1: BYW98 or 3A Schottky diode, 45V of VRRM;
2) L_1: CORE TYPE - MAGNETICS 58120 - A2 MPP
   N° TURNS 45, WIRE GAUGE: 0.8mm (20 AWG)
3) C_6, C_7: ROE, EKR 220μF 40V

Fig. 4 - Quiescent drain current vs. supply voltage (0% duty cycle)

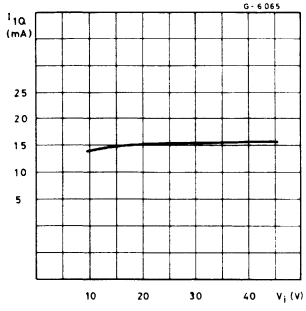


Fig. 5 - Quiescent drain current vs. supply voltage (100% duty cycle)

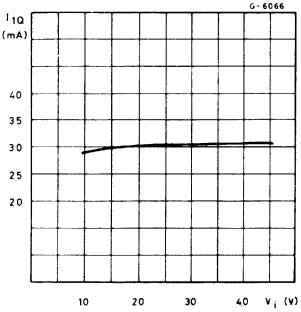


Fig. 6 - Quiescent drain current vs. junction temperature (0% duty cycle)

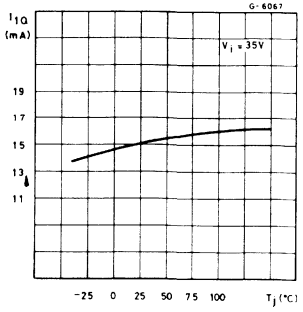


Fig. 7 - Quiescent drain current vs. junction temperature (100% duty cycle)

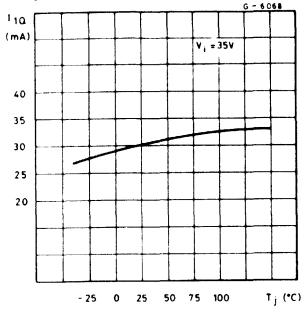


Fig. 8 - Reference voltage (pin 10) vs. V_I rdip) vs. V_I

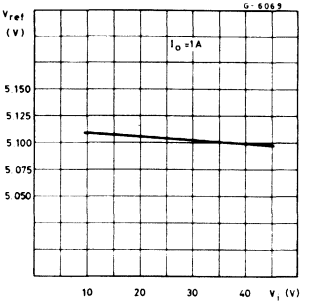


Fig. 9 - Reference voltage (pin 10) vs. junction temperature

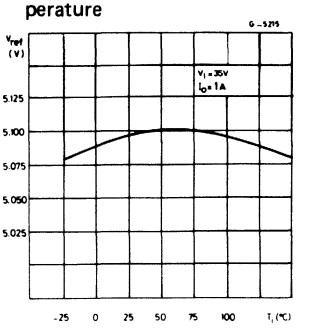


Fig. 10 - Open loop frequency and phase response of error amplifier

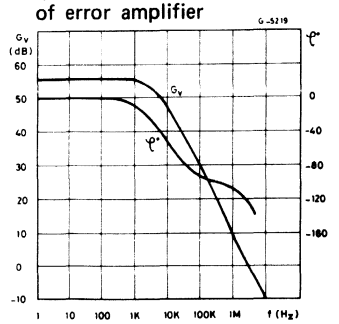


Fig. 11 - Switching frequency vs. input voltage

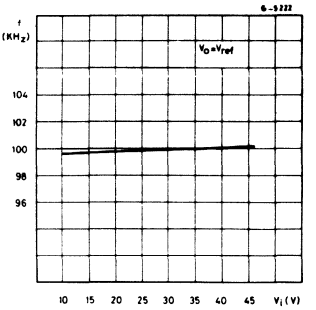


Fig. 12 - Switching frequency vs. junction temperature

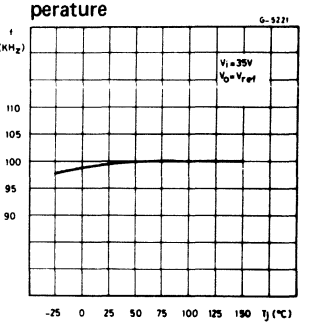


Fig. 13 - Switching frequency vs. R2 (see test circuit)

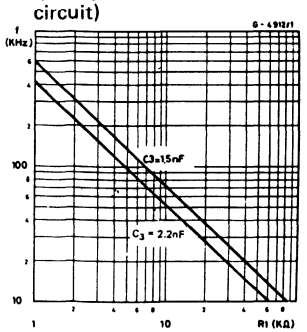


Fig. 14 - Line transient response

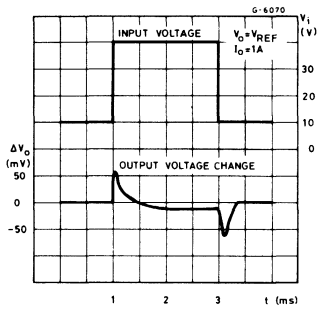


Fig. 15 - Load transient response

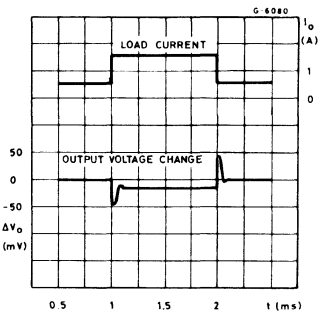


Fig. 16 - Supply voltage ripple rejection vs. frequency

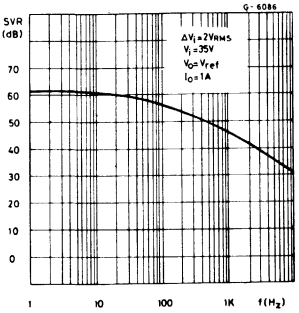


Fig. 17 - Dropout voltage between pin 7 and pin 2 vs. current at pin 2

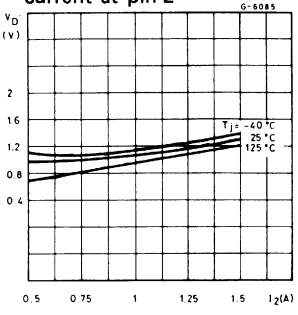


Fig. 18 - Dropout voltage between pin 7 and 2 vs. junction temperature

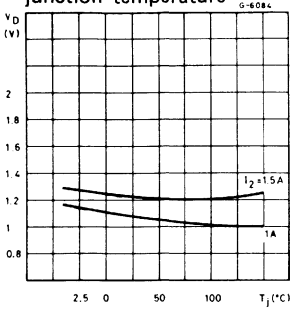


Fig. 19 - Efficiency vs. output current

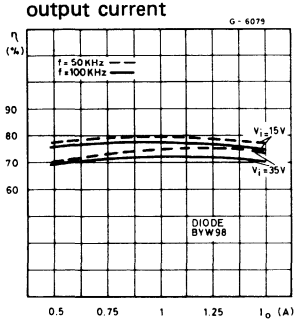


Fig. 20 - Efficiency vs. output current

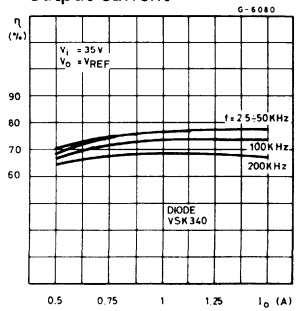


Fig. 21 - Efficiency vs. output current

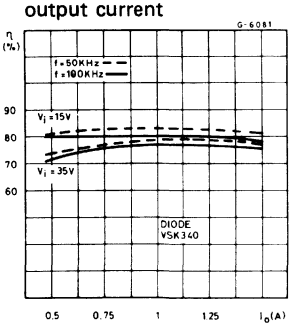


Fig. 22 - Efficiency vs. output voltage

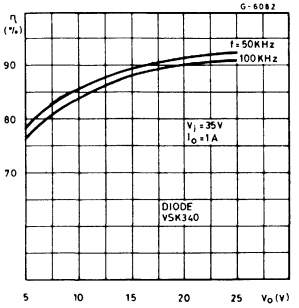


Fig. 23 - Efficiency vs. output voltage

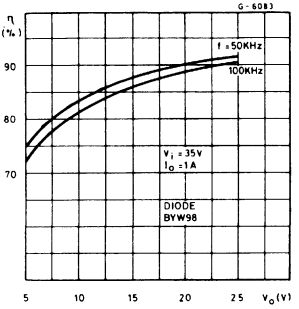
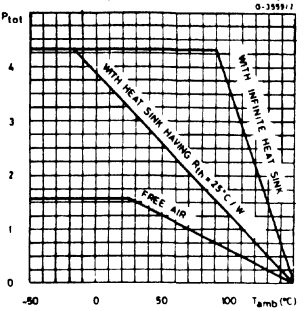
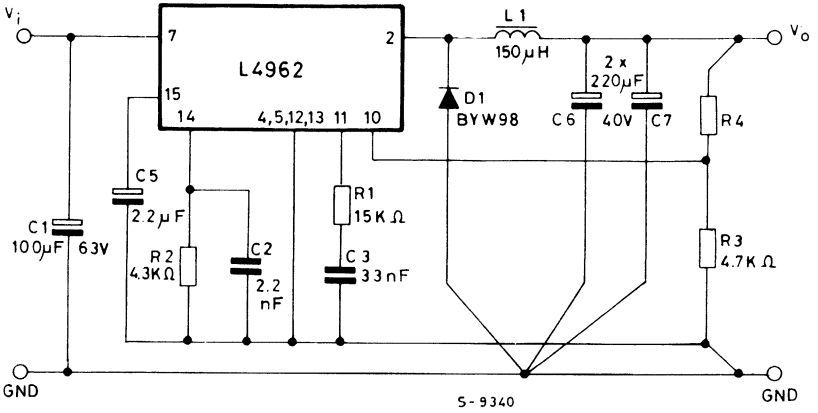


Fig. 24 - Maximum allowable power dissipation vs. ambient temperature (Powerdip)



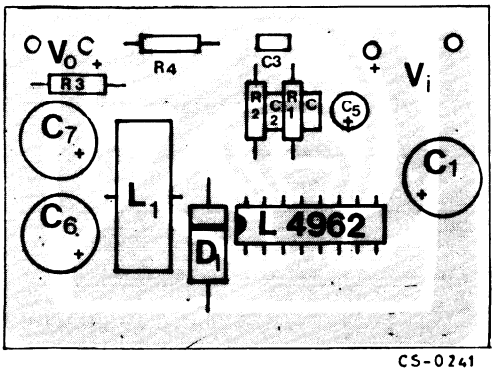
APPLICATION INFORMATION

Fig. 25 - Typical application circuit



C_1, C_6, C_7: EKR (ROE)
D_1: BYW98 OR VISK340 (SCHOTTKY)
SUGGESTED INDUCTORS (L_1): MAGNETICS 58120 - A2MPP - 45 TURNS - WIRE GAUGE 0.8mm (20AWG) - COGEMA 946043
OR U15, GUP15, 60 TURNS 1mm, AIR GAP 0.8mm (20AWG) - COGEMA 969051

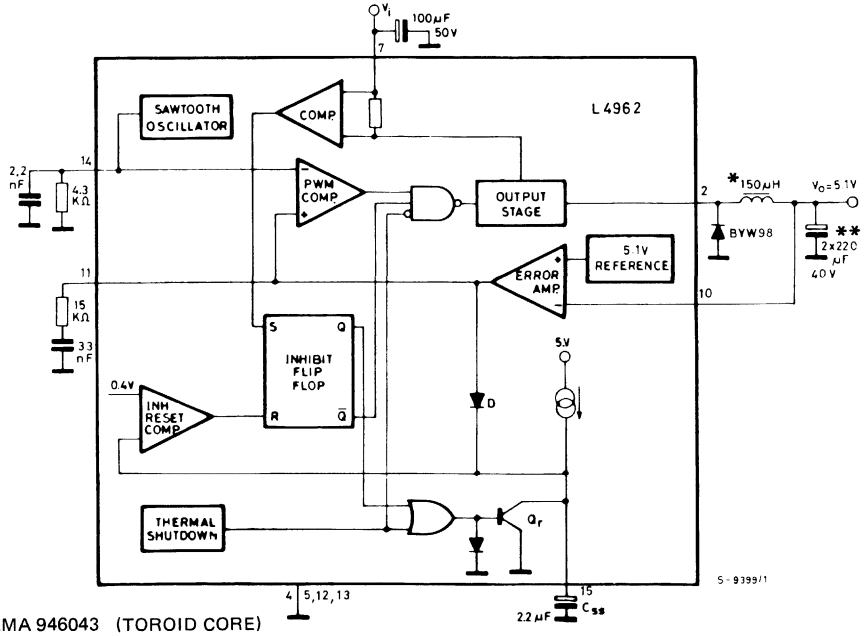
Fig. 26 - P.C. board and component layout of the circuit of Fig. 25 (1 : 1 scale)



Resistor values for standard output 7 voltages		
V_o	R3	R4
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

APPLICATION INFORMATION (continued)

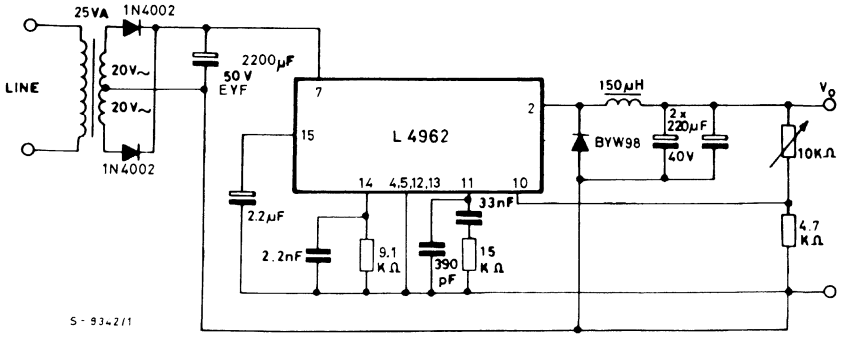
Fig. 27 - A minimal 5.1V fixed regulator; very few components are required



* COGEMA 946043 (TOROID CORE)
969051 (U15 CORE)

** EKR (ROE)

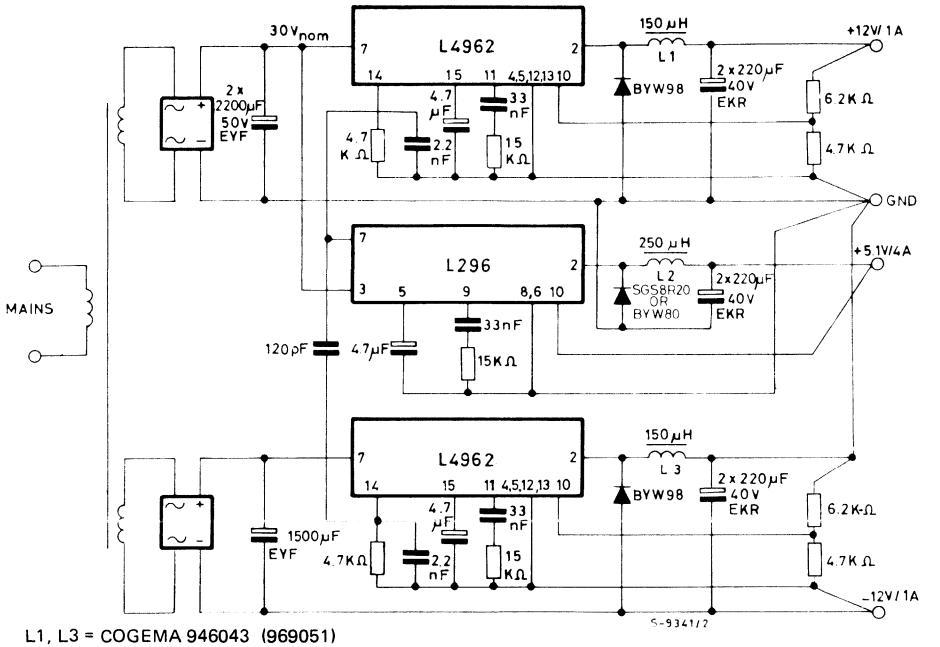
Fig. 27 - Programmable power supply



V_O = 5.1V to 15V
I_O = 1.5A max
Load regulation (0.5A to 1.5A) = 10mV (V_O = 5.1V)
Line regulation (220V ± 15% and to I_O = 1A) = 15mV (V_O = 5.1V)

APPLICATION INFORMATION (continued)

Fig. 29 - DC-DC converter 5.1V/4A, ± 12V/1A. A suggestion how to synchronize a negative output



L1, L3 = COGEMA 946043 (969051)
L2 = COGEMA 946044 (946045)

Fig. 30 - In multiple supplies several L4962s can be synchronized as shown

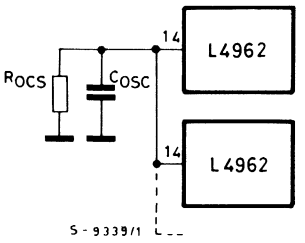
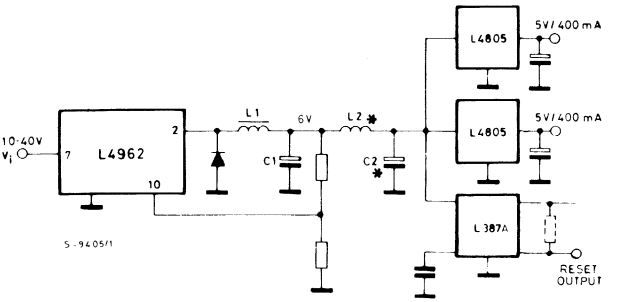


Fig. 31 - Preregulator for distributed supplies



* L2 and C2 are necessary to reduce the switching frequency spikes when linear regulators are remote from L4962

MOUNTING INSTRUCTION

The $R_{th\ j\text{-}amb}$ of the L4962 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 32).
The diagram of figure 33 shows the $R_{th\ j\text{-}amb}$ as a function of the side "ℓ" of two equal square copper areas having the thickness of 35μ (1.4 mils). During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.
The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 32 - Example of P.C. board copper area which is used as heatsink

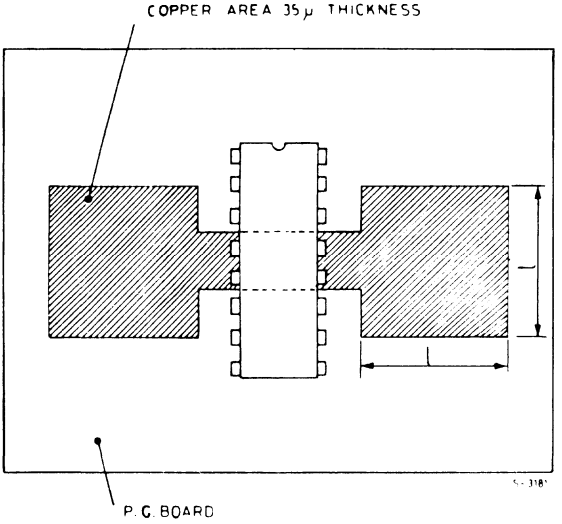
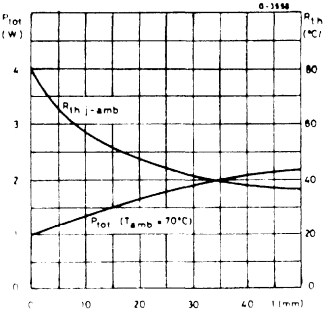


Fig. 33 - Maximum dissipable power and junction to ambient thermal resistance vs. side "ℓ"



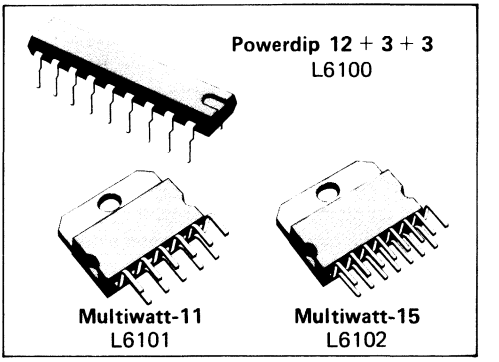
100V-1A, QUAD DMOS POWER SWITCH

The L6100, L6101 and L6102 are DMOS quad transistor array realized with a new process called Multipower-BCD which allows the integration of multiple isolated DMOS transistors - plus bipolar linear and CMOS logic circuits on a single chip.

Each of the four power DMOS transistors is a parallel combination of one thousand elementary cells with a packing density in excess of 1600 cells/mm^2.

The device is assembled in three package: 12+3+3 lead powerdip; 11-lead Multiwatt® and 15-lead Multiwatt®.

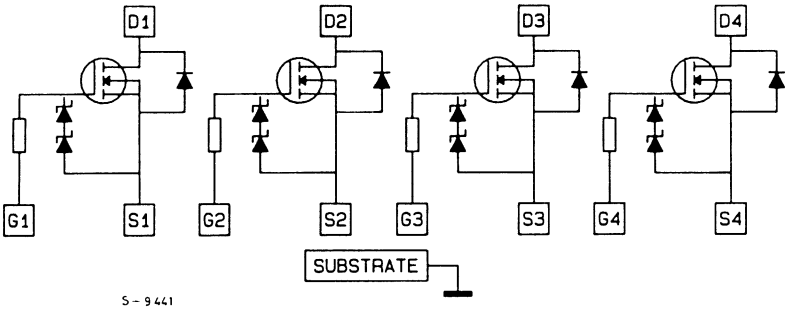
MultiPower BCD Technology



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage	100	V
V_{DGR}	Drain-gate voltage (R_{GS} = 14KΩ)	100	V
V_{GS}	Gate-source voltage	+14 to -0.6	V
I_D	Drain current		
	– DC operation	1	A
	– Pulsed (300μs, 1% duty cycle)	2.5	A
T_{stg}, T_j	Storage and junction temperature range	-40 to +150	°C

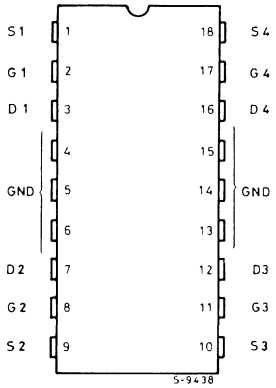
SCHEMATIC DIAGRAM



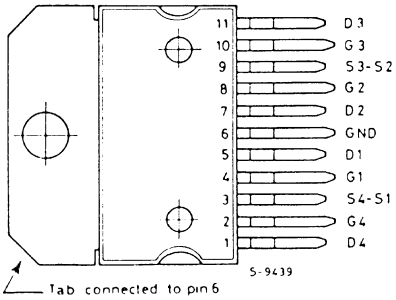
S-9441

CONNECTION DIAGRAMS
(Top view)

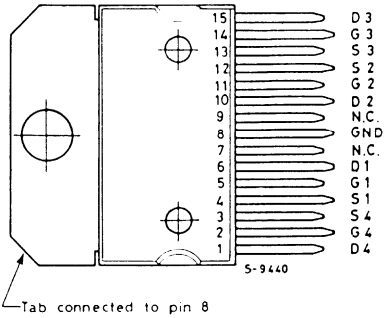
L6100
(Powerdip)



L6101
(Multiwatt-11)



L6102
(Multiwatt-15)



THERMAL DATA

			Powerdip	Multiwatt-11	Multiwatt-15
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	65°C/W	35°C/W	35°C/W
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	11°C/W	3°C/W	3°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-source breakdown voltage	@ I_D = 1mA V_{GS} = 0V	100			V
V_{GS} (TH)	Threshold voltage	@ I_D = 1mA V_{GS} = V_{DS}	2		4	V
I_{GSS}	Gate-source leakage	@ V_{GSS} = 10V			1	μA
R_{DS} (ON)	Static drain-source on-state resistance	@ V_{GS} = 10V I_D = 1A			1.2	Ω

Fig. 1 - Saturation characteristics

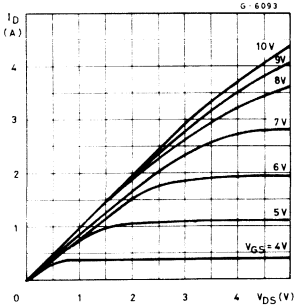


Fig. 2 - Normalized ON-resistance vs. temperature

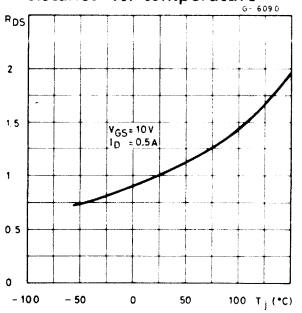


Fig. 3 - Transconductance vs. drain current

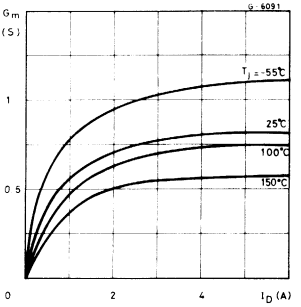
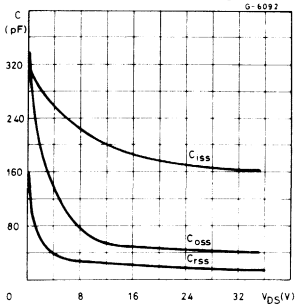


Fig. 4 - Capacitance vs. drain to source voltage



L6221A
L6221N

ADVANCE DATA

QUAD DARLINGTON SWITCHES

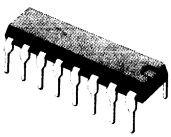
- OUTPUT VOLTAGE TO 50V
- OUTPUT CURRENT TO 1.8A
- VERY LOW SATURATION VOLTAGE
- TTL COMPATIBLE INPUTS
- INTEGRAL FAST RECIRCULATION DIODES

The L6221 monolithic quad darlington switch is designed for high current, high voltage switching applications. Each of the four switches is controlled by a logic input and all four are controlled by a common enable input. All inputs are TTL-compatible for direct connection to logic circuits.

Each switch consists of an open-collector darlington transistor plus a fast diode for switching applications with inductive loads. The emitters of the four switches are commoned. Any number of inputs and outputs of the same device may be paralleled.

Two versions are available: the L6221A mounted in a Powerdip 12+2+ 2 package and the L6221N mounted in a 15-lead Multiwatt package.

Multiwatt 15

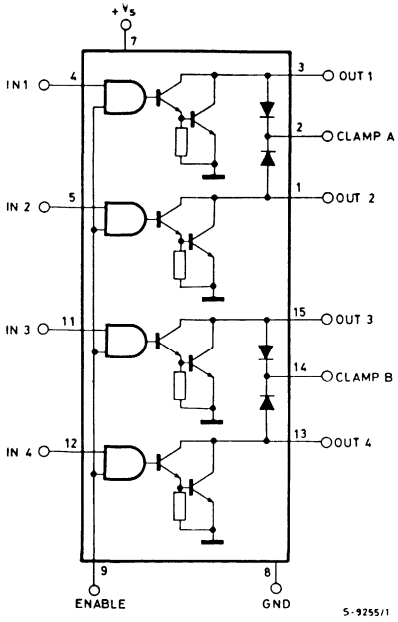


Powerdip 12+2+2

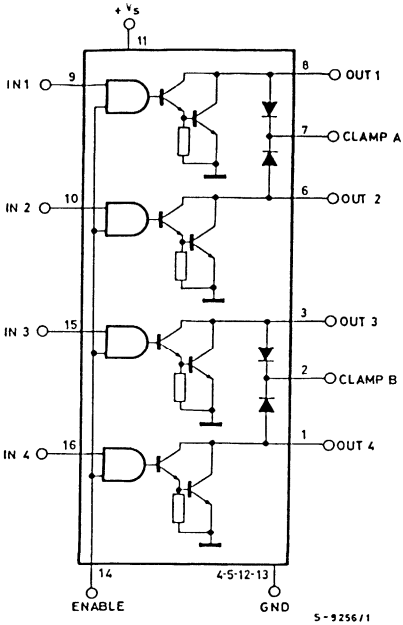
ORDERING NUMBER :

L6221N L6221A

BLOCK DIAGRAMS



L6221N
Multiwatt



L6221A
Powerdip

ABSOLUTE MAXIMUM RATINGS

V_o	Output voltage	50	V
V_{SS}	Logic supply voltage	7	V
V_i	Input voltage	V_{SS}	
I_C	Collector current	1.8	A
I_C	Collector peak current (repetitive, duty cycle = 1% t_{on} = 10ms)	2.5	A
I_C	Collector peak current (non repetitive, t = 10μs)	3.2	A
T_{op}	Operating temperature range (junction)	-40 to +150	°C
T_{stg}	Storage temperature range	-55 to +150	°C
I_{sub}	Output substrate current	350	mA

THERMAL DATA

			Powerdip	Multiwatt
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80°C/W	35°C/W
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	14°C/W	3°C/W

TRUTH TABLE

Enable	Input	Power out
H	H	ON
H	L	OFF
L	X	OFF

For each input: H = High level
L = Low level
X = Don't care

PIN FUNCTIONS

L6221N Multiwatt	L6221A Powerdip	Name	Function
4	9	IN 1	Input to driver 1
5	10	IN 2	Input to driver 2
3	8	OUT 1	Output of driver 1
1	6	OUT 2	Output of driver 2
2	7	CLAMP A	Diode clamp to driver 1 and driver 2
11	15	IN 3	Input to driver 3
12	16	IN 4	Input to driver 4
15	3	OUT 3	Output of driver 3
13	1	OUT 4	Output of driver 4
14	2	CLAMP B	Diode clamp to driver 3 and driver 4
9	14	ENABLE	Enable input to all drivers
7	11	V_{SS}	Logic supply voltage
8	4	GND	Ground
–	5	GND	Ground
–	12	GND	Ground
–	13	GND	Ground
6	–	NC	Not connected
10	–	NC	Not connected

ELECTRICAL CHARACTERISTICS (V_{SS} = 5V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_{SS}	Logic supply voltage			4.5		7	V
$V_{CE(sus)}$	Output sustaining voltage	V_{IN} = 0.8V V_{EN} = 5V I_C = 100mA		46			V
I_{CEX}	Output leakage current	V_{CE} = 50V V_{IN} = 0.8V V_{EN} = 5V				1	mA
$V_{CE(sat)}$	Collector emitter saturation voltage (One input on; all other inputs off.)	I_C = 0.6A	V_{SS} = 4.5V V_{IN} = 2V V_{EN} = 4.5V			1	V
		I_C = 1A				1.2	V
		I_C = 1.8A				1.8	V
V_{IL}	Input low voltage					0.8	V
I_{IL}	Input low current	V_{IN} = 0.4V				-100	µA
V_{IH}	Input high voltage			2.0			V
I_{IH}	Input high current	V_{IN} = 2.0V				± 10	µA
I_s	Logic supply current		All outputs ON I_C = 0.7A			20	mA
			All outputs OFF			20	mA
I_R	Clamp diode leakage current	V_R = 50V V_{IN} = 0.8V V_{EN} = 5V				100	µA
V_F	Clamp diode forward voltage	I_F = 1A				1.6	V
		I_F = 1.8A				2.0	V
t_{on}	Turn on time	V_S = 5V R_L = 10Ω				2	µs
t_{off}	Turn off time	V_S = 5V R_L = 10Ω				5	µs
ΔI_s	Logic supply current variation	V_{IN} = 5V, V_{EN} = 5V, V_{SS} = 5V I_{out} = - 300mA for each channel				120	mA

L6222

ADVANCE DATA

QUAD TRANSISTOR SWITCH

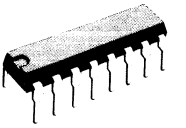
- OUTPUT VOLTAGE TO 50V
- OUTPUT CURRENT TO 1.2A
- VERY LOW SATURATION VOLTAGE
- TTL COMPATIBLE INPUTS
- INTEGRAL SUPPRESSION DIODE

The L6222 monolithic quad transistor switch is designed for high current, high voltage switching applications.

Each of the four switches is controlled by a logic input and all four are controlled by a common enable input. All inputs are TTL-compatible for direct connection to logic circuits. Each switch consists of an open-collector transistor plus a clamp diode for applications with inductive loads.

The emitters of the four switches are commoned. Any number of inputs and outputs of the same device may be paralleled.

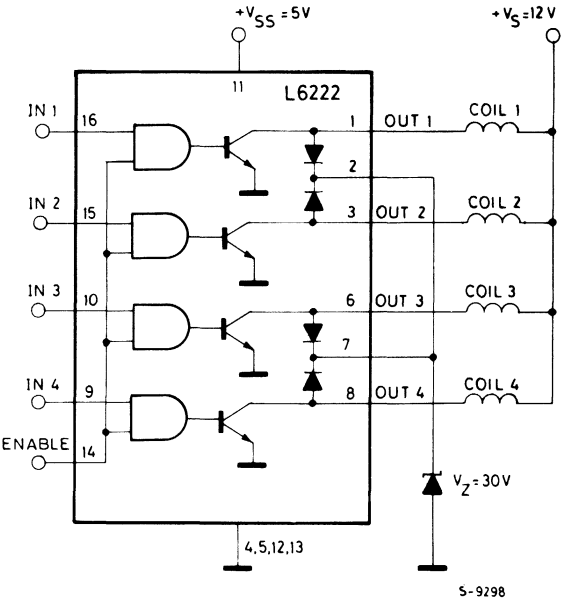
This device is intended to drive coils such as relays, solenoids, unipolar stepper motors, LED, etc.



Powerdip
12 + 2 + 2

ORDERING NUMBER: L6222

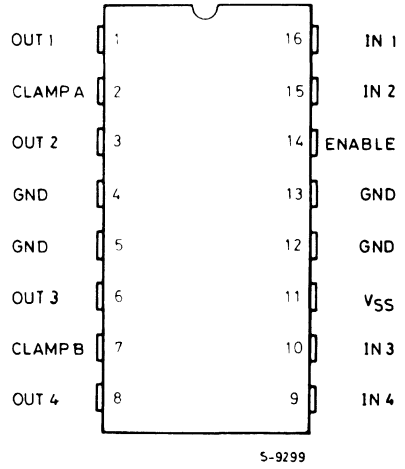
Fig. 1 - Unipolar stepper motor drive



ABSOLUTE MAXIMUM RATINGS

V_s	Output voltage	50	V
V_{ss}	Logic supply voltage	7	V
V_{IN}	Input voltage	15	V
I_C	Collector current (PEAK)	1.2	A
T_{op}	Operating temperature range (junction)	-40 to +150	°C
T_{stg}	Storage temperature range	-55 to +150	°C

CONNECTION DIAGRAM
(Top view)



TRUTH TABLE

Enable	Input	Power out
H	H	ON
H	L	OFF
L	X	OFF

For each input: H = High level
L = Low level
X = Don't care

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	14	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_{SS}	Logic supply voltage			4.50		7	V
$V_{CE(sus)}$	Output sustaining voltage	V_{IN} = 0.8V I_C = 100mA		46			V
I_{CEX}	Output leakage current	V_{CE} = 50V V_{IN} = 0.8V				1	mA
$V_{CE(sat)}$	Collector emitter saturation voltage	$V_{IN} \geqslant$ 2.0V	I_C = 0.1A			0.2	V
			I_C = 0.4A			0.5	
			I_C = 0.7A			0.9	
V_{IL}	Input low voltage					0.8	V
I_{IL}	Input low current	V_{IN} = 0.4V				-100	μA
V_{IH}	Input high voltage			2.0			V
I_{IH}	Input high current	$V_{IN} \geqslant$ 2.0V				± 10	μA
I_S	Logic supply current	V_{SS} = 5V	All outputs ON I_C = 0.7A		50	85	mA
			All outputs OFF		8		mA
I_R	Clamp diode leakage current	V_R = 50V				100	μA
V_F	Clamp diode forward voltage	I_F = 0.7A				1.6	V
		I_F = 1.2A				2.0	

L7150
L7152

PRELIMINARY DATA

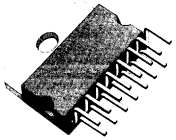
50V QUAD DARLINGTON SWITCHES

- FOUR NPN DARLINGTONS WITH ISOLATED CONNECTIONS
- OUTPUT CURRENT TO 1.5A EACH DARLINGTON
- MINIMUM BREAKDOWN 50V
- SUSTAINING VOLTAGE AT LEAST 35V
- MULTIWATT PACKAGE ALLOWS OPERATION AT 1.5A, 50V, 100% DUTY CYCLE, ALL FOUR DEVICES ON
- INTEGRAL SUPPRESSION DIODES
- VERSIONS FOR 5V AND 6-15V LOGIC FAMILIES

The L7150 and L7152 are 1.5A quad darlington arrays mounted in the 15-lead Multiwatt® plastic package. Each darlington is equipped with a suppression diode for inductive loads and all three terminals are isolated. A minimum breakdown of 50V is specified and the minimum sustaining voltage is 35V, measured at 100mA.

The L7150 has 350Ω input resistors and is compatible with TTL, DTL, LSTTL and 5V CMOS logic. The L7152 has 3KΩ input resistors for use with 6-15V CMOS and PMOS logic.

These devices are suitable for driving a wide range of inductive and non-inductive loads including DC motors, stepper motors, solenoids, relays, lamps, multiplexed LEDs and heaters.



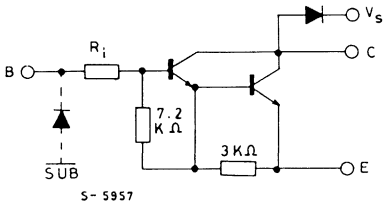
Multiwatt 15

ORDERING NUMBER: L7150
L7152

ABSOLUTE MAXIMUM RATINGS

V_{CEX}	Output voltage	50	V
$V_{CE(sus)}$	Output sustaining voltage	35	V
I_o	Output current	1.75	A
V_i	Input voltage	30	V
I_B	Input current	25	mA
P_{tot}	Power dissipation (T_{case} = 75°C)	25	W
T_{amb}	Operating ambient temperature range	0 to 70	°C
T_{stg}	Storage temperature	-55 to 150	°C

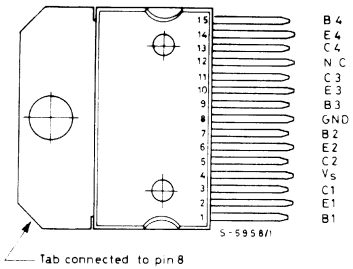
SCHEMATIC DIAGRAM



L7150 : R_{IN} = 350Ω
L7152 : R_{IN} = 3 KΩ

L7150
L7152

CONNECTION DIAGRAM
(top view)



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max.	35	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output leakage current	V_{CE} = 50V V_{CE} = 50V T_{amb} = 70°C			100 500	µA µA	1
$V_{CE(sus)}$	Collector-emitter sustaining voltage	I_C = 100mA V_i = 0.4V	35			V	2
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C = 500mA I_B = 625µA I_C = 750mA I_B = 935µA I_C = 1A I_B = 1.25mA I_C = 1.25A I_B = 2 mA			1.15 1.3 1.4 1.5	V V V V	3
$I_{i(on)}$	Input current	for **L7150** V_i = 2.4V for **L7150** V_i = 3.75V for **L7152** V_i = 5V for **L7152** V_i = 12V	**1.4** **3.3** **0.6** **1.7**		4.3 9.6 1.8 5.2	mA mA mA mA	4
$V_{i(on)}$	Input voltage	for **L7150** V_{CE} = 2V I_C = 1A V_{CE} = 2V I_C = 1.5A for **L7152** V_{CE} = 2V I_C = 1A V_{CE} = 2V I_C = 1.5A			 2 2.5 6.5 10	 V V V V	5
t_{PLH}	Turn-on delay time	0.5V_i to 0.5V_o			1	µs	
t_{PHL}	Turn-off delay time	0.5V_i to 0.5V_o			1.5	µs	

TEST CIRCUITS

Fig. 1

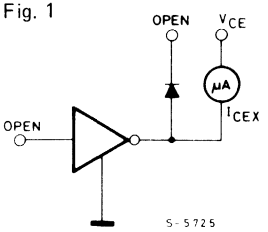


Fig. 2

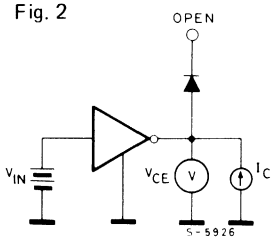


Fig. 3

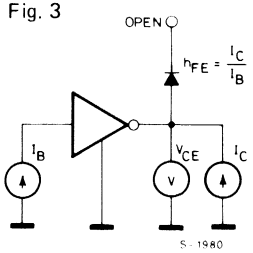


Fig. 4

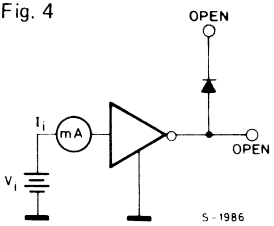
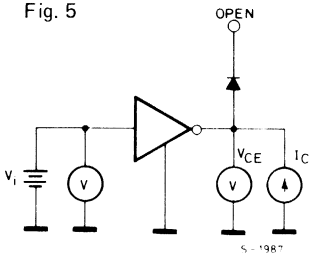


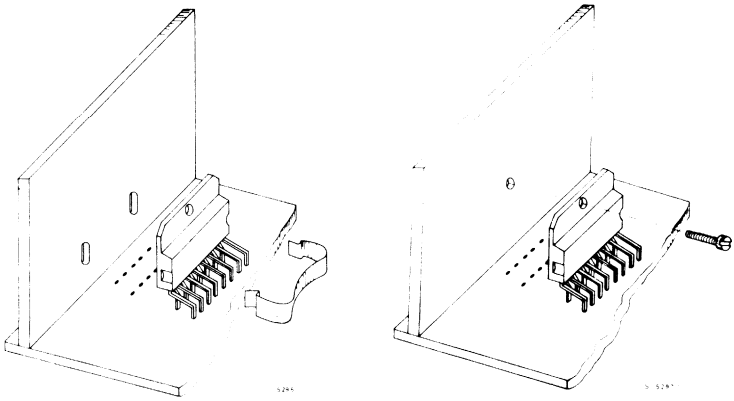
Fig. 5



MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.
Thanks to the Multiwatt® package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact; no electrical isolation is needed between the two surfaces.

Fig. 6 - Mounting example



L7180
L7182

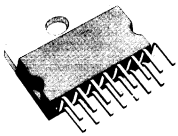
80V QUAD DARLINGTON SWITCHES

- FOUR NPN DARLINGTONS WITH ISOLATED CONNECTIONS
- OUTPUT CURRENT TO 1.5A EACH DARLINGTON
- MINIMUM BREAKDOWN 80V
- SUSTAINING VOLTAGE AT LEAST 50V
- MULTIWATT PACKAGE ALLOWS OPERATION AT 1.5A, 80V, 100% DUTY CYCLE, ALL FOUR DEVICES ON
- INTEGRAL SUPPRESSION DIODES
- VERSIONS FOR 5V AND 6-15V LOGIC FAMILIES

The L7180 and L7182 are 1.5A quad darlington arrays mounted in the 15-lead Multiwatt® plastic package. Each darlington is equipped with a suppression diode for inductive loads, and all three terminals are isolated. A minimum breakdown of 80V is specified and the minimum sustaining voltage is 50V.

The L7180 has 350Ω input resistors and is compatible with TTL, DTL, LSTTL and 5V CMOS logic. The L7182 has 3KΩ input resistors for use with 6-15V CMOS and PMOS logic.

These devices are suitable for driving a wide range of inductive and non-inductive loads including DC motors, stepper motors, solenoids, relays, lamps, multiplexed LEDs and heaters.



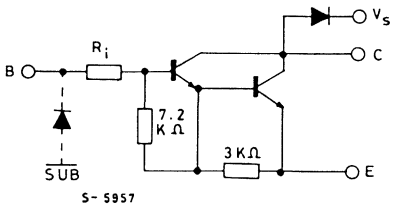
Multiwatt 15

ORDERING NUMBER: L7180
L7182

ABSOLUTE MAXIMUM RATINGS

V_{CEX}	Output voltage	80	V
$V_{CE\ (sus)}$	Output sustaining voltage	50	V
I_o	Output current	1.75	A
V_i	Input voltage	60	V
I_B	Input current	25	mA
P_{tot}	Power dissipation (T_{case} = 75°C)	25	W
T_{amb}	Operating ambient temperature range	0 to 70	°C
T_{stg}	Storage temperature	-55 to 150	°C

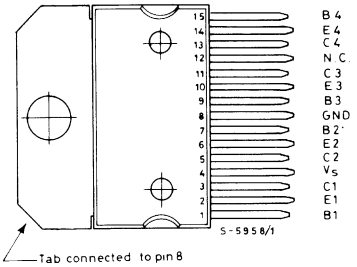
SCHEMATIC DIAGRAM

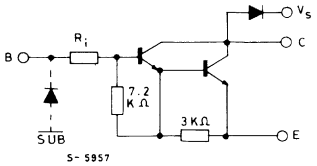


L7180 : R_{IN} = 350 Ω
L7182 : R_{IN} = 3 KΩ

L7180
L7182

CONNECTION AND SCHEMATIC DIAGRAMS
(top view)





L7180 : R_{IN} = 350 Ω
L7182 : R_{IN} = 3 KΩ

THERMAL DATA

$R_{thj\text{-}case}$	Thermal resistance junction-case	max.	3	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max.	35	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output leakage current	V_{CE} = 80V V_{CE} = 80V T_{amb} = 70°C			100 500	µA µA	1
$V_{CE(sus)}$	Collector-emitter sustaining voltage	I_C = 100mA V_i = 0.4V	50			V	2
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C = 500mA I_B = 625µA I_C = 750mA I_B = 935µA I_C = 1A I_B = 1.25mA I_C = 1.5A I_B = 2.25mA			**1.15** **1.3** **1.4** **1.6**	V V V V	3
$I_{i(on)}$	Input current	for **L7180** V_i = 2.4V for **L7180** V_i = 3.75V for **L7182** V_i = 5V for **L7182** V_i = 12V	**1.4** **3.3** **0.6** **1.7**		4.3 9.6 1.8 5.2	mA mA mA mA	4
$V_{i(on)}$	Input voltage	for **L7180** V_{CE} = 2V I_C = 1A V_{CE} = 2V I_C = 1.5A for **L7182** V_{CE} = 2V I_C = 1A V_{CE} = 2V I_C = 1.5A			 2 2.5 6.5 10	 V V V V	5
t_{PLH}	Turn-on delay time	0.5V_i to 0.5V_o			1	µs	
t_{PHL}	Turn-off delay time	0.5V_i to 0.5V_o			1.5	µs	

TEST CIRCUITS

Fig. 1

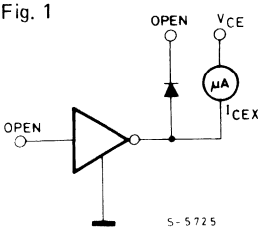


Fig. 2

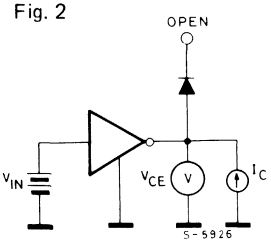


Fig. 3

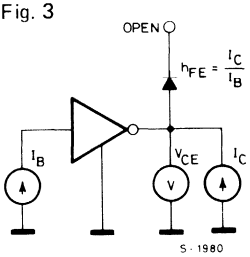


Fig. 4

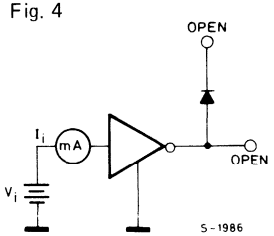
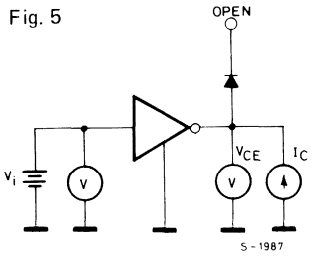


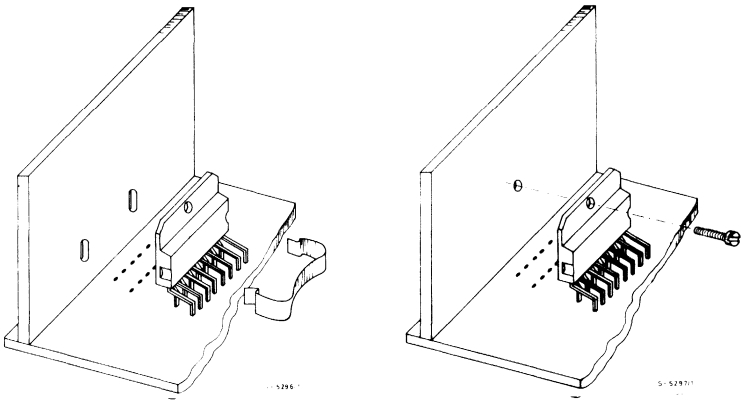
Fig. 5



MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.
Thanks to the Multiwatt® package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact; no electrical isolation is needed between the two surfaces.

Fig. 6 - Mounting example

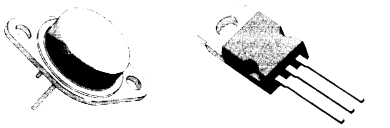


L7800 Series

POSITIVE VOLTAGE REGULATORS

- OUTPUT CURRENT UP TO 1.5A
- OUTPUT VOLTAGES OF 5; 6; 8; 12; 15; 18; 20; 24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR SOA PROTECTION

The L7800 series of three-terminal positive regulator is available in TO-220 and TO-3 packages and with several fixed output voltages making it useful in a wide range of applications. These regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

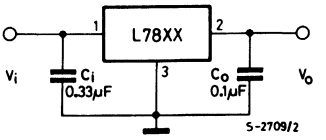


TO-3 TO-220

ABSOLUTE MAXIMUM RATINGS

V_i	DC input voltage (for V_o = 5 to 18V)	35	V
	(for V_o = 20, 24V)	40	V
I_o	Output current	internally limited	
P_{tot}	Power dissipation	internally limited	
T_{op}	Operating junction temperature (for **L7800**)	-55 to +150	°C
	(for **L7800C**)	0 to +150	°C
T_{stg}	Storage temperature	-65 to +150	°C

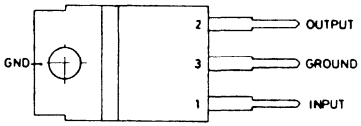
APPLICATION CIRCUIT

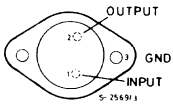


L7800 Series

CONNECTION DIAGRAMS AND ORDERING NUMBERS

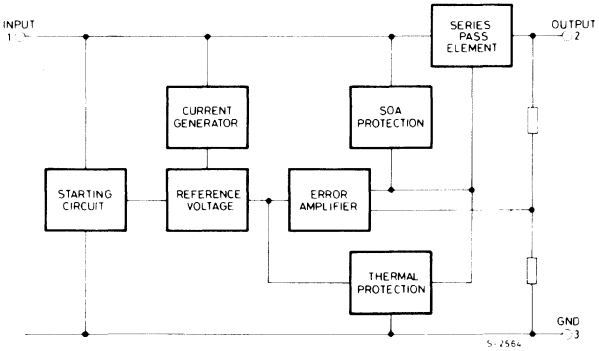
(top views)



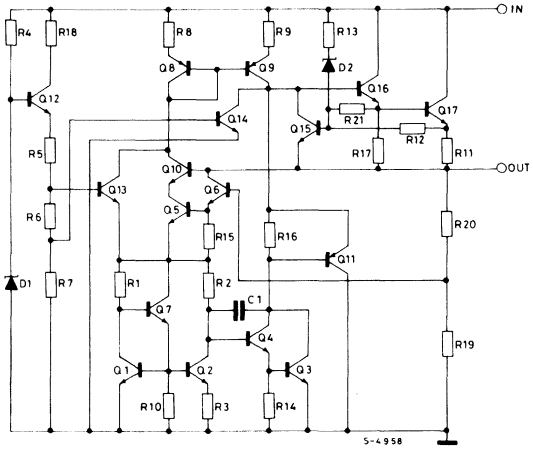


Type	TO-220	TO-3	Output voltage
L 7805	–	L 7805T	5V
L 7805C	L 7805CV	L 7805 CT	5V
L 7806	–	L 7806T	6V
L 7806C	L 7806 CV	L 7806CT	6V
L 7808	–	L 7808T	8V
L 7808C	L 7808 CV	L 7808CT	8V
L 7812	–	L 7812T	12V
L 7812C	L 7812CV	L 7812CT	12V
L 7815	–	L 7815T	15V
L 7815C	L 7815CV	L 7815CT	15V
L 7818	–	L 7818T	18V
L 7818C	L 7818CV	L 7818CT	18V
L 7820	–	L 7820T	20V
L 7820C	L 7820CV	L 7820CT	20V
L 7824	–	L 7824T	24V
L 7824C	L 7824CV	L 7824CT	24V

BLOCK DIAGRAM



SCHEMATIC DIAGRAM



TEST CIRCUITS

Fig. 1 - DC parameters

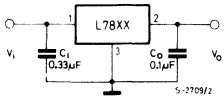


Fig. 2 - Load regulation

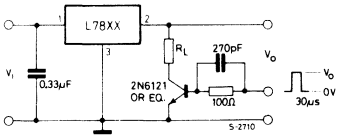
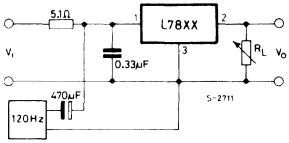


Fig. 3 - Ripple rejection



THERMAL DATA

			TO-220	TO-3
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3 °C/W	4 °C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50 °C/W	35 °C/W

ELECTRICAL CHARACTERISTICS L 7800 (Refer to the test circuits, T_j= -55 to 150°C, I_o = 500 mA, C_i = 0.33 μF, C_o= 0.1 μF unless otherwise specified)

OUTPUT VOLTAGE			5			6			8			12			Unit
INPUT VOLTAGE (Unless otherwise specified)			10			11			14			19			
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output voltage	T_j= 25°C	4.8	5	5.2	5.75	6	6.25	7.7	8	8.3	11.5	12	12.5	V
		I_o= 5 mA to 1A, $P_o \leq$ 15W	4.65	5	5.35 (V_i= 8 to 20V)	5.65	6	6.35 (V_i= 9 to 21V)	7.6	8	8.4 (V_i= 11.5 to 23V)	11.4	12	12.6 (V_i= 15.5 to 27V)	
ΔV_o	Line regulation	T_j= 25°C			50 (V_i= 7 to 25V)			60 (V_i= 8 to 25V)			80 (V_i= 10.5 to 25V)			120 (V_i= 14.5 to 30V)	mV
					25 (V_i= 8 to 12V)			30 (V_i= 9 to 13V)			40 (V_i= 11 to 17V)			60 (V_i= 16 to 22V)	
ΔV_o	Load regulation	T_j= 25°C, I_o= 5 mA to 1.5A			100			100			100			120	mV
		T_j= 25°C, I_o= 250 to 750 mA			25			30			40			60	
I_d	Quiescent current	T_j= 25°C			6			6			6			6	mA
ΔI_d	Quiescent current change	I_o= 5 mA to 1A			0.5			0.5			0.5			0.5	mA
					0.8 (V_i= 8 to 25V)			0.8 (V_i= 9 to 25V)			0.8 (V_i= 11.5 to 25V)			0.8 (V_i= 15 to 30V)	
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o= 5 mA		0.6			0.7			1			1.5		mV/°C
e_N	output noise voltage	B= 10Hz to 100KHz, T_j= 25°C			40			40			40			40	$\frac{\mu V}{V_o}$
SVR	Supply voltage rejection	f = 120 Hz	68 (V_i= 8 to 18V)			65 (V_i= 9 to 19V)			62 (V_i= 11.5 to 21.5V)			61 (V_i= 15 to 25V)			dB
V_d	Dropout voltage	I_o= 1A, T_j= 25°C		2	2.5		2	2.5		2	2.5		2	2.5	V
R_o	Output resistance	f = 1 KHz		17			19			16			18		mΩ
I_{sc}	Short circuit current	V_i= 35V, T_j= 25°C		0.75	1.2		0.75	1.2		0.75	1.2		0.75	1.2	A
I_{scp}	Short circ. peak current	T_j= 25°C	1.3	2.2	3.3	1.3	2.2	3.3	1.3	2.2	3.3	1.3	2.2	3.3	A

ELECTRICAL CHARACTERISTICS L 7800 (continued)

OUTPUT VOLTAGE			15			18			20			24			Unit
INPUT VOLTAGE (Unless otherwise specified)			23			26			28			33			
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output voltage	T_j= 25°C	14.4	15	15.6	17.3	18	18.7	19.2	20	20.8	23	24	25	V
		I_o= 5 mA to 1A $P_o \leq$ 15W	14.25 (V_i= 18.5 to 30V)	15	15.75	17.1 (V_i= 22 to 33V)	18	18.9	19 (V_i= 24 to 35V)	20	21	22.8 (V_i= 28 to 38V)	24	25.2	
ΔV_o	Line regulation	T_j = 25°C			150 (V_i= 17.5 to 30V)			180 (V_i= 21 to 33V)			200 (V_i= 22.5 to 35V)			240 (V_i= 27 to 38V)	mV
					75 (V_j= 20 to 26V)			90 (V_i= 24 to 30V)			100 (V_i= 26 to 32V)			120 (V_i= 30 to 36V)	
ΔV_o	Load regulation	T_j= 25°C I_o= 5 mA to 1.5A			150			180			200			240	mV
		T_j= 25°C I_o= 250 to 750 mA			75			90			100			120	
I_d	Quiescent current	T_j= 25°C			6			6			6			6	mA
ΔI_d	Quiescent current change	I_o= 5 mA to 1A			0.5			0.5			0.5			0.5	mA
					0.8 (V_i= 18.5 to 30V)			0.8 (V_i= 22 to 33V)			0.8 (V_i= 24 to 35V)			0.8 (V_i= 28 to 38V)	
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o= 5 mA		1.8			2.3			2.5			3		mV/°C
e_N	output noise voltage	B= 10Hz to 100KHz T_j= 25°C		40			40			40			40		$\frac{\mu V}{V_o}$
SVR	Supply voltage rejection	f = 120 Hz	60 (V_i=18.5 to 28.5V)			59 (V_i= 22 to 32V)			58 (V_i= 24 to 35V)			56 (V_i= 28 to 38V)			dB
V_d	Dropout voltage	I_o= 1A T_j= 25°C		2	2.5		2	2.5		2	2.5		2	2.5	V
R_o	Output resistance	f = 1 KHz		19			22			24			28		mΩ
I_{sc}	Short circuit current	V_i= 35V T_j= 25°C		0.75	1.2		0.75	1.2		0.75	1.2		0.75	1.2	A
I_{scp}	Short circ. peak current	T_j= 25°C	1.3	2.2	3.3	1.3	2.2	3.3	1.3	2.2	3.3	1.3	2.2	3.3	A

ELECTRICAL CHARACTERISTICS L 7800C (Refer to the test circuits, T_j = 0 to 125°C, I_o = 500 mA, C_i = 0.33 µF, C_o = 0.1 µF unless otherwise specified)

OUTPUT VOLTAGE			5			6			8			12			Unit
INPUT VOLTAGE (Unless otherwise specified)			10			11			14			19			
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output voltage	T_j = 25°C	4.8	5	5.2	5.75	6	6.25	7.7	8	8.3	11.5	12	12.5	V
		I_o = 5 mA to 1A, $P_o \leq$ 15W	4.75	5	5.25	5.7	6	6.3	7.6	8	8.4	11.4	12	12.6	V
			(V_i = 7 to 20V)			(V_i = 8 to 21V)			(V_i = 10.5 to 25V)			(V_i = 14.5 to 27V)			
ΔV_o	Line regulation	T_j = 25°C		3	100			120			160			240	mV
				(V_i = 7 to 25V)				(V_i = 8 to 25V)			(V_i = 10.5 to 25V)			(V_i = 14.5 to 30V)	
				1	50			60			80			120	mV
				(V_i = 8 to 12V)				(V_i = 9 to 13V)			(V_i = 11 to 17V)			(V_i = 16 to 22V)	
ΔV_o	Load regulation	T_j = 25°C, I_o = 5 mA to 1.5A			100			120			160			240	mV
		T_j = 25°C, I_o = 250 to 750 mA			50			60			80			120	mV
I_d	Quiescent current	T_j = 25°C			8			8			8			8	mA
ΔI_d	Quiescent current change	I_o = 5 mA to 1A			0.5			0.5			0.5			0.5	mA
					1.3			1.3			1			1	mA
			(V_i = 7 to 25V)			(V_i = 8 to 25V)			(V_i = 10.5 to 25V)			(V_i = 14.5 to 30V)			
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o = 5 mA		-1.1			-0.8			-0.8			-1		mV/°C
e_N	Output noise voltage	B= 10Hz to 100KHz, T_j = 25°C		40			45			52			75		µV
SVR	Supply voltage rejection	f = 120 Hz	62 (V_i = 8 to 18V)			59 (V_i = 9 to 19V)			56 (V_i = 11.5 to 21.5V)			55 (V_i = 15 to 25V)			dB
V_d	Dropout voltage	I_o = 1A		2			2			2			2		V
R_o	Output resistance	f = 1 KHz		17			19			16			18		mΩ
I_{sc}	Short circuit current	V_i = 35V, T_j = 25°C		750			550			450			350		mA
I_{scp}	Short circ. peak current	T_j = 25°C		2.2			2.2			2.2			2.2		A

ELECTRICAL CHARACTERISTICS L 7800C (continued)

OUTPUT VOLTAGE			15			18			20			24			Unit
INPUT VOLTAGE (Unless otherwise specified)			23			26			28			33			
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output voltage	T_j= 25°C	14.4	15	15.6	17.3	18	18.7	19.2	20	20.8	23	24	25	V
		I_o= 5 mA to 1A $P_o \leq$ 15W	14.25 (V_i= 17.5 to 30V)	15	15.75	17.1 (V_i= 21 to 33V)	18	18.9	19 (V_i= 23 to 35V)	20	21	22.8 (V_i= 27 to 38V)	24	25.2	
ΔV_o	Line regulation	T_j= 25°C			300 (V_i= 17.5 to 30V)			360 (V_i= 21 to 33V)			400 (V_i= 22.5 to 35V)			480 (V_i= 27 to 38V)	mV
					150 (V_i= 20 to 26V)			180 (V_i= 24 to 30V)			200 (V_i= 26 to 32V)			240 (V_i= 30 to 36V)	
ΔV_o	Load regulation	T_j= 25°C I_o= 5 mA to 1.5A			300			360			400			480	mV
		T_j= 25°C I_o= 250 to 750 mA			150			180			200			240	
I_d	Quiescent current	T_j= 25°C			8			8			8			8	mA
ΔI_d	Quiescent current change	I_o= 5 mA to 1A			0.5			0.5			0.5			0.5	mA
					1 (V_i= 17.5 to 30V)			1 (V_i= 21 to 33V)			1 (V_i= 23 to 35V)			1 (V_i= 27 to 38V)	
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o= 5 mA		-1			-1			-1			-1.5		mV/°C
e_N	Output noise voltage	B= 10Hz to 100KHz T_j= 25°C		90			110			150			170		μV
SVR	Supply voltage rejection	f = 120 Hz	54			53			52			50			dB
V_d	Dropout voltage	I_o= 1A		2			2			2			2		V
R_o	Output resistance	f = 1 KHz		19			22			24			28		mΩ
I_{sc}	Short circuit current	V_i= 35V T_j = 25°C		230			200			180			150		mA
I_{scp}	Short circ. peak current	T_j = 25°C		2.1			2.1			2.1			2.1		A

Fig. 4 - Dropout voltage vs. junction temperature

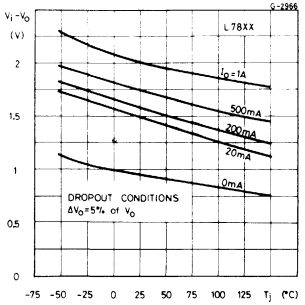


Fig. 5 - Peak output current vs. input/output differential voltage

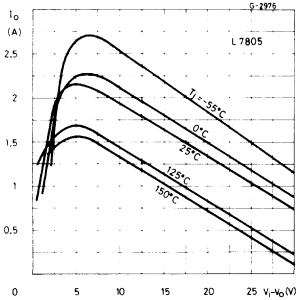


Fig. 6 - Supply voltage rejection vs. frequency

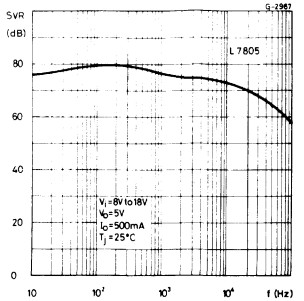


Fig. 7 - Output voltage vs. junction temperature

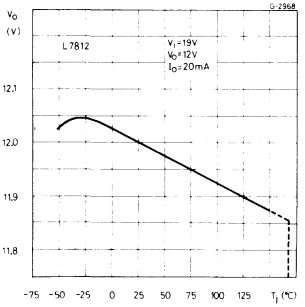


Fig. 8 - Output impedance vs. frequency

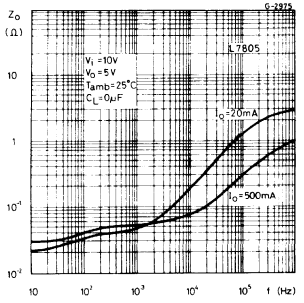


Fig. 9 - Quiescent current vs. junction temperature

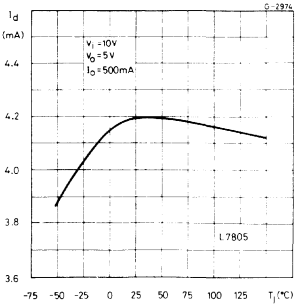


Fig. 10 - Load transient response

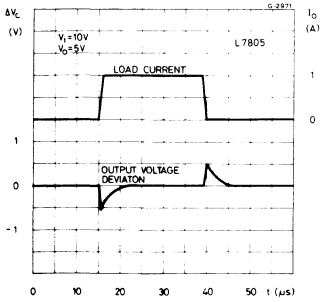


Fig. 11 - Line transient response

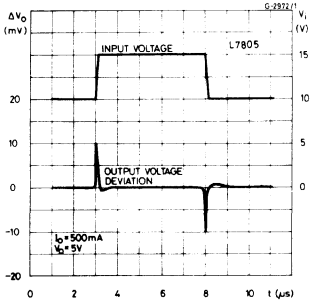
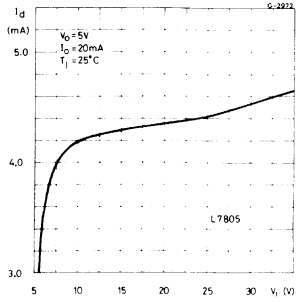
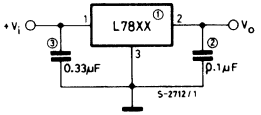


Fig. 12 - Quiescent current vs. input voltage



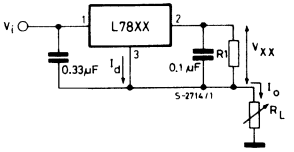
APPLICATION INFORMATION (continued)

Fig. 13 - Fixed output regulator



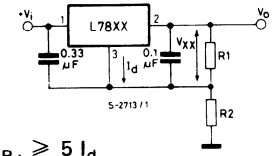
Notes:
(1) To specify an output voltage, substitute voltage value for "XX".
(2) Although no output capacitor is needed for stability, it does improve transient response.
(3) Required if regulator is located an appreciable distance from power supply filter.

Fig. 14 - Current regulator



$$I_o = \frac{V_{xx}}{R_1} + I_d$$

Fig. 15 - Circuit for increasing output voltage



$$I_{R_1} \geqslant 5\, I_d$$

$$V_o = V_{xx}\ (1 + \frac{R_2}{R_1}) + I_d\, R_2$$

Fig. 16 - Adjustable output regulator (7 to 30V)

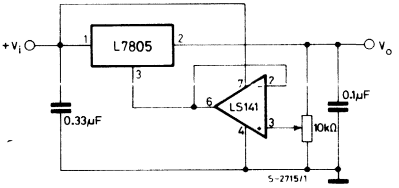
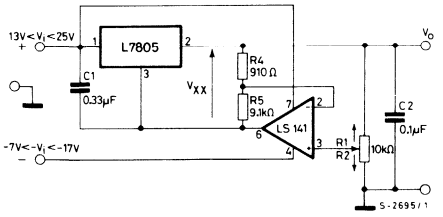
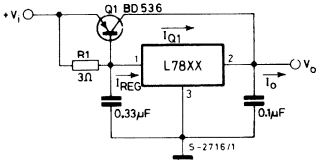


Fig. 17 - 0.5 to 10V regulator



$$V_o = V_{xx}\ \frac{R_4}{R_1}$$

Fig. 18 - High current voltage regulator

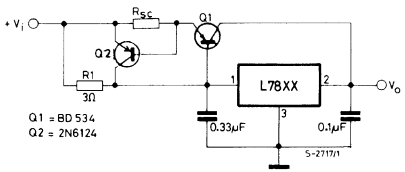


$$R_1 = \frac{V_{BEQ_1}}{I_{REG} - \frac{I_{Q_1}}{\beta_{Q_1}}}$$

$$I_o = I_{REG} + \beta_{Q_1}\ [I_{REG} - \frac{V_{BEQ_1}}{R_1}]$$

APPLICATION INFORMATION (continued)

Fig. 19 - High output current with short circuit protection



$$R_{SC} = \frac{V_{BEQ_2}}{I_{SC}}$$

Fig. 20 - Tracking voltage regulator

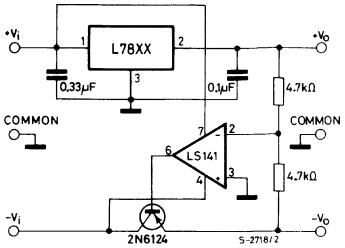
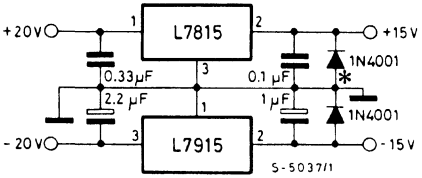


Fig. 21 - Split power supply (±15V - 1A)



* Against potential latch-up problems

Fig. 22 - Negative output voltage circuit

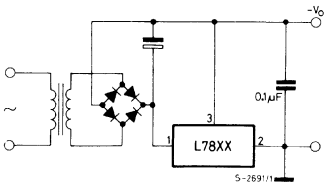


Fig. 23 - Switching regulator

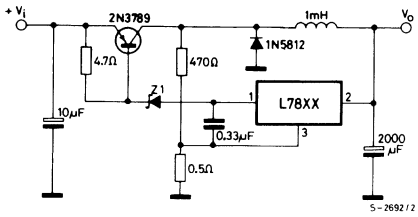
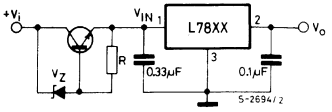


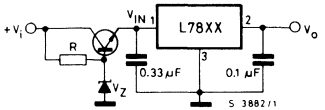
Fig. 24 - High input voltage circuit



$$V_{IN} = V_i - (V_Z + V_{BE})$$

APPLICATION INFORMATION (continued)

Fig. 25 - High input voltage circuit



$V_{IN} = V_Z - V_{BE}$

Fig. 26 - High output voltage regulator

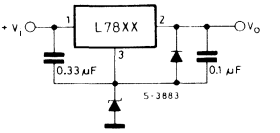
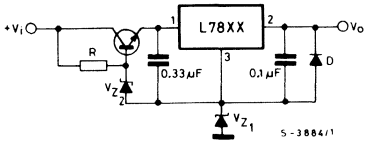
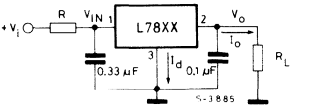


Fig. 27 - High input and output voltage



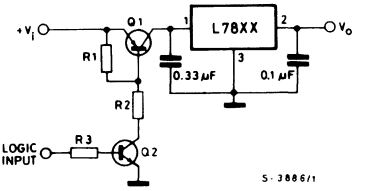
$V_O = V_{XX} + V_{Z1}$

Fig. 28 - Reducing power dissipation with dropping resistor



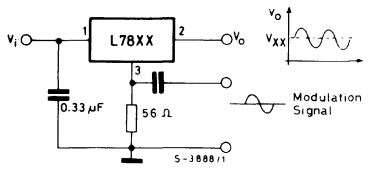
$$R = \frac{V_{i(min)} - V_{XX} - V_{DROP(max)}}{I_{o(max)} + I_{d(max)}}$$

Fig. 29 - Remote shuntdown



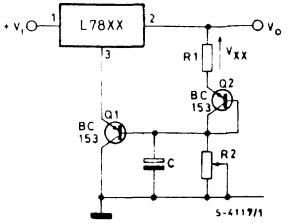
APPLICATION INFORMATION (continued)

Fig. 30 - Power AM modulator (unity voltage gain, $I_o \leq 1A$)



Note: The circuit performs well up to 100 KHz.

Fig. 31 - Adjustable output voltage with temperature compensation

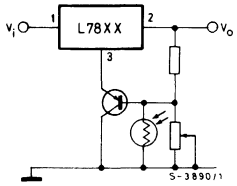


Note: Q_2 is connected as a diode in order to compensate the variation of the Q_1 V_{BE} with the temperature. C allows a slow rise-time of the V_o

$$V_o = V_{XX}\left(1 + \frac{R_2}{R_1}\right) + V_{BE}$$

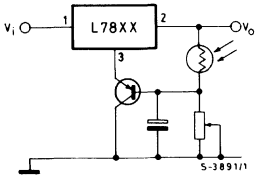
Fig. 32 - Light controllers ($V_{o\ min} = V_{XX} + V_{BE}$)

(a)



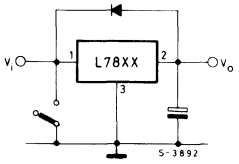
V_o falls when the light goes up

(b)



V_o rises when the light goes up

Fig. 33 - Protection against input short-circuit with high capacitance loads



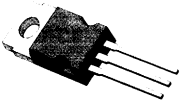
Applications with high capacitance loads and an output voltage greater than 6 volts need an external diode (see fig. 33) to protect the device against input short circuit. In this case the input voltage falls rapidly while the output voltage decreases showly. The capacitance discharges by means of the Base-Emitter junction of the series pass transistor in the regulator. If the energy is sufficiently high, the transistor may be destroyed. The external diode by-passes the current from the IC to ground.

L7800AB
L7800AC

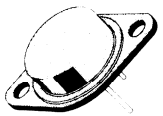
PRECISION 1A REGULATORS

- OUTPUT CURRENT IN EXCESS OF 1A
- OUTPUT VOLTAGES OF 5; 6; 8; 12; 15; 18; 24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR SOA PROTECTION
- 2% OUTPUT VOLTAGE TOLERANCE
- GUARANTEED IN EXTENDED TEMPERATURE RANGES

The L7800A series of three-terminal positive regulators is available in TO-220 and TO-3 packages and with several fixed output voltages, making it useful in a wide range of applications. These regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.



TO-220

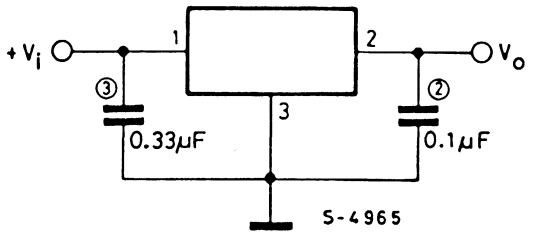


TO-3

ABSOLUTE MAXIMUM RATINGS

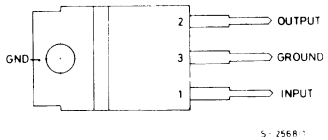
V_i	DC input voltage (for V_o = 5 to 18V)		35	V
	(for V_o = 24V)		40	V
I_o	Output current		internally limited	
P_{tot}	Power dissipation		internally limited	
T_j	Operating junction temperature	L7800 AC	0 to 125	°C
		L7800 AB	-40 to 125	°C
T_{stg}	Storage temperature		-65 to +150	°C

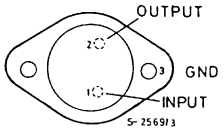
TYPICAL APPLICATION



L7800AB
L7800AC

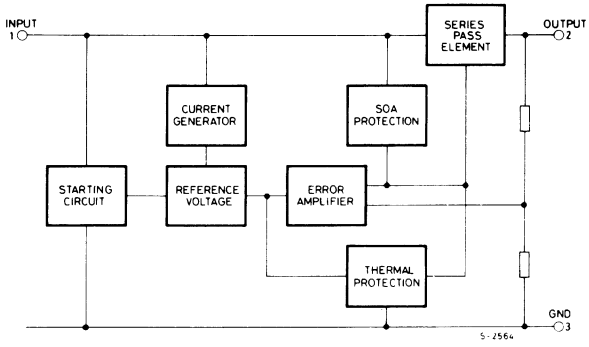
CONNECTION DIAGRAM AND ORDERING NUMBERS
(top view)



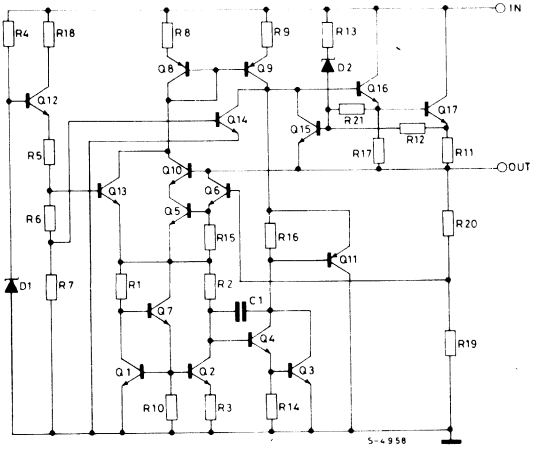


ORDERING NUMBERS			Output Voltage
T_j = -40 to 125°C	T_j = 0 to 125°C		
TO-220	TO-220	TO-3	
L7805ABV	L7805ACV	L7805ACT	5V
L7806ABV	L7806ACV	L7806ACT	6V
L7808ABV	L7808ACV	L7808ACT	8V
L7812ABV	L7812ACV	L7812ACT	12V
L7815ABV	L7815ACV	L7815ACT	15V
L7818ABV	L7818ACV	L7818ACT	18V
L7824ABV	L7824ACV	L7824ACT	24V

BLOCK DIAGRAM



SCHEMATIC DIAGRAM



TEST CIRCUITS

Fig. 1 - DC parameters

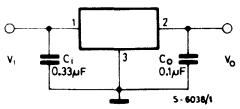


Fig. 2 - Load regulation

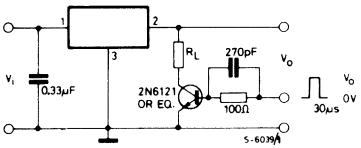
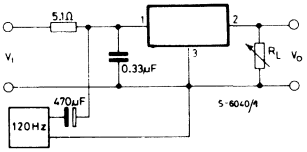


Fig. 3 - Ripple rejection



THERMAL DATA

			TO-220	TO-3
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3°C/W	4°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50°C/W	35°C/W

ELECTRICAL CHARACTERISTICS L7805A (V_i = 10V, I_o = 1A, T_j = 0 to 125°C (L7805AC), T_j = -40 to 125°C (L7805AB) unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_o	Output voltage	T_j = 25°C	4.9	5	5.1	V
V_o	Output voltage	I_o = 5mA to 1A, Po ⩽ 15W V_i = 7.5 to 20V	4.8	5	5.2	V
ΔV_o*	Line regulation	V_i = 7.5 to 25V, I_o = 500 mA V_i = 8 to 12V		7 10	50 50	mV mV
		V_i = 8 to 12V, T_j = 25°C V_i = 7.3 to 20V, T_j = 25°C		2 7	25 50	mV mV
ΔV_o*	Load regulation	I_o = 5mA to 1A I_o = 5mA to 1.5A, T_j = 25°C I_o = 250 to 750 mA		25 25 8	100 100 50	mV mV mV
I_d	Quiescent current	T_j = 25°C		4.3	6 6	mA mA
ΔI_d	Quiescent current change	V_i = 8 to 25V, I_o = 500mA V_i = 7.5 to 20V, T_j = 25°C I_o = 5mA to 1A			0.8 0.8 0.5	mA mA mA
SVR	Supply voltage rejection	V_i = 8 to 18V, f = 120Hz I_o = 500mA		68		dB
V_d	Dropout voltage	I_o = 1A T_j = 25°C		2		V
e_N	Output noise voltage	f = 10Hz to 100KHz, T_j = 25°C		10		$\mu V/V_o$
R_o	Output resistance	f = 1KHz		17		mΩ
I_{sc}	Short circuit current	T_{amb} = 25°C V_i = 35V		0.2		A
I_{scp}	Short circuit peak current	T_j = 25°C		2.2		A
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift			− 1.1		mV/°C

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS L7806A (V_i = 11V, I_o = 1A, T_j = 0 to 125°C (L7806AC), T_j = -40 to 125°C (L7806AB); unless otherwise specified

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_o	Output voltage	T_j = 25°C	5.88	6	6.12	V
V_o	Output voltage	I_o = 5mA to 1A, $P_o \leq$ 15W V_i = 8.6 to 21V	5.76	6	6.24	V
ΔV_o*	Line regulation	V_i = 8.6 to 25V, I_o = 500mA V_i = 9 to 13V		9 11	60 60	mV mV
		V_i = 9 to 13V, T_j = 25°C V_i = 8.3 to 21V, T_j = 25°C		3 9	30 60	mV mV
ΔV_o*	Load regulation	I_o = 5mA to 1A I_o = 5mA to 1.5A, Tj= 25°C I_o = 250 to 750 mA		43 43 16	100 100 50	mV mV mV
I_d	Quiescent current	T_j = 25°C		4.3	6 6	mA mA
ΔI_d	Quiescent current change	V_i = 9 to 25V, I_o = 500mA V_i = 8.6 to 21V, T_j = 25°C I_o = 5mA to 1A			0.8 0.8 0.5	mA mA mA
SVR	Supply voltage rejection	V_i = 9 to 19V, f = 120Hz I_o = 500mA		65		dB
V_d	Dropout voltage	I_o = 1A, T_j = 25°C		2		V
e_N	Output noise voltage	T_j = 25°C, f = 10Hz to 100KHz		10		$\mu V/V_o$
R_o	Output resistance	f = 1KHz		17		mΩ
I_{sc}	Short circuit current	T_{amb} = 25°C V_i = 35V		0.2		A
I_{scp}	Short circuit peak current	T_j = 25°C		2.2		A
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift			− 0.8		mV/°C

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS L7808A (V_I = 14V, I_O = 1A, T_j = 0 to 125°C (L7808AC), T_j = -40 to 125°C (L7808AB), unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_O	Output voltage	T_j = 25°C	7.84	8	8.16	V
V_O	Output voltage	I_O = 5mA to 1A, $P_O \leqslant$ 15W V_i = 10.6 to 23V	7.7	8	8.3	V
ΔV_O*	Line regulation	V_i = 10.6 to 25V, I_O = 500mA V_i = 11 to 17V		12 15	80 80	mV mV
		V_i = 11 to 17V, T_j = 25°C V_i = 10.4 to 23V, T_j = 25°C		5 12	40 80	mV mV
ΔV_O*	Load regulation	I_O = 5mA to 1 A I_O = 5mA to 1.5 A, T_j = 25°C I_O = 250 to 750 mA		45 45 16	100 100 50	mV mV mV
I_d	Quiescent current	T_j = 25°C		4.3	6 6	mA mA
ΔI_d	Quiescent current change	V_i = 11 to 25V, I_O = 500mA V_i = 10.6 to 23V, T_j = 25°C I_O = 5mA to 1A			0.8 0.8 0.5	mA mA mA
SVR	Supply voltage rejection	V_i = 11.5 to 21.5V, f = 120Hz I_O = 500mA		62		dB
V_d	Dropout voltage	I_O = 1A, T_j = 25°C		2		V
e_N	Output noise voltage	T_j = 25°C, f = 10Hz to 100KHz		10		$\mu V/V_O$
R_O	Output resistance	f = 1KHz		18		mΩ
I_{sc}	Short circuit current	T_{amb} = 25°C V_i = 35V		0.2		A
I_{scp}	Short circuit peak current	T_j = 25°C		2.2		A
$\frac{\Delta V_O}{\Delta T}$	Output voltage drift			− 0.8		mV/°C

* Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS L7812A (V_I = 19V, I_o = 1A, T_j = 0 to 125°C (L7812AC), T_j = -40 to 125°C (L7812AB), unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_o	Output voltage	T_j = 25°C	11.75	12	12.25	V
V_o	Output voltage	I_o = 5mA to 1A, $P_o \leqslant$ 15W V_i = 14.8 to 27V	11.5	12	12.5	V
ΔV_o*	Line regulation	V_i = 14.8 to 30V, I_o = 500mA V_i = 16 to 22V		13 16	120 120	mV mV
		V_i = 16 to 22V, T_j = 25°C V_i = 14.5 to 27V, T_j = 25°C		6 13	60 120	mV mV
ΔV_o*	Load regulation	I_o = 5mA to 1A I_o = 5mA to 1.5 A, T_j = 25°C I_o = 250 to 750 mA		46 46 17	100 100 50	mV mV mV
I_d	Quiescent current	T_j = 25°C		4.4	6 6	mA mA
ΔI_d	Quiescent current change	V_i = 15 to 30V, I_o = 500mA V_i = 14.8 to 27V, T_j = 25°C I_o = 5mA to 1A			0.8 0.8 0.5	mA mA mA
SVR	Supply voltage rejection	V_i = 15 to 25V, f = 120Hz I_o = 500mA		60		dB
V_d	Dropout voltage	I_o = 1A, T_j = 25°C		2		V
e_N	Output noise voltage	T_j = 25°C, f = 10Hz to 100KHz		10		$\mu V/V_o$
R_o	Output resistance	f = 1KHz		18		mΩ
I_{sc}	Short circuit current	T_{amb} = 25°C V_i = 35V		0.2		A
I_{scp}	Short circuit peak current	T_j = 25°C		2.2		A
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift			-1		mV/°C

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS L7815A (V_i = 23V, I_o = 1A, T_j = 0 to 125°C (L7815AC), T_j = -40 to 125°C (L7815AB), unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_o	Output voltage	T_j = 25°C	14.7	15	15.3	V
V_o	Output voltage	I_o = 5mA to 1A, $P_o \leqslant$ 15W V_i = 17.9 to 30V	14.4	15	15.6	V
ΔV_o*	Line regulation	V_i = 17.9 to 30V, I_o = 500mA V_i = 20 to 26V		13 16	150 150	mV mV
		V_i = 20 to 26V, T_j = 25°C V_i = 17.5 to 30V, T_j = 25°C		6 13	75 150	mV mV
ΔV_o*	Load regulation	I_o = 5mA to 1A I_o = 5mA to 1.5 A, T_j = 25°C I_o = 250 to 750 mA		52 52 20	100 100 50	mV mV mV
I_d	Quiescent current	T_j = 25°C		4.4	6 6	mA mA
ΔI_d	Quiescent current change	V_i = 17.5 to 30V, I_o = 500mA V_i = 17.5 to 30V, T_j = 25°C I_o = 5mA to 1A			0.8 0.8 0.5	mA mA mA
SVR	Supply voltage rejection	V_i = 18.5 to 28.5V, f = 120Hz I_o = 500mA		58		dB
V_d	Dropout voltage	I_o = 1A, T_j = 25°C		2		V
e_N	Output noise voltage	T_j = 25°C, f = 10Hz to 100KHz		10		$\mu V/V_o$
R_o	Output resistance	f = 1KHz		19		mΩ
I_{sc}	Short circuit current	T_{amb} = 25°C V_i = 35V		0.2		A
I_{scp}	Short circuit peak current	T_j = 25°C		2.2		A
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift			− 1		mV/°C

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS L7818A (V_I = 27V, I_o = 1A, T_j = 0 to 125°C (L7818AC), T_j = -40 to 125°C (L7818AB), unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_o	Output voltage	T_j = 25°C	17.64	18	18.36	V
V_o	Output voltage	I_o = 5mA to 1A, $P_o \leqslant$ 15W V_i = 21 to 33V	17.3	18	18.7	V
ΔV_o*	Line regulation	V_i = 21 to 33V, I_o = 500mA V_i = 24 to 30V		25 28	180 180	mV mV
		V_i = 24 to 30V, T_j = 25°C V_i = 20.6 to 33V, T_j = 25°C		10 25	90 180	mV mV
ΔV_o*	Load regulation	I_o = 5mA to 1A I_o = 5mA to 1.5 A, T_j = 25°C I_o = 250 to 750 mA		55 55 22	100 100 50	mV mV mV
I_d	Quiescent current	T_j = 25°C		4.5	6 6	mA mA
ΔI_d	Quiescent current change	V_i = 21 to 33V, I_o = 500mA V_i = 21 to 33V, T_j = 25°C I_o = 5mA to 1A			0.8 0.8 0.5	mA mA mA
SVR	Supply voltage rejection	V_i = 22 to 32V, f = 120Hz I_o = 500mA		57		dB
V_d	Dropout voltage	I_o = 1A, T_j = 25°C		2		V
e_N	Output noise voltage	T_j = 25°C, f = 10Hz to 100KHz		10		$\mu V/V_o$
R_o	Output resistance	f = 1KHz		19		mΩ
I_{sc}	Short circuit current	T_{amb} = 25°C V_i = 35V		0.2		A
I_{scp}	Short circuit peak current	T_j = 25°C		2.2		A
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift			− 1		mV/°C

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS L7824A (V_i = 33V, I_o = 1A, T_j = 0 to 125°C (L7824AC), T_j = -40 to 125°C (L7824AB), unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_o	Output voltage	T_j = 25°C	23.5	24	24.5	V
V_o	Output voltage	I_o = 5mA to 1A, $P_o \leqslant$ 15W V_i = 27.3 to 38V	23	24	25	V
ΔV_o*	Line regulation	V_i = 27 to 38V, I_o = 500mA V_i = 30 to 36V V_i = 30 to 36V, T_j = 25°C V_i = 26.7 to 38V, T_j = 25°C		31 35 14 31	240 240 120 240	mV mV mV mV
ΔV_o*	Load regulation	I_o = 5mA to 1 A I_o = 5mA to 1.5 A, T_j = 25°C I_o = 250 to 750 mA		60 60 25	100 100 50	mV mV mV
I_d	Quiescent current	T_j = 25°C		4.6	6 6	mA mA
ΔI_d	Quiescent current change	V_i = 27.3 to 38V, I_o = 500mA V_i = 27.3 to 38V, T_j = 25°C I_o = 5mA to 1A			0.8 0.8 0.5	mA mA mA
SVR	Supply voltage rejection	V_i = 28 to 38V, f = 120Hz I_o = 500mA		54		dB
V_d	Dropout voltage	I_o = 1A, T_j = 25°C		2		V
e_N	Output noise voltage	T_j = 25°C, f = 10Hz to 100KHz		10		$\mu V/V_o$
R_o	Output resistance	f = 1KHz		20		mΩ
I_{sc}	Short circuit current	T_{amb} = 25°C V_i = 35V		0.2		A
I_{scp}	Short circuit peak current	T_j = 25°C		2.2		A
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift			− 1.5		mV/°C

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

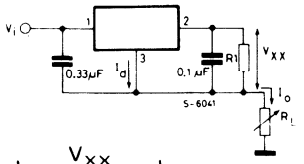
APPLICATIONS INFORMATION

Design Considerations

The L7800A Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

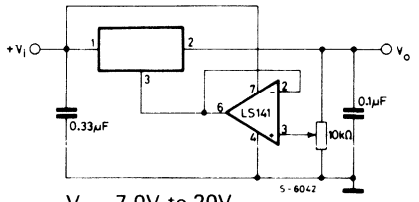
In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

Fig. 4 - Current regulator



$$I_o = \frac{V_{XX}}{R_1} + I_d$$

Fig. 5 - Adjustable output regulator

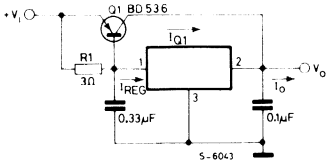


V_O, 7.0V to 20V

$V_i - V_O \geqslant 2.0V$

The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0V greater than the regulator voltage.

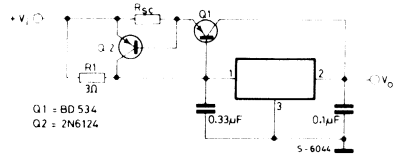
Fig. 6 - Current boost regulator



$$R_1 = \frac{V_{BEQ_1}}{I_{REG} - \frac{I_{Q_1}}{\beta_{Q_1}}}$$

$$I_o = I_{REG} + \beta_{Q_1}\left[I_{REG} - \frac{V_{BEQ_1}}{R_1}\right]$$

Fig. 7 - Short-circuit protection



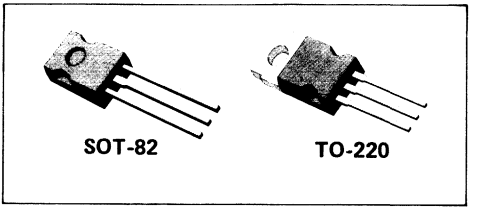
The circuit of Figure 6 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, a four-ampere plastic power transistor is specified.

L78M00 Series

POSITIVE VOLTAGE REGULATORS

- OUTPUT CURRENT TO 0.5A
- OUTPUT VOLTAGES OF 5; 6; 8; 12; 15; 18; 20; 24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR SOA PROTECTION

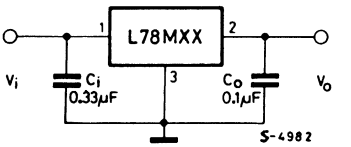
The L78M00 series of three-terminal positive regulators is available in TO-220 and SOT-82 packages and with several fixed output voltages, making it useful in a wide range of applications. These regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 0.5A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.



ABSOLUTE MAXIMUM RATINGS

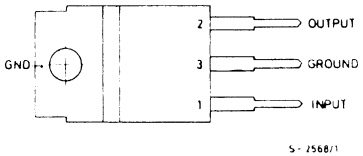
V_i	DC input voltage (for V_o = 5 to 18V)	35	V
	(for V_o = 20, 24V)	40	V
I_o	Output current	Internally limited	
P_{tot}	Power dissipation	Internally limited	
T_{stg}	Storage temperature	-65 to +150	°C
T_{op}	Operating junction temperature	0 to +150	°C

APPLICATION CIRCUIT

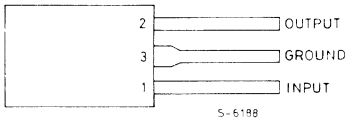


CONNECTION DIAGRAM AND ORDERING NUMBERS

(top view)



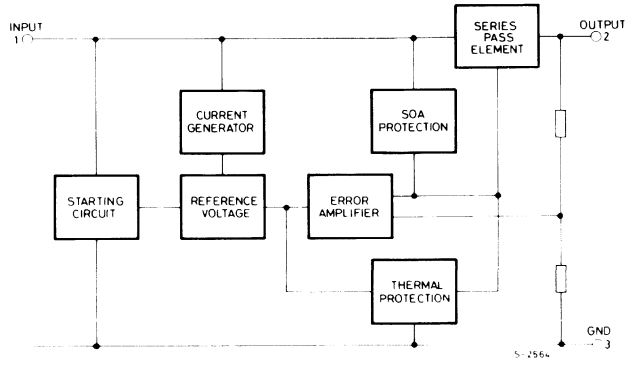
TO-220



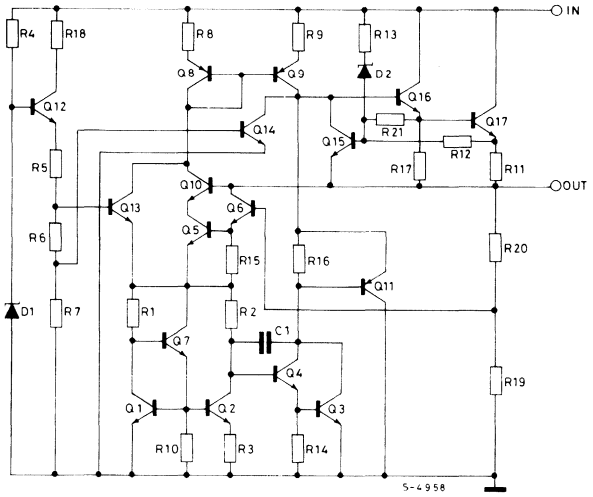
SOT-82

Ordering Numbers		Output Voltage
TO-220	SOT-82	
L78M05CV	L78M05CX	5V
L78M06CV	L78M06CX	6V
L78M08CV	L78M08CX	8V
L78M12CV	L78M12CX	12V
L78M15CV	L78M15CX	15V
L78M18CV	L78M18CX	18V
L78M20CV	L78M20CX	20V
L78M24CV	L78M24CX	24V

BLOCK DIAGRAM



SCHEMATIC DIAGRAM



TEST CIRCUITS

Fig. 1 - DC parameters

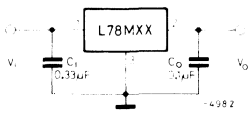


Fig. 2 - Load regulation

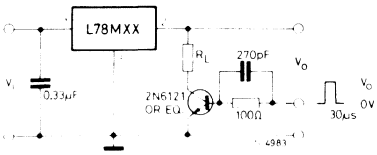
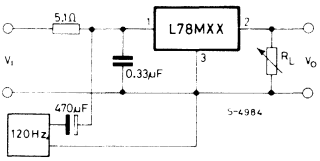


Fig. 3 - Ripple rejection



THERMAL DATA

			SOT-82	TO-220
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	8 °C/W	3 °C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100 °C/W	50 °C/W

ELECTRICAL CHARACTERISTICS L78M00C (Refer to the test circuits, T_j = 25°C, I_o = 350 mA unless otherwise specified, C_i = 0.33 μF, C_o = 0.1 μF)

OUTPUT VOLTAGE			5			6			8			12			Unit
INPUT VOLTAGE (Unless otherwise specified)			10			11			14			19			
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output voltage		4.8	5	5.2	5.75	6	6.25	7.7	8	8.3	11.5	12	12.5	V
		I_o = 5 to 350 mA	4.75	5	5.25 (V_i = 7 to 20V)	5.7	6	6.3 (V_i = 8 to 21V)	7.6	8	8.4 (V_i = 10.5 to 23V)	11.4	12	12.6 (V_i = 14.5 to 27V)	
ΔV_o	Line regulation	I_o = 200 mA			100 (V_i = 7 to 25V)			100 (V_i = 8 to 25V)			100 (V_i = 10.5 to 25V)			100 (V_i = 14.5 to 30V)	mV
					50 (V_i = 8 to 25V)			50 (V_i = 9 to 25V)			50 (V_i = 11 to 25V)			50 (V_i = 16 to 30V)	
ΔV_o	Load regulation	I_o = 5 mA to 0.5A			100			120			160			240	mV
		I_o = 5 mA to 200 mA			50			60			80			120	
I_d	Quiescent current				6			6			6			6	mA
ΔI_d	Quiescent current change	I_o = 5 mA to 350 mA			0.5			0.5			0.5			0.5	
		I_o = 200 mA			0.8 (V_i = 8 to 25V)			0.8 (V_i = 9 to 25V)			0.8 (V_i = 10.5 to 25)			0.8 (V_i = 14.5 to 30V)	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage drift	I_o = 5 mA T_j = 0 to 125°C		-0.5			-0.5			-0.5			-1.0		mV/°C
e_N	Output noise voltage	B= 10Hz to 100KHz		40			45			52			75		μV
SVR	Supply voltage rejection	f = 120 Hz I_o = 300 mA	62 (V_i = 8 to 18V)			59 (V_i = 9 to 19V)			56 (V_i =11.5 to 21.5V)			55 (V_i = 15 to 25V)			dB
V_d	Dropout voltage			2			2			2			2		V
I_{sc}	Short circuit current	V_i = 35V		300			270			250			240		mA
I_{scp}	Short circ. peak current			700			700			700			700		mA

ELECTRICAL CHARACTERISTICS L78M00C (continued)

OUTPUT VOLTAGE			15			18			20			24			Unit
INPUT VOLTAGE (Unless otherwise specified)			23			26			29			33			
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_O	Output Voltage		14.4	15	15.6	17.3	18	18.7	19.2	20	20.8	23	24	25	V
		I_O = 5 to 350 mA	14.25	15	15.75 (V_i = 17.5 to 30V)	17.1	18	18.9 (V_i = 20.5 to 33V)	19	20	21 (V_i = 23 to 35V)	22.8	24	25.2 (V_i = 27 to 38V)	
ΔV_O	Line regulation	I_O = 200 mA			100 (V_i = 17.5 to 30V)			100 (V_i = 21 to 33V)			100 (V_i = 23 to 35V)			100 (V_i = 27 to 38V)	mV
					50 (V_i = 20 to 30V)			50 (V_i = 24 to 33V)			50 (V_i = 24 to 35V)			50 (V_i = 28 to 38V)	
ΔV_O	Load regulation	I_O = 5 mA to 0.5A			300			360			400			480	mV
		I_O = 5 mA to 200 mA			150			180			200			240	
I_d	Quiescent current				6			6			6			6	mA
ΔI_d	Quiescent current change	i_O = 5 mA to 350 mA			0.5			0.5			0.5			0.5	mA
		I_O = 200 mA			0.8 (V_i = 17.5 to 30V)			0.8 (V_i = 21 to 33V)			0.8 (V_i = 23 to 35V)			0.8 (V_i = 27 to 38V)	
$\frac{\Delta V_O}{\Delta T}$	Output voltage drift	I_O = 5 mA T_{amb} = 0 to 125 C		-1			-1.1			-1.1			-1.2		mV/ C
e_N	Output noise voltage	B = 10Hz to 100KHz		90			100			110			170		μV
SVR	Supply voltage rejection	f = 120 Hz I_O = 300 mA	54 (V_i = 18.5 to 28.5V)			53 (V_i = 22 to 32V)			53 (V_i = 24 to 34V)			50 (V_i = 28 to 38V)			dB
V_d	Dropout Voltage			2			2			2			2		V
I_{sc}	Short circuit current	V_i = 35V		240			240			240			240		mA
I_{scp}	Short circ. peak current			700			700			700			700		mA

Fig. 4 - Dropout voltage vs. junction temperature

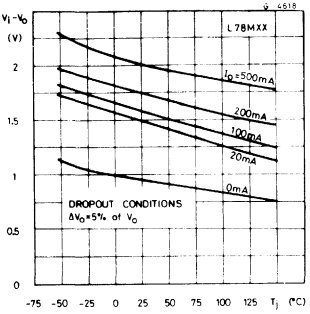


Fig. 5 - Dropout characteristics

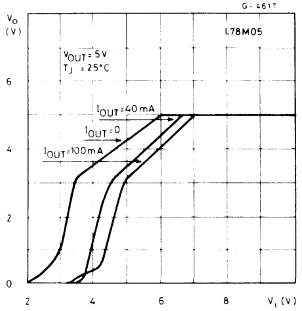


Fig. 6 - Peak output current vs. input-output differential voltage

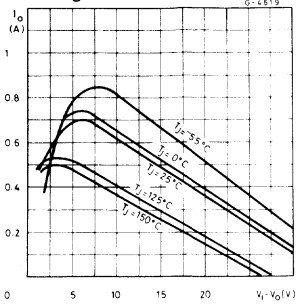


Fig. 7 - Output voltage vs. junction temperature

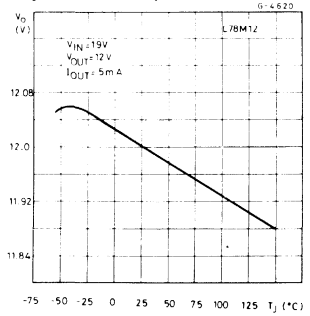


Fig. 8 - Supply voltage rejection vs. frequency

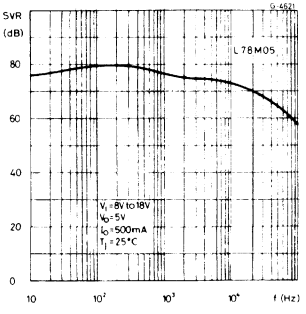


Fig. 9 - Quiescent current vs. junction temperature

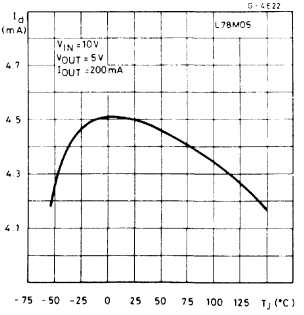


Fig. 10 - Load transient response

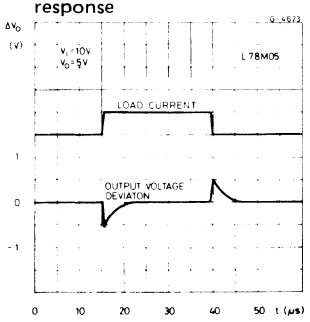


Fig. 11 - Line transient response

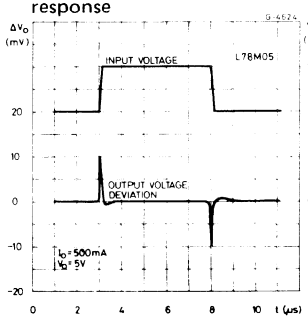
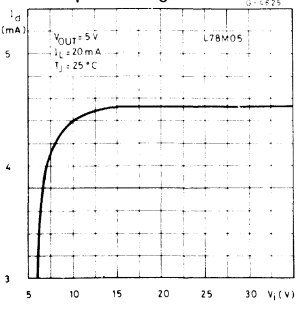
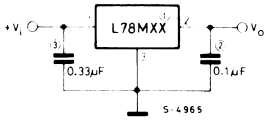


Fig. 12 - Quiescent current vs. input voltage



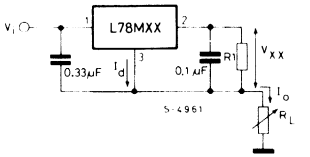
APPLICATION INFORMATION (continued)

Fig. 13 - Fixed output regulator



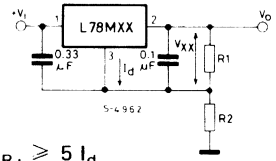
Notes:
(1) To specify an output voltage, substitute voltage value for "XX".
(2) Although no output capacitor is needed for stability, it does improve transient response.
(3) Required if regulator is located an appreciable distance from power supply filter.

Fig. 14 - Costant current regulator



$$I_o = \frac{V_{xx}}{R_1} + I_d$$

Fig. 15 - Circuit for increasing output voltage



$$I_{R_1} \geqslant 5\, I_d$$

$$V_o = V_{xx}\ (1 + \frac{R_2}{R_1}) + I_d\, R_2$$

Fig. 16 - Adjustable output regulator (7 to 30V)

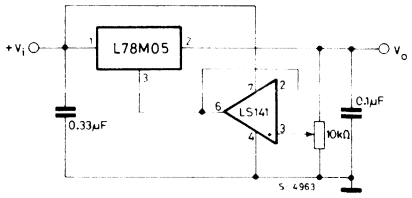
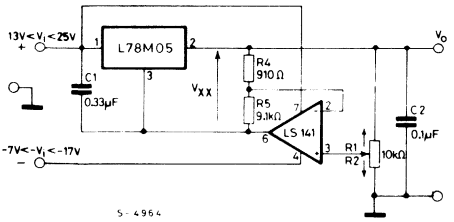
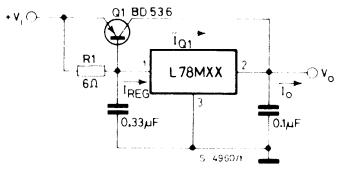


Fig. 17 - 0.5 to 10V regulator



$$V_o = V_{xx}\ \frac{R_4}{R_1}$$

Fig. 18 High current voltage regulator

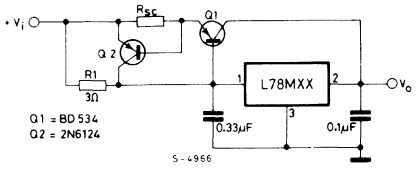


$$R_1 = \frac{V_{BEQ_1}}{I_{REG} - \frac{I_{Q_1}}{\beta_{Q_1}}}$$

$$I_o = I_{REG} + \beta_{Q_1}\ [I_{REG} - \frac{V_{BEQ_1}}{R_1}]$$

APPLICATION INFORMATION (continued)

Fig. 19 - High output current with short circuit protection



$$R_{SC} = \frac{V_{BEQ_2}}{I_{SC}}$$

Fig. 20 - Tracking voltage regulator

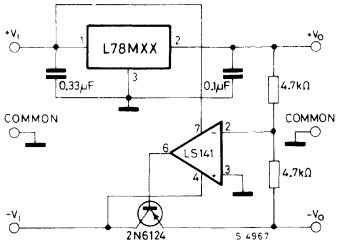
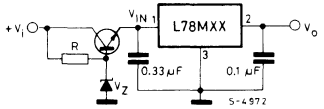
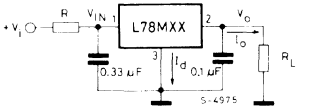


Fig. 21 - High input voltage circuit



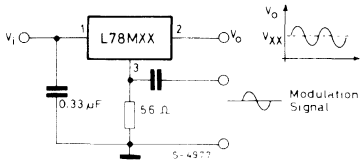
$$V_{IN} = V_Z - V_{BE}$$

Fig. 22 - Reducing power dissipation with dropping resistor



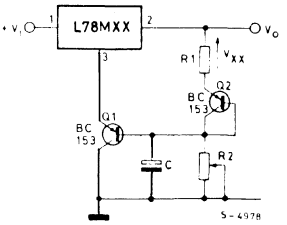
$$R = \frac{V_{i(min)} - V_{XX} - V_{DROP(max)}}{I_{o(max)} + I_{d(max)}}$$

Fig. 23 - Power AM modulator (unity voltage gain, $I_o \leqslant 0.5$)



Note: The circuit performs well up to 100 KHz.

Fig. 24 - Adjustable output voltage with temperature compensation



Note: Q_2 is connected as a diode in order to compensate the variation of the Q_1 V_{BE} with the temperature. C allows a slow rise-time of the V_o

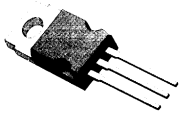
$$V_o = V_{XX}\left(1 + \frac{R_2}{R_1}\right) + V_{BE}$$

L78M00AB

PRECISION 500mA REGULATORS

- OUTPUT CURRENT UP TO 0.5A
- OUTPUT VOLTAGES OF 5; 6; 8; 12; 15; 18; 20; 24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTORS SOA PROTECTION
- ± 2% OUTPUT VOLTAGE TOLERANCE
- GUARANTEED IN EXTENDED TEMPERATURE RANGES

The L78M00AB series of three-therminal positive regulators is available in TO-220 package and with several fixed output voltages, making it useful in a wide range of applications. These regulators can provide local on-card regulation eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 0.5A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

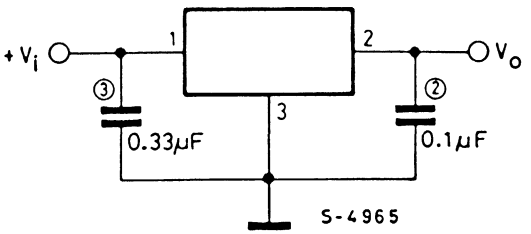


TO-220

ABSOLUTE MAXIMUM RATINGS

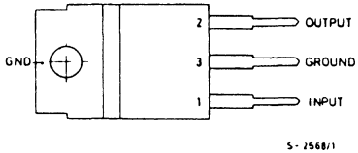
V_i	DC input voltage (for V_o = 5 to 18V)	35	V
	(for V_o = 20, 24V)	40	V
I_o	Output current	Internally limited	
P_{tot}	Power dissipation	Internally limited	
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Operating junction temperature	-40 to 125	°C

TYPICAL APPLICATION



L78M00AB

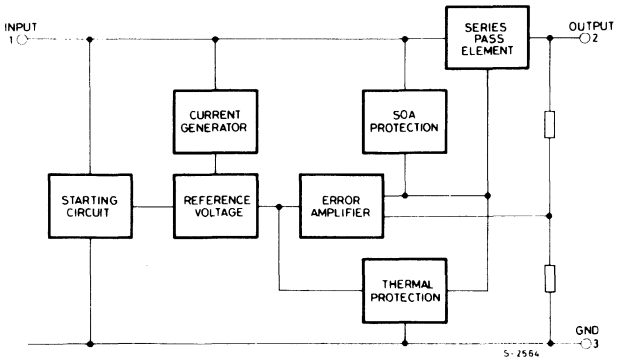
CONNECTION DIAGRAM AND ORDERING NUMBERS
(top view)



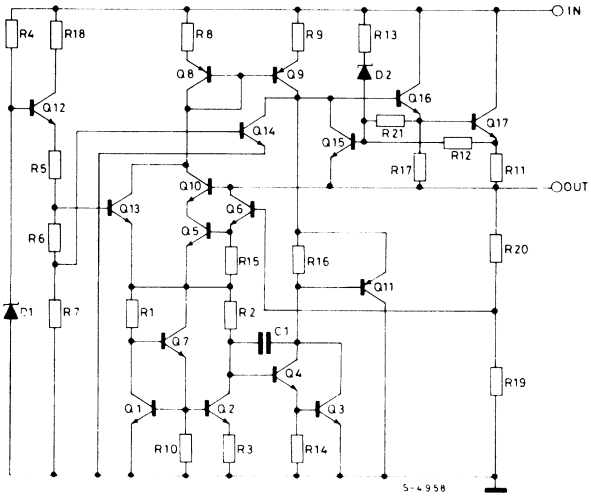
TO-220

ORDERING NUMBERS	Output Voltage
L78M05ABV	5V
L78M06ABV	6V
L78M08ABV	8V
L78M12ABV	12V
L78M15ABV	15V
L78M18ABV	18V
L78M20ABV	20V
L78M24ABV	24V

BLOCK DIAGRAM



SCHEMATIC DIAGRAM



TEST CIRCUITS

Fig. 1 - DC parameters

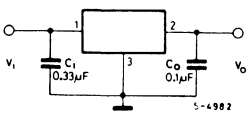


Fig. 2 - Load regulation

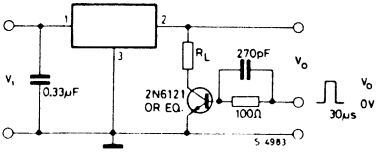
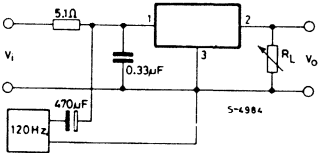


Fig. 3 - Ripple rejection



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3 °C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50 °C/W

ELECTRICAL CHARACTERISTICS L78M00AB (Refer to the test circuits, T_j = -40 to 125°C, I_o = 350mA unless otherwise specified, C_i = 0.33μF, C_o = 0.1μF)

OUTPUT VOLTAGE			5			6			8			12			Unit
INPUT VOLTAGE (Unless otherwise specified)			10			11			14			19			
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output voltage	T_j = 25eC	4.9	5	5.1	5.88	6	6.12	7.84	8	8.16	11.75	12	12.25	V
		I_o= 5 to 350 mA	4.8	5	5.2 (V_i= 7 to 20V)	5.75	6	6.3 (V_i= 8 to 21V)	7.7	8	8.3 (V_i= 10.5 to 23V)	11.5	12	12.5 (V_i= 14.5 to 27V)	
ΔV_o	Line regulation	I_o= 200 mA T_j = 25°C			100 (V_i= 7 to 25V)			100 (V_i= 8 to 25V)			100 (V_i= 10.5 to 25V)			100 (V_i= 14.5 to 30V)	mV
					30 (V_i= 8 to 25V)			30 (V_i= 9 to 25V)			30 (V_i= 11 to 25V)			30 (V_i= 16 to 30V)	
ΔV_o	Load regulation	I_o= 5 mA to 0.5A T_j = 25°C I_o= 5 mA to 200 mA			100			120			160			240	mV
					50			60			80			120	
I_d	Quiescent current	T_j = 25°C			6			6			6			6	mA
ΔI_d	Quiescent current change	I_o= 5 mA to 350 mA			0.5			0.5			0.5			0.5	mA
		I_o= 200 mA			0.8 (V_i= 8 to 25V)			0.8 (V_i= 9 to 25V)			0.8 (V_i= 10.5 to 25)			0.8 (V_i= 14.5 to 30V)	
$\frac{\Delta V_o}{\Delta T}$	Output Voltage drift	I_o= 5 mA		-0.5			-0.5			-0.5			-1.0		mV/°C
e_N	Output noise voltage	B= 10Hz to 100KHz T_j = 25°C		40			45			52			75		μV
SVR	Supply voltage rejection	f = 120 Hz I_o= 300 mA T_j = 25°C	62 (V_i= 8 to 18V)			59 (V_i= 9 to 19V)			56 (V_i=11.5 to 21.5V)			55 (V_i= 15 to 25V)			dB
V_d	Dropout voltage	T_j = 25°C		2			2			2			2		V
I_{sc}	Short circuit current	V_i= 35V T_j = 25°C		300			270			250			240		mA
I_{scp}	Short circ. peak current	T_j = 25°C		700			700			700			700		mA

ELECTRICAL CHARACTERISTICS L78M00AB (continued)

OUTPUT VOLTAGE			15			18			20			24			Unit
INPUT VOLTAGE (Unless otherwise specified)			23			26			29			33			
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output Voltage	T_j = 25°C	14.7	15	15.3	17.64	18	18.36	19.6	20	20.4	23.5	24	24.5	V
		I_o = 5 to 350 mA	14.4 (V_i = 17.5 to 30V)	15	15.6	17.3 (V_i = 20.5 to 33V)	18	18.7	19.2 (V_i = 23 to 35V)	20	20.8	23 (V_i = 27 to 38V)	24	25	
ΔV_o	Line regulation	I_o = 200 mA T_j = 25°C			100 (V_i = 17.5 to 30V)			100 (V_i = 21 to 33V)			100 (V_i = 23 to 35V)			100 (V_i = 27 to 38V)	mV
					30 (V_i = 20 to 30V)			30 (V_i = 24 to 33V)			30 (V_i = 24 to 35V)			30 (V_i = 28 to 38V)	
ΔV_o	Load regulation	I_o = 5 mA to 0.5A T_j = 25°C			300			360			400			480	mV
		I_o = 5 mA to 200 mA			150			180			200			240	
I_d	Quiescent current				6			6			6			6	mA
ΔI_d	Quiescent current change	I_o = 5 mA to 350 mA			0.5			0.5			0.5			0.5	mA
		I_o = 200 mA			0.8 (V_i = 17.5 to 30V)			0.8 (V_i = 21 to 33V)			0.8 (V_i = 23 to 35V)			0.8 (V_i = 27 to 38V)	
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o = 5 mA		-1			-1.1			-1.1			-1.2		mV/°C
e_N	Output noise voltage	B= 10Hz to 100KHz T_j = 25°C		90			100			110			170		μV
SVR	Supply voltage rejection	f = 120 Hz I_o = 300 mA T_j = 25°C	54 (V_i = 18.5 to 28.5V)			53 (V_i = 22 to 32V)			53 (V_i = 24 to 34V)			50 (V_i = 28 to 38V)			dB
V_d	Dropout Voltage	T_j = 25°C		2			2			2			2		V
I_{sc}	Short circuit current	V_i = 35V T_j = 25°C		240			240			240			240		mA
I_{scp}	Short circ. peak current	T_j = 25°C		700			700			700			700		mA

Fig. 4 - Dropout voltage vs. junction temperature

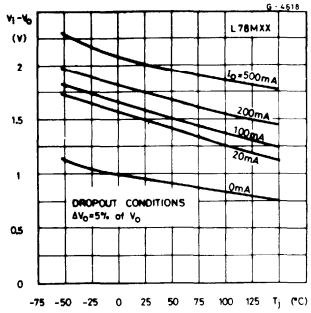


Fig. 5 - Dropout characteristics

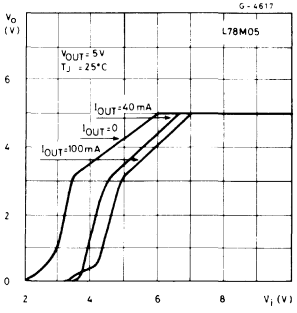


Fig. 6 - Peak output current vs. input-output differential voltage

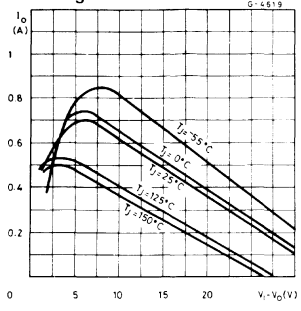


Fig. 7 - Output voltage vs. junction temperature

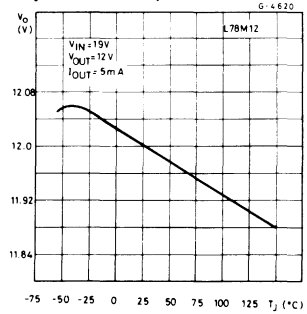


Fig. 8 - Supply voltage rejection vs. frequency

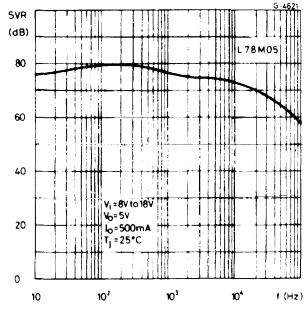


Fig. 9 - Quiescent current vs. junction temperature

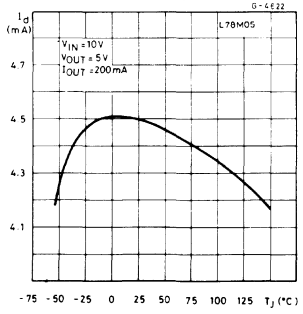


Fig. 10 - Load transient response

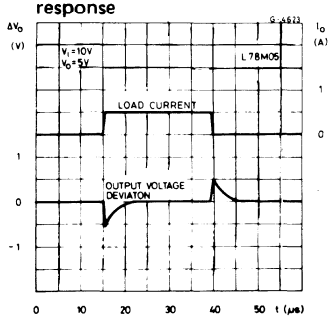


Fig. 11 - Line transient response

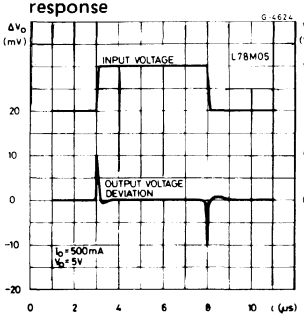
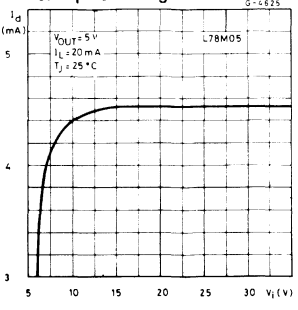


Fig. 12 - Quiescent current vs. input voltage



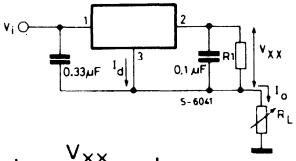
APPLICATIONS INFORMATION

Design Considerations

The L78M00AB Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

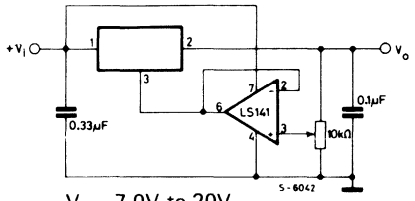
In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

Fig. 13 - Current regulator



$$I_o = \frac{V_{xx}}{R_1} + I_d$$

Fig. 14 - Adjustable output regulator

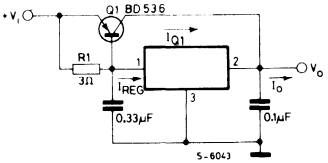


V_O, 7.0V to 20V

$V_i - V_O \geq 2.0V$

The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0V greater than the regulator voltage.

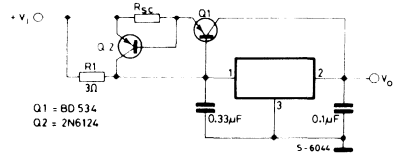
Fig. 15 - Current boost regulator



$$R_1 = \frac{V_{BEQ_1}}{I_{REG} - \frac{I_{Q_1}}{\beta_{Q_1}}}$$

$$I_o = I_{REG} + \beta_{Q_1}\left[I_{REG} - \frac{V_{BEQ_1}}{R_1}\right]$$

Fig. 16 - Short-circuit protection



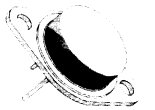
The circuit of Figure 6 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, R_{sc}, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, a four-ampere plastic power transistor is specified.

L78S00 Series

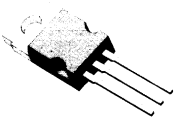
2A POSITIVE VOLTAGE REGULATORS

- OUTPUT CURRENT TO 2A
- OUTPUT VOLTAGES OF 5; 7.5; 9; 10; 12; 15; 18; 24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR SOA PROTECTION

The L78S00 series of three-terminal positive regulators is available in TO-220 and TO-3 packages and with several fixed output voltages, making it useful in a wide range of applications. These regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 2A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.



TO-3

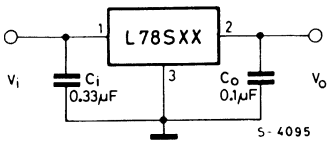


TO-220

ABSOLUTE MAXIMUM RATINGS

V_i	DC input voltage (for V_o = 5 to 18V)	35	V
	(for V_o = 24V)	40	V
I_o	Output current	internally limited	
P_{tot}	Power dissipation	Internally limited	
T_{stg}	Storage temperature	-65 to +150	°C
T_{op}	Operating junction temperature (for **L78S00**)	-55 to +150	°C
	(for **L78S00C**)	0 to +150	°C

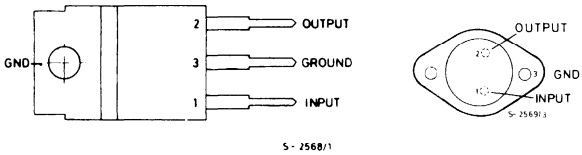
APPLICATION CIRCUIT



L78S00 Series

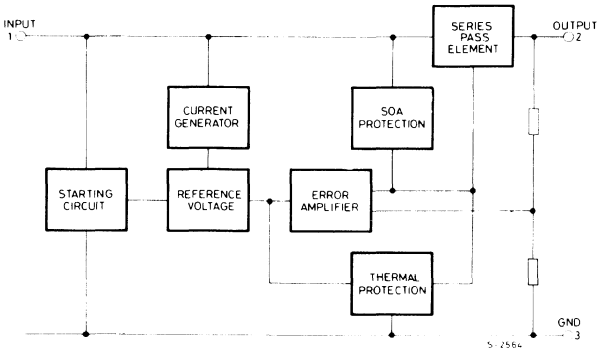
CONNECTION DIAGRAMS AND ORDERING NUMBERS

(top views)

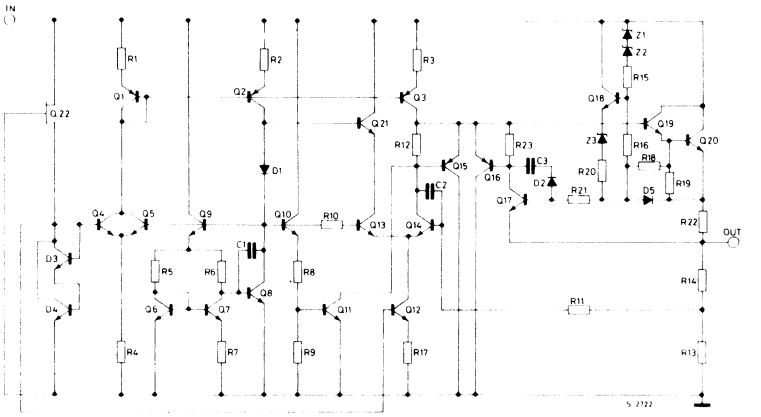


Type	TO-220	TO-3	Output voltage
L 78S05	–	L 78S05T	5V
L 78S05C	L 78S05CV	L 78S05CT	5V
L 78S75	–	L 78S75T	7.5V
L 78S75C	L 78S75CV	L 78S75CT	7.5V
L 78S09	–	L 78S09T	9V
L 78S09C	L 78S09CV	L 78S09CT	9V
L 78S10	–	L 78S10T	10V
L 78S10C	L 78S10CT	L 78S10CT	10V
L 78S12	–	L 78S12T	12V
L 78S12C	L 78S12CV	L 78S12CT	12V
L 78S15	–	L 78S15T	15V
L 78S15C	L 78S15CV	L 78S15CT	15V
L 78S18	–	L 78S18T	18V
L 78S18C	L 78S18CV	L 78S18CT	18V
L 78S24	–	L 78S24T	24V
L 78S24C	L 78S24CV	L 78S24CT	24V

BLOCK DIAGRAM



SCHEMATIC DIAGRAM



TEST CIRCUITS

Fig. 1 - DC parameters

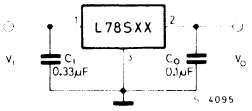


Fig. 2 - Load regulation

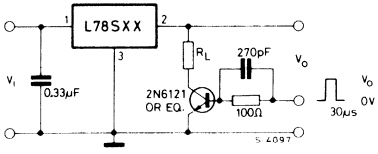
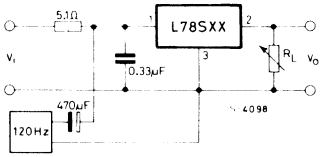


Fig. 3 - Ripple rejection



THERMAL DATA

			TO-220	TO-3
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3 °C/W	4 °C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50 °C/W	35 °C/W

ELECTRICAL CHARACTERISTICS L78S00 (Refer to the test circuits, T_j= 25°C, I_o= 500 mA unless otherwise specified)

OUTPUT VOLTAGE			5			7.5			9			10			Unit
INPUT VOLTAGE (Unless otherwise specified)			10			12.5			14			15			
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output voltage		4.8	5	5.2	7.15	7.5	7.9	8.65	9	9.35	9.5	10	10.5	V
		I_o= 1A	4.75	5	5.25 (V_i= 7V)	7.1	7.5	7.95 (V_i= 9.5V)	8.6	9	9.4 (V_i= 11V)	9.4	10	10.6 (V_i= 12.5V)	
ΔV_o	Line regulation				100 (V_i= 7 to 25V)			120 (V_i= 9.5 to 25V)			130 (V_i= 11 to 25V)			200 (V_i= 12.5 to 30V)	mV
					50 (V_i= 8 to 12V)			60 (V_i= 10.5 to 20V)			65 (V_i= 11 to 20V)			100 (V_i= 14 to 22V)	
ΔV_o	Load regulation	I_o= 20 mA to 2A			100			120			130			150	mV
I_d	Quiescent current				8			8			8			8	mA
ΔI_d	Quiescent current change	I_o= 20 mA to 1A			0.5			0.5			0.5			0.5	mA
		I_o= 20 mA			1.3 (V_i= 7 to 25V)			1.3 (V_i= 9.5 to 25V)			1.3 (V_i= 11 to 25V)			1 (V_i= 12.5 to 30V)	
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o= 5 mA T_j= -55 to 150°C		-1.1			-0.8			-1			-1		mV/°C
e_N	Output noise voltage	B= 10Hz to 100KHz		40			52			60			65		μV
SVR	Supply voltage rejection	f = 120 Hz	60			54			53			53			dB
V_i	Operating input voltage	$I_o \leqslant$ 1.5A	8			10.5			12			13			V
R_o	Output resistance	f = 1 KHz		17			16			17			17		mΩ
I_{sc}	Short circuit current	V_i = 27V		500			500			500			500		mA
I_{scp}	Short circ. peak current				4			4			4			4	A

ELECTRICAL CHARACTERISTICS L78S00 (continued)

OUTPUT VOLTAGE			12			15			18			24			Unit
INPUT VOLTAGE (Unless otherwise specified)			19			23			26			33			
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output voltage		11.5	12	12.5	14.4	15	15.6	17.1	18	18.9	23	24	25	V
		I_o= 1A	11.4 (V_i= 14.5V)	12	12.6	14.25 (V_i= 17.5V)	15	15.75	17 (V_i= 20.5V)	18	19	22.8 (V_i= 27V)	24	25.2	
ΔV_o	Line regulation				240 (V_i= 14.5 to 30V)			300 (V_i= 17.5 to 30V)			360 (V_i= 20.5 to 30V)			480 (V_i= 27 to 38V)	mV
					120 (V_i= 16 to 22V)			150 (V_i= 20 to 26V)			180 (V_i= 22 to 28V)			240 (V_i= 30 to 36V)	
ΔV_o	Load regulation	I_o= 20 mA to 2A			160			180			200			250	mV
I_d	Quiescent current				8			8			8			8	mA
ΔI_d	Quiescent current change	I_o= 20 mA to 1A			0.5			0.5			0.5			0.5	mA
		I_o= 20 mA			1 (V_i= 14.5 to 30V)			1 (V_i= 17.5 to 30V)			1 (V_i= 22 to 33V)			1 (V_i= 28 to 38V)	
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o= 5mA T_{amb}= 0 to 70°C		-1			-1			-1			-1.5		mV/°C
e_N	Output noise voltage	B= 10Hz to 100KHz		75			90			110			170		μV
SVR	Supply voltage rejection	f = 120 Hz	53			52			49			48			dB
V_i	Operating input voltage	I_o ≤ 1.5A	15			18			21			27			V
R_o	Output resistance	f = 1 KHz		18			19			22			23		mΩ
I_{sc}	Short circuit current	V_i = 27V	500			500			500			500			mA
I_{scp}	Short circ. peak current			4			4			4			4		A

ELECTRICAL CHARACTERISTICS L78S00C (Refer to the test circuits, T_j= 25°C, I_o= 500mA unless otherwise specified)

OUTPUT VOLTAGE			5			7.5			9			10			Unit
INPUT VOLTAGE (Unless otherwise specified)			10			12.5			14			15			
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output voltage		4.8	5	5.2	7.15	7.5	7.9	8.65	9	9.35	9.5	10	10.5	V
		I_o= 1A	4.75	5	5.25 (V_i= 7V)	7.1	7.5	7.95 (V_i= 9.5V)	8.6	9	9.4 (V_i= 11V)	9.4	10	10.6 (V_i= 12.5V)	
ΔV_o	Line regulation				100 (V_i= 7 to 25V)			120 (V_i= 9.5 to 25V)			130 (V_i= 11 to 25V)			200 (V_i= 12.5 to 30V)	mV
					50 (V_i= 8 to 12V)			60 (V_i= 10.5 to 20V)			65 (V_i= 11 to 20V)			100 (V_i= 14 to 22V)	
ΔV_o	Load regulation	I_o= 20 mA to 1.5A I_o = 2A			100 80			140 100			170 100			240 150	mV
I_d	Quiescent current				8			8			8			8	mA
ΔI_d	Quiescent current change	I_o= 20 mA to 1A			0.5			0.5			0.5			0.5	mA
		I_o= 20 mA			1.3 (V_i= 7 to 25V)			1.3 (V_i = 9.5 to 25V)			1.3 (V_i = 11 to 25V)			1.0 (V_i= 12.5 to 30V)	
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o= 5 mA T_{amb}= 0 to 70°C			-1.1			-0.8			-1			-1	mV/°C
e_N	Output noise voltage	B= 10Hz to 100KHz			40			52			60			65	μV
SVR	Supply voltage rejection	f = 120 Hz	54			48			47			47			dB
V_i	Operating input voltage	$I_o \leq$ 1.5A	8			10.5			12			13			V
R_o	Output resistance	f = 1 KHz		17			16			17			17		mΩ
I_{sc}	Short circuit current	V_i = 27V		500			500			500			500		mA
I_{scp}	Short circ. peak current				4			4			4			4	A

ELECTRICAL CHARACTERISTICS L78S00C (continued)

OUTPUT VOLTAGE			12	15	18	24	
INPUT VOLTAGE (Unless otherwise specified)			19	23	26	33	Unit
Parameter		Test conditions	Min. Typ. Max.	Min. Typ. Max.	Min. Typ. Max.	Min. Typ. Max.	
V_o	Output voltage		11.5 12 12.5	14.4 15 15.6	17.1 18 18.9	23 24 25	V
		I_o= 1A	11.4 12 12.6 (V_i= 14.5V)	14.25 15 15.75 (V_i= 17.5V)	17 18 19 (V_i= 20.5V)	22.8 24 25.2 (V_i= 27V)	
ΔV_o	Line regulation		240 (V_i= 14.5 to 30V)	300 (V_i= 17.5 to 30V)	360 (V_i= 20.5 to 30V)	480 (V_i= 27 to 38V)	mV
			120 (V_i= 16 to 22V)	150 (V_i= 20 to 26V)	180 (V_i= 22 to 28V)	240 (V_i= 30 to 36V)	
ΔV_o	Load regulation	I_o= 20 mA to 1.5A I_o = 2A	240 150	300 150	360 200	480 300	mV
I_d	Quiescent current		8	8	8	8	mA
ΔI_d	Quiescent current change	I_o= 20 mA to 1A	0.5	0.5	0.5	0.5	mA
		I_o= 20 mA	1.0 (V_i = 14.5 to 30V)	1.0 (V_i = 17.5 to 30V	1.0 (V_i = 20.5 to 30V)	1.0 (V_i = 27 to 38V)	
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o= 5mA T_{amb}= 0 to 70°C	-1	-1	-1	-1.5	mV/°C
e_N	Output noise voltage	B= 10Hz to 100KHz	75	90	110	170	μV
SVR	Supply voltage rejection	f = 120 Hz	47	46	43	42	dB
V_i	Operating input voltage	$I_o \leqslant$ 1.5A	15	18	21	27	V
R_o	Output resistance	f = 1 KHz	18	19	22	28	mΩ
I_{sc}	Short circuit current	V_i = 27V	500	500	500	500	mA
I_{scp}	Short circ. peak current		4	4	4	4	A

Fig. 4 - Dropout voltage vs. junction temperature

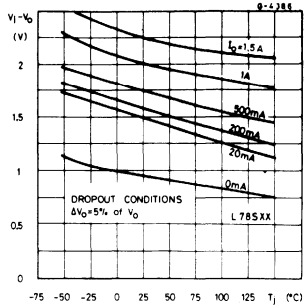


Fig. 5 - Peak output current vs. input/output differential voltage

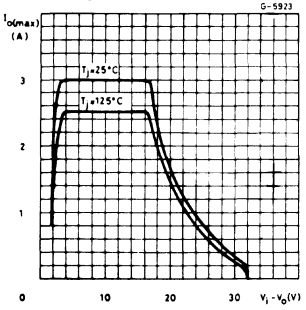


Fig. 6 - Supply voltage rejection vs. frequency

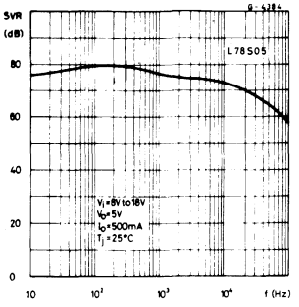


Fig. 7 - Output voltage vs. junction temperature

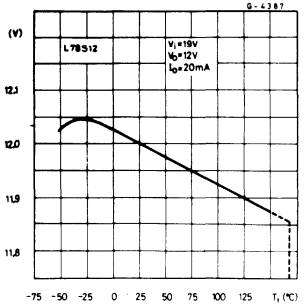


Fig. 8 - Output impedance vs. frequency

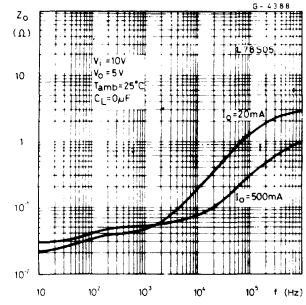


Fig. 9 - Quiescent current vs. junction temperature

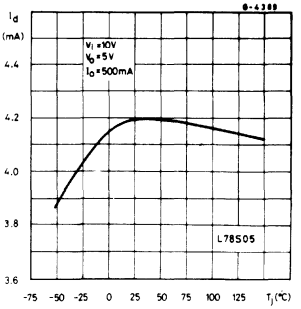


Fig. 10 - Load transient response

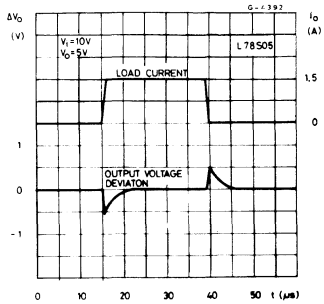


Fig. 11 - Line transient response

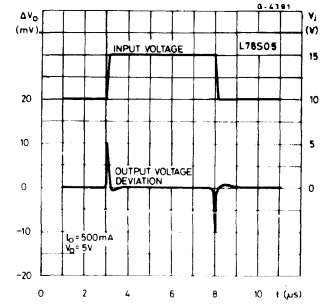
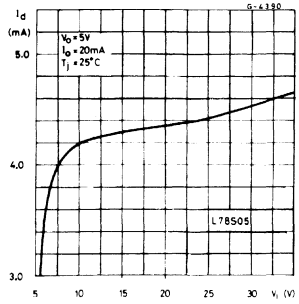
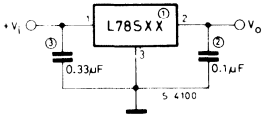


Fig. 12 - Quiescent current vs. input voltage



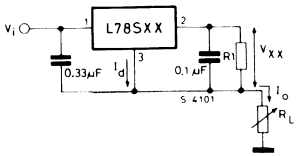
APPLICATION INFORMATION (continued)

Fig. 13 - Fixed output regulator



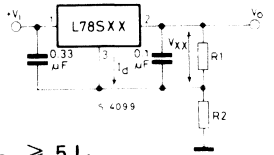
Notes:
(1) To specify an output voltage, substitute voltage value for "XX".
(2) Although no output capacitor is needed for stability, it does improve transient response.
(3) Required if regulator is located an appreciable distance from power supply filter.

Fig. 14 - Costant current regulator



$$I_o = \frac{V_{XX}}{R_1} + I_d$$

Fig. 15 - Circuit for increasing output voltage



$$I_{R_1} \geqslant 5\, I_d$$

$$V_o = V_{XX}\ (1 + \frac{R_2}{R_1}) + I_d\, R_2$$

Fig. 16 - Adjustable output regulator (7 to 30V)

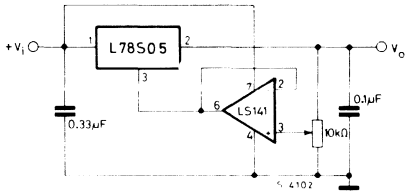
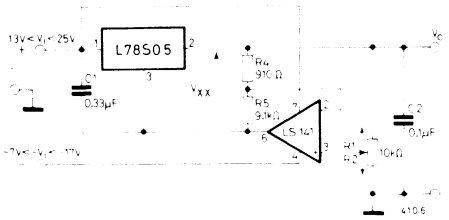
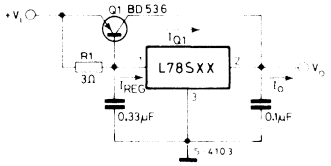


Fig. 17 - 0.5 to 10V regulator



$$V_o = V_{XX}\ \frac{R_4}{R_1}$$

Fig. 18 - High current voltage regulator

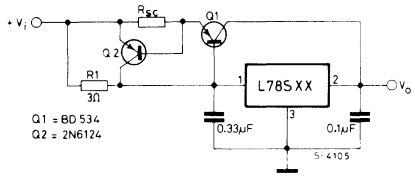


$$R_1 = \frac{V_{BEQ_1}}{I_{REG} - \frac{I_{Q_1}}{\beta_{Q_1}}}$$

$$I_o = I_{REG} + \beta_{Q_1}\ [I_{REG} - \frac{V_{BEQ_1}}{R_1}]$$

APPLICATION INFORMATION (continued)

Fig. 19 - High output current with short circuit protection



$$R_{SC} = \frac{V_{BEQ_2}}{I_{SC}}$$

Fig. 20 - Tracking voltage regulator

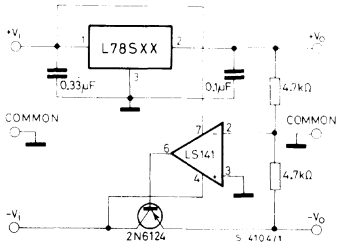
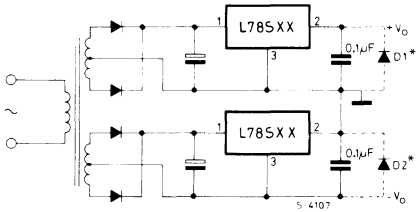


Fig. 21 - Positive and negative regulator



(*) D_1 and D_2 are necessary if the load is connected between $+V_o$ and $-V_o$

Fig. 22 - Negative output voltage circuit

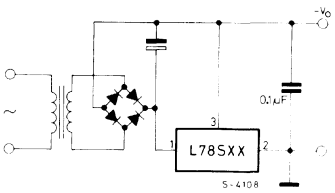


Fig. 23 - Switching regulator

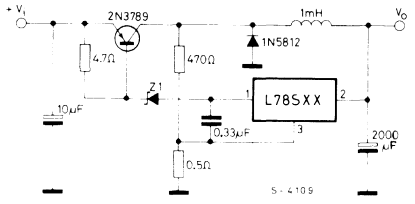
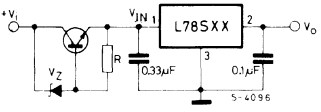


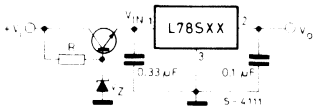
Fig. 24 - High input voltage circuit



$$V_{IN} = V_i - (V_Z + V_{BE})$$

APPLICATION INFORMATION (continued)

Fig. 25 - High input voltage circuit



$V_{IN} = V_Z - V_{BE}$

Fig. 26 - High output voltage regulator

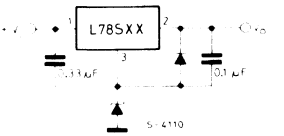
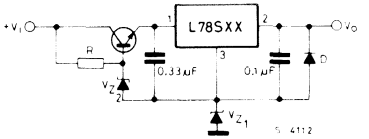
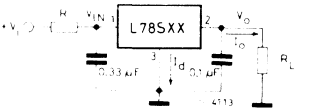


Fig. 27 - High input and output voltage



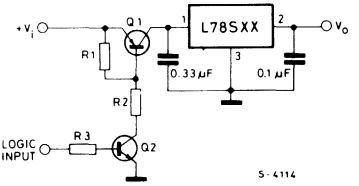
$V_O = V_{XX} + V_{Z1}$

Fig. 28 - Reducing power dissipation with dropping resistor



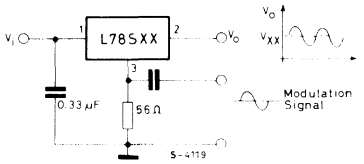
$$R = \frac{V_{i(min)} - V_{XX} - V_{DROP(max)}}{I_{o(max)} + I_{d(max)}}$$

Fig. 29 - Remote shuntdown



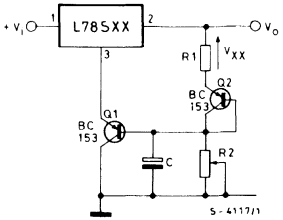
APPLICATION INFORMATION (continued)

Fig. 30 - Power AM modulator oscillator (unity voltage gain, $I_o \leqslant 1.5A$)



Note: The circuit performs well up to 100 KHz.

Fig. 31 - Adjustable output voltage with temperature compensation

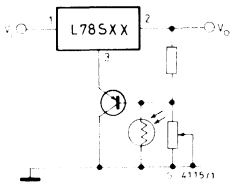


Note: Q_2 is connected as a diode in order to compensate the variation of the Q_1 V_{BE} with the temperature. C allows a slow rise-time of the V_o

$$V_o = V_{XX}\left(1 + \frac{R_2}{R_1}\right) + V_{BE}$$

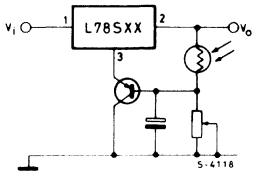
Fig. 32 - Light controllers ($V_{o\ min} = V_{XX} + V_{BE}$)

(a)



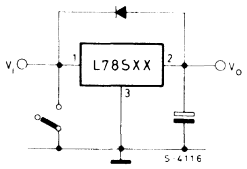
V_o falls when the light goes up

(b)



V_o rises when the light goes up

Fig. 33 - Protection against input short-circuit with high capacitance loads



Applications with high capacitance loads and an output voltage greater than 6 volts need an external diode (see fig. 33) to protect the device against input short circuit. In this case the input voltage falls rapidly while the output voltage decreases showly. The capacitance discharges by means of the Base-Emitter junction of the series pass transistor in the regulator. If the energy is sufficiently high, the transistor may be destroyed. The external diode by-passes the current from the IC to ground.

L7900 Series

NEGATIVE VOLTAGE REGULATORS

- OUTPUT CURRENT UP TO 1.5A
- OUTPUT VOLTAGES OF -5; -5.2; -8; -12; -15; -18; -20; -24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR SOA PROTECTION

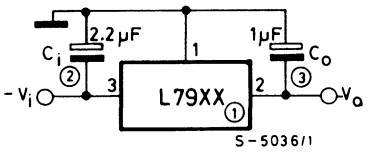
The L7900 series of three-terminal negative regulators is available in TO-220 and TO-3 packages and with several output voltages. They can provide local on-card regulation, eliminating the distribution problems associated with single point regulation; furthermore, having the same voltage options as the L7800 positive standard series, they are particularly suited for split power supplies. In addition, the -5.2V is also available for ECL system.
If adeguate heatsinking is provided, the L7900 series can deliver an output current in excess of 1.5A. Although designed primarly as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

TO-3 TO-220

ABSOLUTE MAXIMUM RATINGS

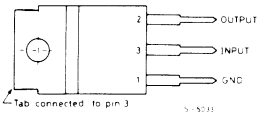
V_i	DC input voltage (for V_o = -5 to -18V)	-35	V
	(for V_o = -20, -24V)	-40	V
I_o	Output current	Internally limited	
P_{tot}	Total power dissipation	Internally limited	
T_{op}	Operating junction temperature	0 to +150	°C
T_{stg}	Storage temperature	-65 to +150	°C

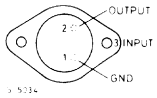
APPLICATION CIRCUIT



L7900 Series

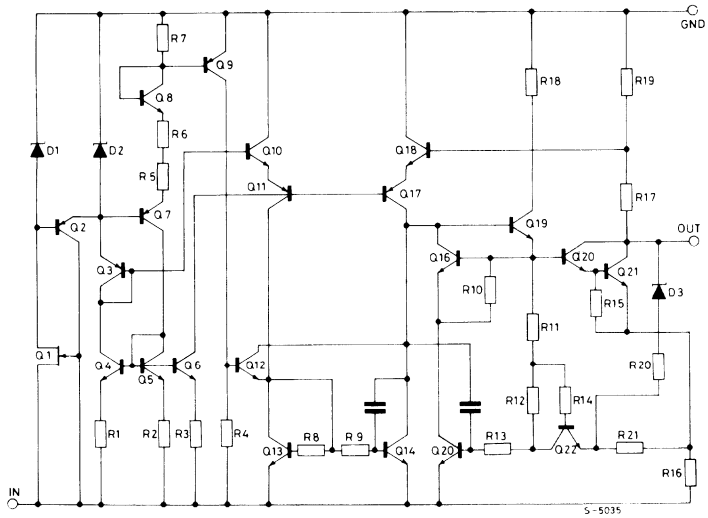
CONNECTION DIAGRAMS AND ORDERING NUMBERS
(top views)





Type	TO-220	TO-3	Output Voltage
L7905C	L7905CV	L7905CT	-5V
L7952C	L7952CV	L7952CT	-5.2V
L7908C	L7908CV	L7908CT	-8V
L7912C	L7912CV	L7912CT	-12V
L7915C	L7915CV	L7915CT	-15V
L7918C	L7918CV	L7918CT	-18V
L7920C	L7920CV	L7920CT	-20V
L7924C	L7924CV	L7924CT	-24V

SCHEMATIC DIAGRAM



THERMAL DATA

			TO-220	TO-3
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3 °C/W	4 °C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50 °C/W	35 °C/W

ELECTRICAL CHARACTERISTICS L7900C (C_i = 2.2 µF, C_o = 1 µF, T_j = 0 to 125°C, I_o = 500 mA unless otherwise specified)

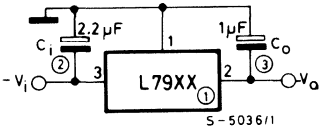
OUTPUT VOLTAGE			-5			-5.2			-8			-12			Unit
INPUT VOLTAGE (Unless otherwise specified)			-10			-10			-14			-19			
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output voltage	T_j = 25°C	-4.8	-5	-5.2	-5	-5.2	-5.4	-7.7	-8	-8.3	-11.5	-12	-12.5	V
		I_o = 5 mA to 1A, P_o < 15W	-4.75	-5	-5.25 (V_i = -8 to -20V)	-4.95	-5.2	-5.45 (V_i = -9 to -21V)	-7.6	-8	-8.4 (V_i = -11.5 to -23V)	-11.4	-12	-12.6 (V_i = -15.5 to -27V)	V
ΔV_o	Line regulation	T_j = 25°C			100 (V_i = -7 to -25V)			105 (V_i = -8 to -25V)			160 (V_i = -10.5 to -25V)			240 (V_i = -14.5 to -30V)	mV
					50 (V_i = -8 to -12V)			52 (V_i = -9 to -13V)			80 (V_i = -11 to -17V)			120 (V_i = -16 to -22V)	mV
ΔV_o	Load regulation	T_j = 25°C, I_o = 5 mA to 1.5A			100			105			160			240	mV
		T_j = 25°C, I_o = 250 to 750 mA			50			52			80			120	mV
I_d	Quiescent current	T_j = 25°C			2			2			2			3	mA
ΔI_d	Quiescent current change	I_o = 5 mA to 1A			0.5			0.5			0.5			0.5	mA
					1.3 (V_i = -8 to -25V)			1.3 (V_i = -9 to -25V)			1 (V_i = -11.5 to -25V)			1 (V_i = -15 to -30V)	mA
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o = 5 mA		-0.4			-0.5			-0.6			-0.8		mV/°C
e_N	Output noise voltage	B = 10Hz to 100KHz, T_j = 25°C		100			125			175			200		µV
SVR	Supply voltage rejection	f = 120 Hz, ΔV_i = 10V	54	60		54	60		54	60		54	60		dB
V_{i-o}	Dropout voltage	T_j = 25°C, I_o = 1A, ΔV_o = 100 mV		2			1.8			1.1			1.1		V
I_{sc}	Short circuit current			2.1			2			1.5			1.5		A
I_{scp}	Short circ. peak current	T_j = 25°C		2.5			2.5			2.5			2.5		A

ELECTRICAL CHARACTERISTICS (continued)

OUTPUT VOLTAGE			-15			-18			-20			-24			Unit
INPUT VOLTAGE (Unless otherwise specified)			-23			-27			-29			-33			
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output voltage	T_j = 25°C	-14.4	-15	-15.6	-17.3	-18	-18.7	-19.2	-20	-20.8	-23	-24	-25	V
		I_o= 5 mA to 1A P_o < 15W	-14.3 (V_i=-18.5 to -30V)	-15	-15.7	-17.1 (V_i= -22 to -33V)	-18	-18.9	-19 (V_i= -24 to -35V)	-20	-21	-22.8 (V_i= -27 to -38V)	-24	-25.2	
ΔV_o	Line regulation	T_j = 25°C			300 (V_i=-17.5 to -30V)			360 (V_i= -21 to -33V)			400 (V_i= -23 to -35V)			480 (V_i= -27 to -38V)	mV
					150 (V_i= -20 to -26V)			180 (V_i= -24 to -30V)			200 (V_i= -26 to -32V)			240 (V_i= -30 to -36V)	
ΔV_o	Load regulation	T_j= 25°C I_o= 5 mA to 1.5A			300			360			400			480	mV
		T_j= 25°C I_o= 250 to 750 mA			150			180			200			240	
I_d	Quiescent current	T_j= 25°C			3			3			3			3	mA
ΔI_d	Quiescent current change	I_o= 5 mA to 1A			0.5			0.5			0.5			0.5	mA
					1 (V_i=-18.5 to -30V)			1 (V_i= -22 to -33V)			1 (V_i= -24 to -35V)			1 (V_i= -27 to -38V)	
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o= 5 mA		-0.9			-1			-1.1			-1		mV/°C
e_N	output noise voltage	B= 10Hz to 100KHz T_j= 25°C		250			300			350			400		μV
SVR	Supply voltage rejection	f = 120 Hz ΔV_i= 10V	54	60		54	60		54	60		54	60		dB
V_{i-o}	Dropout voltage	T_j= 25°C I_o= 1A ΔV_o= 100 mV		1.1			1.1			1.1			1.1		V
I_{sc}	Short circuit current			1.3			1.1			0.9			1.1		A
I_{scp}	Short circ. peak current	T_j= 25°C		2.2			2.2			2.2			2.2		A

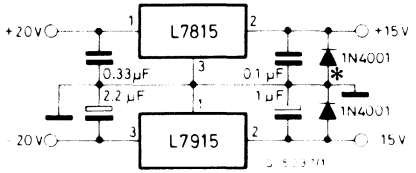
APPLICATION INFORMATION

Fig. 1 - Fixed output regulator



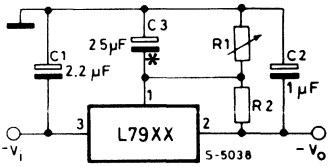
Notes:
(1) To specify an output voltage, substitute voltage value for "XX".
(2) Required for stability. For value given, capacitor must be solid tantalum. If aluminium electrolitics are used, at least ten times value shown should be selected. C_i is required if regulator is located an appreciable distance from power supply filter.
(3) To improve transient response. If large capacitors are used, a high current diode from input to output (1N4001 or similar) should be introduced to protect the device from momentary input short circuit.

Fig. 2 - Split power supply (± 15V/1A)



* Against potential latch-up problems.

Fig. 3 - Circuit for increasing output voltage



$$V_o \cong V_{xx} \cdot \frac{R1 + R2}{R2} \qquad \frac{V_{xx}}{R2} > 3\, I_d$$

* C3 optional for improved transient response and ripple rejection.

Fig. 4 - High current negative regulator (-5V/4A with 5A current limiting)

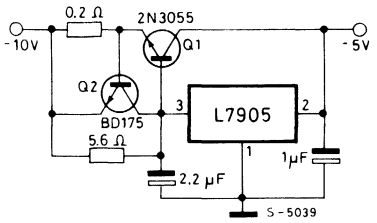
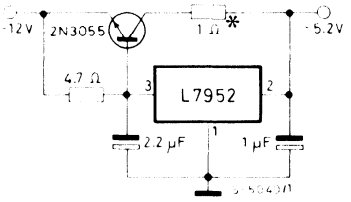


Fig. 5 - Typical ECL system power supply (-5.2V/ 4A)



* Optional dropping resistor to reduce the power dissipated in the boost transistor.

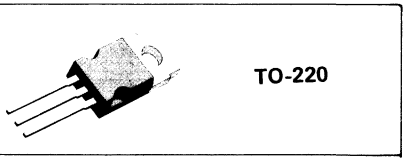
L7900AC Series

± 2% NEGATIVE VOLTAGE REGULATORS

- OUTPUT CURRENT UP TO 1.5A
- OUTPUT VOLTAGES OF -5; -5.2; -8; -12; -15; -18; -20; -24V
- THERMAL CIRCUIT PROTECTION
- OUTPUT TRANSISTOR SOA PROTECTION

The L7900AC series of three-terminal negative regulators is available in TO-220 package and with several output voltage. They can provide local on-card regulation, eliminating the distribution problems associated with single point regulation; furthermore, having the same voltage options as the L7800 positive standard series, they are particularly suited for split power supplies.

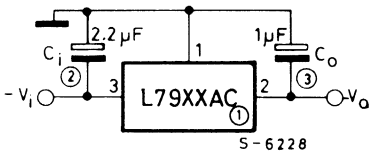
In addition, the -5.2V is also available for ECL system.
If adeguate heatsinking is provided, the L7900AC series can deliver an output current in excess of 1.5A Although designed primarly as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.



ABSOLUTE MAXIMUM RATINGS

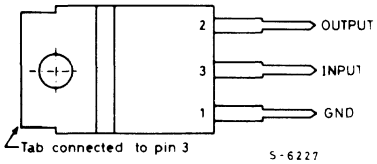
V_i	DC input voltage (for V_o = -5 to -18V)	-35 V
	(for V_o = -20, -24V)	-40 V
I_o	Output current	Internally limited
P_{tot}	Total power dissipation	Internally limited
T_{op}	Operating junction temperature	0 to +150 °C
T_{stg}	Storage temperature	-65 to +150 °C

APPLICATION CIRCUIT



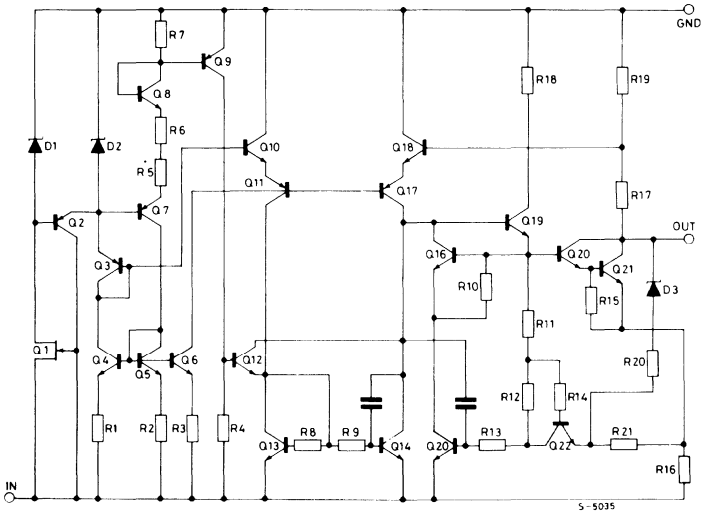
L7900AC Series

CONNECTION DIAGRAMS AND ORDERING NUMBERS
(top views)



Ordering Numbers	Output Voltage
L7905ACV	-5V
L7952ACV	-5.2V
L7908ACV	-8V
L7912ACV	-12V
L7915ACV	-15V
L7918ACV	-18V
L7920ACV	-20V
L7924ACV	-24V

SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3 °C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50 °C/W

ELECTRICAL CHARACTERISTICS L7900AC (C_i = 2.2 μF, C_o = 1 μF, T_j = 0 to 125°C, I_o = 500 mA unless otherwise specified)

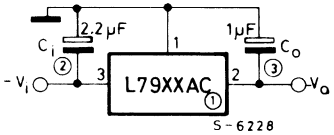
OUTPUT VOLTAGE			-5			-5.2			-8			-12			Unit
INPUT VOLTAGE (Unless otherwise specified)			-10			-10			-14			-19			
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output voltage	T_j= 25°C	-4.9	-5	-5.1	-5.1	-5.2	-5.3	-7.84	-8	-8.16	-11.75	-12	-12.25	V
		I_o= 5 mA to 1A P_o < 15W	-4.8	-5	-5.2 (V_i= -8 to -20V)	-5.0	-5.2	-5.4 (V_i= -9 to -21V)	-7.7	-8	-8.3 (V_i= -11.5 to -23V)	-11.5	-12	-12.5 (V_i= -15.5 to -27V)	
ΔV_o	Line regulation	T_j = 25°C			100 (V_i= -7 to -25V)			105 (V_i= -8 to -25V)			160 (V_i= -10.5 to -25V)			240 (V_i= -14.5 to -30V)	mV
					50 (V_i= -8 to -12V)			52 (V_i= -9 to -13V)			80 (V_i= -11 to -17V)			120 (V_i= -16 to -22V)	
ΔV_o	Load regulation	T_j= 25°C I_o= 5 mA to 1.5A			100			105			160			240	mV
		T_j= 25°C I_o= 250 to 750 mA			50			52			80			120	
I_d	Quiescent current	T_j= 25°C			2			2			2			3	mA
ΔI_d	Quiescent current change	I_o= 5 mA to 1A			0.5			0.5			0.5			0.5	mA
					1.3 (V_i= -8 to -25V)			1.3 (V_i= -9 to -25V)			1 (V_i=-11.5 to -25V)			1 (V_i= -15 to -30V)	
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o= 5 mA		-0.4			-0.5			-0.6			-0.8		mV/°C
e_N	Output noise voltage	B = 10Hz to 100KHz T_j= 25°C		100			125			175			200		μV
SVR	Supply voltage rejection	f = 120 Hz ΔV_i= 10V	54	60		54	60		54	60		54	60		dB
V_{i-o}	Dropout voltage	T_j= 25°C I_o= 1A ΔV_o= 100 mV		2			1.8			1.1			1.1		V
I_{sc}	Short circuit current			2.1			2			1.5			1.5		A
I_{scp}	Short circ. peak current	T_j= 25°C		2.5			2.5			2.5			2.5		A

ELECTRICAL CHARACTERISTICS (continued)

OUTPUT VOLTAGE			-15			-18			-20			-24			Unit
INPUT VOLTAGE (Unless otherwise specified)			-23			-27			-29			-33			
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output voltage	T_j = 25°C	-14.7	-15	-15.3	-17.64	-18	-18.36	-19.6	-20	-20.4	-23.5	-24	-24.5	V
		I_o= 5 mA to 1A P_o < 15W	-14.4	-15	-15.6 (V_i=-18.5 to -30V)	-17.3	-18	-18.7 (V_i= -22 to -33V)	-19.2	-20	-20.8 (V_i= -24 to -35V)	-23	-24	-25 (V_i= -27 to -38V)	
ΔV_o	Line regulatio	T_j = 25°C			300 (V_i=-17.5 to -30V)			360 (V_i= -21 to -33V)			400 (V_i= -23 to -35V)			480 (V_i= -27 to -38V)	mV
					150 (V_i= -20 to -26V)			180 (V_i= -24 to -30V)			200 (V_i= -26 to -32V)			240 (V_i= -30 to -36V)	
ΔV_o	Load regulation	T_j= 25°C I_o= 5 mA to 1.5A			300			360			400			480	mV
		T_j= 25°C I_o= 250 to 750 mA			150			180			200			240	
I_d	Quiescent current	T_j= 25°C			3			3			3			3	mA
ΔI_d	Quiescent current change	I_o= 5 mA to 1A			0.5			0.5			0.5			0.5	mA
					1 (V_i=-18.5 to -30V)			1 (V_i= -22 to -33V)			1 (V_i= -24 to -35V)			1 (V_i= -27 to -38V)	
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o= 5 mA		-0.9			-1			-1.1			-1		mV/°C
e_N	output noise voltage	B= 10Hz to 100KHz T_j= 25°C		250			300			350			400		μV
SVR	Supply voltage rejection	f = 120 Hz ΔV_i= 10V	54	60		54	60		54	60		54	60		dB
V_{i-o}	Dropout voltage	T_j= 25°C I_o= 1A ΔV_o= 100 mV		1.1			1.1			1.1			1.1		V
I_{sc}	Short circuit current			1.3			1.1			0.9			1.1		A
I_{scp}	Short circ. peak current	T_j= 25°C		2.2			2.2			2.2			2.2		A

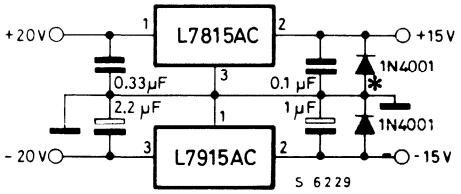
APPLICATION INFORMATION

Fig. 1 - Fixed output regulator



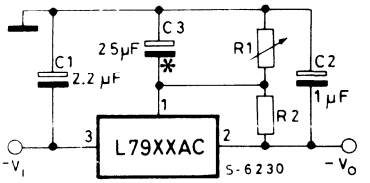
Notes:
(1) To specify an output voltage, substitute voltage value for "XX".
(2) Required for stability. For value given, capacitor must be solid tantalum. If aluminium electrolitics are used, at least ten times value shown should be selected. C_i is required if regulator is located an appreciable distance from power supply filter.
(3) To improve transient response. If large capacitors are used, a high current diode from input to output (1N4001 or similar) should be introduced to protect the device from momentary input short circuit.

Fig. 2 - Split power supply (± 15V/1A)



* Against potential latch-up problems.

Fig. 3 - Circuit for increasing output voltage



$$V_o \cong V_{xx} \cdot \frac{R1 + R2}{R2} \qquad \frac{V_{xx}}{R2} > 3\, I_d$$

* C3 optional for improved transient response and ripple rejection.

Fig. 4 - High current negative regulator (-5V/4A with 5A current limiting)

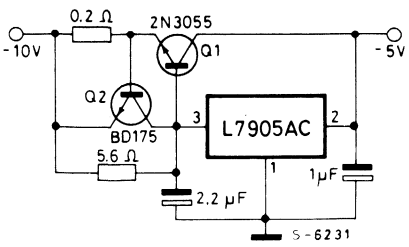
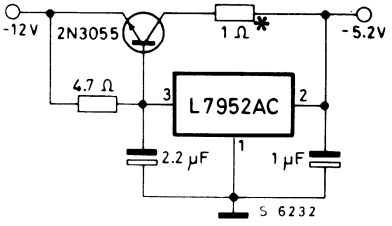


Fig. 5 - Typical ECL system power supply (-5.2V/ 4A)



* Optional dropping resistor to reduce the power dissipated in the boost transistor.

1.2V TO 37V ADJUSTABLE VOLTAGE REGULATOR

- OUTPUT VOLTAGE RANGE: 1.2 TO 37V
- OUTPUT CURRENT IN EXCESS OF 1.5A
- 0.1% LINE AND LOAD REGULATION
- FLOATING OPERATION FOR HIGH VOLTAGES
- COMPLETE SERIES OF PROTECTIONS: CURRENT LIMITING, THERMAL SHUTDOWN AND SOA CONTROL.

The LM117/LM217/LM317 are monolithic integrated circuit in TO-220 and TO-3 packages intended for use as positive adjustable voltage regulators.

They are designed to supply more than 1.5A of load current with an output voltage adjustable over a 1.2 to 37V range.

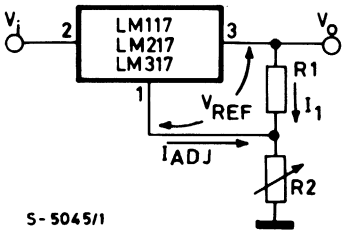
The nominal output voltage is selected by means of only a resistive divider, making the device exceptionally easy to use and eliminating the stocking of many fixed regulators.

TO-220 TO-3

ABSOLUTE MAXIMUM RATINGS

V_{i-o}	Input-output differential voltage		40 V
I_o	Output current		Internally limited
T_{op}	Operating junction temperature for:	LM 117	-55 to 150 °C
		LM 217	-25 to 150 °C
		LM 317	0 to 125 °C
P_{tot}	Power dissipation		Internally limited
T_{stg}	Storage temperature		-65 to 150 °C

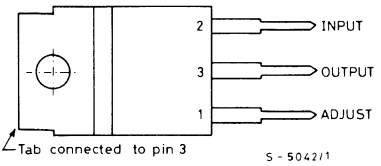
Basic adjustable regulator

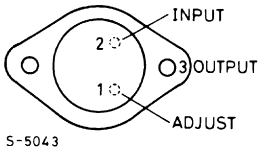


LM117
LM217
LM317

CONNECTION DIAGRAMS AND ORDERING NUMBERS

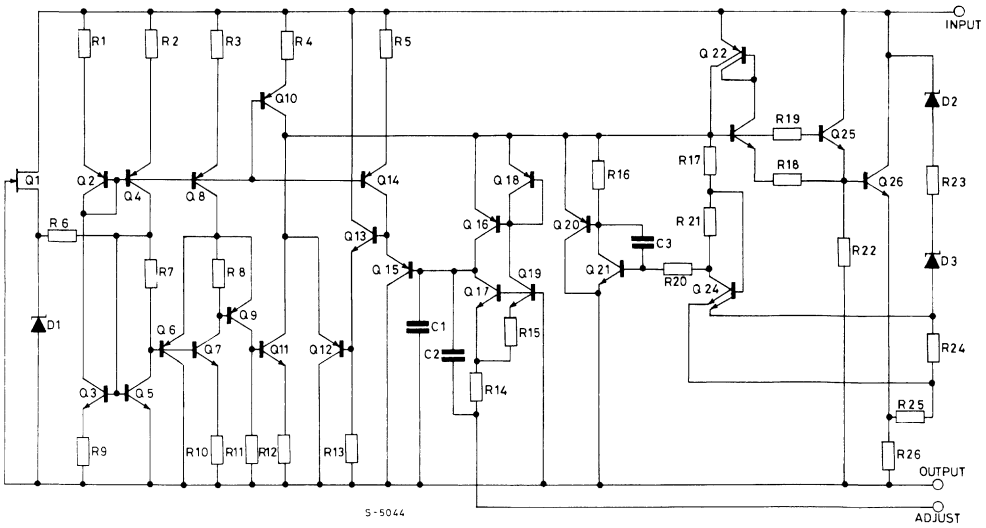
(top views)





Type	TO-220	TO-3
LM 117	—	LM 117K
LM 217	—	LM 217K
LM 317	LM 317T	LM 317K

SCHEMATIC DIAGRAM



THERMAL DATA

			TO-3	TO-220
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4 °C/W	4 °C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	35 °C/W	50 °C/W

ELECTRICAL CHARACTERISTICS (V_i-V_o = 5V, I_o = 500 mA, unless otherwise specified)

Parameter		Test conditions		LM 117/LM 217			LM 317			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
ΔV_o	Line regulation	V_i-V_o= 3 to 40V	T_j= 25°C		0.01	0.02		0.01	0.04	%/V
					0.02	0.05		0.02	0.07	
ΔV_o	Load regulation	$V_o \leqslant$ 5V, I_o= 10mA to 1.5A	T_j= 25°C		5	15		5	25	mV
					20	50		20	70	
		$V_o \geqslant$ 5V, I_o= 10 mA to 1.5A	T_j= 25°C		0.1	0.3		0.1	0.5	%
					0.3	1		0.3	1.5	
I_{ADJ}	Adjustment pin current				50	100		50	100	μA
ΔI_{ADJ}	Adjustment pin current	V_i-V_o= 2.5 to 40V, I_o= 10 mA to 1.5A			0.2	5		0.2	5	μA
V_{REF}	Reference voltage (between pin 3 and pin 1)	V_i-V_o= 3 to 40V, I_o= 10 mA to 1.5A		1.2	1.25	1.3	1.2	1.25	1.3	V
$\frac{\Delta V_o}{V_o}$	Output voltage temperature stability				1			1		%
$I_{o\,min}$	Minimum load current	V_i-V_o = 40V			3.5	5		3.5	10	mA
$I_{o\,max}$	Maximum load current	V_i-$V_o \leqslant$ 15V		1.5	2.2		1.5	2.2		A
		V_i-V_o= 40V			0.4			0.4		
e_N	Output noise (percentage of V_o)	T_j= 25°C, 10Hz to 10KHz			0.003			0.003		%
SVR	Supply voltage rejection (*)	T_j= 25°C, f = 120 Hz	C_{ADJ}= 0		65			65		dB
			C_{ADJ}= 10 μF	66	80		66	80		

(*) C_{ADJ} is connected between pin 1 and ground.

Note – Unless otherwise specified the above specs, apply over the following conditions: LM 117 T_j= -55 to 150°C; LM 217 T_j = -25 to 150°C; LM 317 T_j = 0 to 125°C.

Fig. 1 - Output current vs. input-output differential voltage

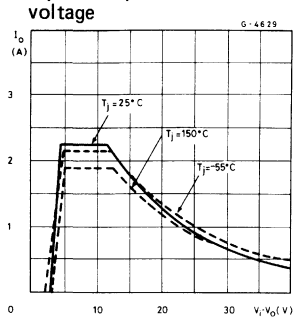


Fig. 2 - Dropout voltage vs. junction temperature

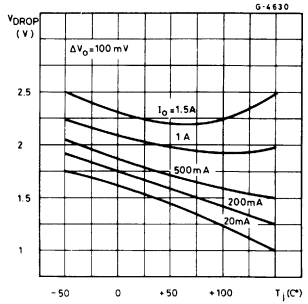
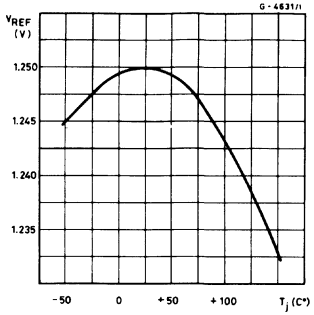


Fig. 3 - Reference voltage vs. junction temperature

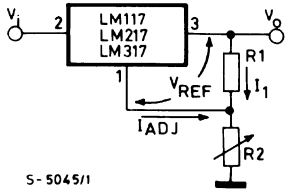


APPLICATION INFORMATION

The LM 117/LM 217/LM 317 provides an internal reference voltage of 1.25V between the output and adjustment terminals. This is used to set a constant current flow across an external resistor divider (see fig. 4), giving an output voltage V_o of:

$$V_o = V_{REF} \left(1 + \frac{R2}{R1}\right) + I_{ADJ}\ R2$$

Fig. 4 - Basic adjustable regulator



The device was designed to minimize the term I_{ADJ} (100 μA max) and to maintain it very constant with line and load changes. Usually, the error term $I_{ADJ} \cdot R2$ can be neglected. To obtain the previous requirement, all the regulator quiescent current is returned to the output terminal, imposing a minimum load current condition. If the load is insufficient, the output voltage will rise.

Since the LM 117/LM 217/LM 317 is a floating regulator and "sees" only the input-to-output differential voltage, supplies of very high voltage with respect to ground can be regulated as long as the maximum input-to-output differential is not exceeded. Furthermore, programmable regulator are easily obtainable and, by connecting a fixed resistor between the adjustment and output, the device can be used as a precision current regulator.

In order to optimise the load regulation, the current set resistor R1 (see fig. 4) should be tied as close as possible to the regulator, while the ground terminal of R2 should be near the ground of the load to provide remote ground sensing.

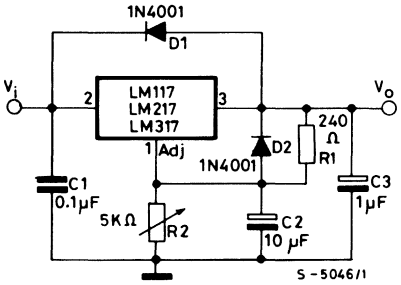
No external capacitors are required, but performance may be improved with added capacitance as follows:

- An input bypass capacitor of 0.1 μF.
- An adjustment terminal to ground 10 μF capacitor to improve the ripple rejection of about 15 dB (C_{ADJ}).
- An 1 μF tantalum capacitor on the output to improve transient response.

APPLICATION INFORMATION (continued)

In additional to external capacitors, it is good practice to add protection diodes, as shown in fig. 5.

Fig. 5 - Voltage regulator with protection diodes.



D1 protects the device against input short circuit, while D2 protects against output short circuit for capacitors discharging.

Fig. 6 - Slow turn-on 15V regulator

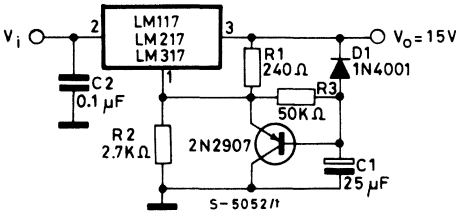
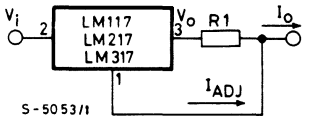


Fig. 7 - Current regulator



$$I_o = \frac{V_{ref}}{R1} + I_{ADJ} \cong \frac{1.25V}{R1}$$

(I_o = 10 mA to 1.5A)

Fig. 8 - 5V electronic shut-down regulator

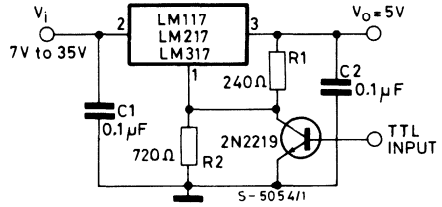
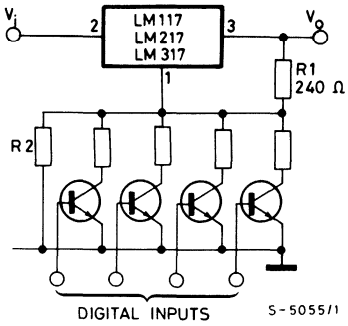


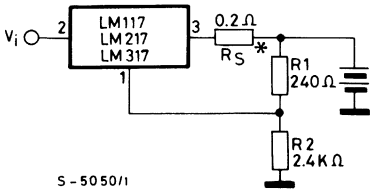
Fig. 9 - Digitally selected outputs



(R2 sets maximum V_o)

APPLICATION INFORMATION (continued)

Fig. 10 - Battery charger (12V).

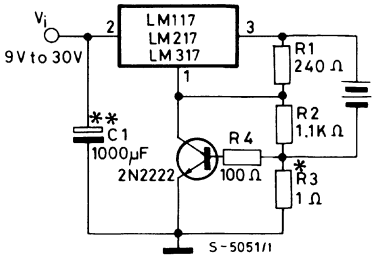


* R_S sets output impedance of charger

$$Z_o = R_s\left(1 + \frac{R2}{R1}\right)$$

Use of R_S allows low charging rates with fully charged battery.

Fig. 11 - Current limited 6V charger.



* R3 sets peak current (0.6A for 1Ω).

** C1 recommended to filter out input transients.

QUAD OPERATIONAL AMPLIFIERS

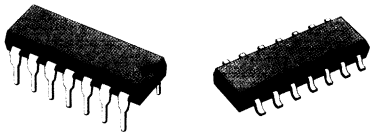
- SINGLE OR SPLIT POWER SUPPLY
- VERY LOW POWER CONSUMPTION
- INPUT COMMON-MODE RANGE INCLUDING GROUND
- LARGE DC VOLTAGE GAIN (100 dB)

The LM124 series consist of four indipendent, high gain, internally frequency compensated opamps specifically designed to operate from a single power supply over a wide range of voltages.

Both in split and in single supply the current drain is independent of the magnitude of the power supply voltage.

In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operating from only a single power supply voltage.

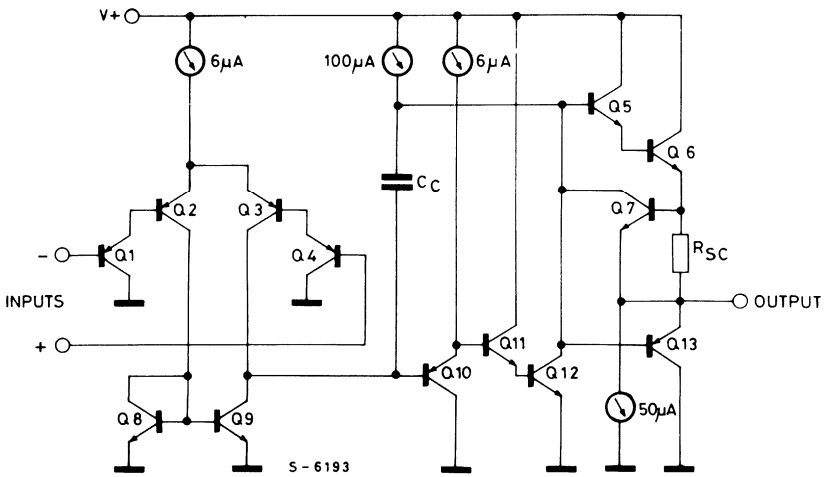
The LM124 is available in a standard 14-lead dual in-line plastic or ceramic package and in a 14-lead micropackage version.



DIP-14
(Plastic and Ceramic)

SO-14

SCHEMATIC DIAGRAM
(one section)

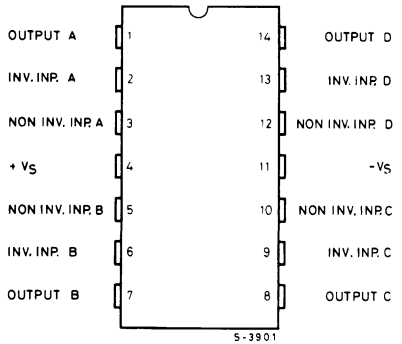


ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage		32	V
	Supply voltage (**LM2902** only)		26	V
V_i	Input voltage (single supply)		-0.3 to 26	V
V_i	Differential input voltage		32	V
T_{op}	Operating temperature for:	**LM2902**	-40 to 85	°C
		LM324/324A	0 to 70	°C
		LM224/224A	-25 to 85	°C
		LM124/124A	-55 to 125	°C
T_j	Junction temperature		150	°C
T_{stg}	Storage temperature		-65 to 150	°C

CONNECTION DIAGRAM AND ORDERING NUMBERS

(top view)



Temperature range	Ceramic DIP-14	Plastic DIP-14	SO-14
Commercial 0 to 70°C	LM324J LM324AJ	LM324N LM324AN	LM324D
Industrial -25 to 85°C	LM224J LM224AJ	LM224N	LM224D
Automotive -40 to 85°C	LM2902J	LM2902N	LM2902D
Military -55 to 125°C	LM124J LM124AJ	—	—

THERMAL DATA

			Ceramic DIP-14	SO-14	Plastic DIP-14
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	150°C/W	165°C/W	200°C/W

ELECTRICAL CHARACTERISTICS (V_s = +5V, T_{amb} = -55 to 125°C for the LM124/LM124A and T_{amb} = -25 to 85°C for the LM224/LM224A unless otherwise specified)

Parameter		Test conditions		LM124/LM224			LM124A			LM224A			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_S	Supply current	$R_L = \infty$	V_s = 30V		1.5	3		1.5	3		1.5	3	mA
					0.7	1.2		0.7	1.2		0.7	1.2	
I_b	Input bias current	T_{amb} = 25°C			45	150		20	50		40	80	nA
					40	300		40	100		40	100	
V_{os}	Input offset voltage	R_g = 0 V_s = 5V to 30V	T_{amb} = 25°C		2	5		1	2		1	3	mV
						7			4			4	
$\frac{\Delta V_{os}}{\Delta T}$	Input offset voltage drift	R_g = 0			7			7	20		7	20	µV/°C
I_{os}	Input offset current	T_{amb} = 25°C			3	30		2	10		2	15	nA
						100			30			30	
$\frac{\Delta I_{os}}{\Delta T}$	Input offset current drift				10			10	200		10	200	pA/°C
I_{sc}	Output short circuit to ground current	T_{amb} = 25°C (*)			40	60		40	60		40	60	mA
G_v	Large signal open loop voltage gain	V_s = 15V $R_L \geqslant 2$ KΩ	T_{amb} = 25°C	94	100		94	100		94	100		dB
				88			88			88			
	Input common-mode voltage range	V_s = 30V	T_{amb} = 25°C	0		V_s-1.5	0		V_s-1.5	0		V_s-1.5	V
				0		V_s-2	0		V_s-2	0		V_s-2	
V_o	Output voltage swing	T_{amb} = 25°C	R_L = 2 KΩ			V_s-1.5			V_s-1.5				V
			$R_L \geqslant$ 10 KΩ									V_s-1.5	
		V_s = 30V	R_L = 2 KΩ	26			26			26			V
			$R_L \geqslant$ 10 KΩ	27	28		27	28		27	28		
$V_{o\ sat}$	Output saturation voltage to ground	$R_L \leqslant$ 10 KΩ			5	20		5	20		5	20	mV
CMR	Common mode rejection	T_{amb} = 25°C		70	85		70	85		70	85		dB
SVR	Supply voltage rejection	T_{amb} = 25°C		65	100		65	100		65	100		dB
CS	Channel separation	f = 1 KHz to 20 KHz T_{amb} = 25°C (Input referred)			120			120			120		dB
I_o^+	Output source current	V_s = 15V V_i^+ = 1V V_i^- = 0V	T_{amb} = 25°C	20	40		20	40		20	40		mA
				10	20		10	20		10	20		
I_o^-	Output sink current	V_i^+ = 0V V_i^- = 1V V_o = 200 mV	T_{amb} = 25°C	12	50		12	50		12	50		µA
		V_i^- = 1V V_i^+ = 0V V_s = 15V	T_{amb} = 25°C	10	20		10	20		10	20		mA
				5	8		10	15		5	8		

(*) Short circuits from the output to positive supply voltage can cause excessive heating and eventual destruction. The maximum output current is 40 mA typ. independent of the magnitude of V_s. Destructive dissipation can result from simultaneous shorts on all amplifiers.

ELECTRICAL CHARACTERISTICS (V_s = + 5V, T_{amb} = 0 to 70°C for the LM324A/LM324 and T_{amb} = -40 to 85°C for the LM2902, unless otherwise specified).

Parameter		Test conditions		LM 324			LM 324A			LM 2902			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_S	Supply current	$R_L = \infty$	V_s = 30V (*)		1.5	3		1.5	3		1.5	3	mA
					0.7	1.2		0.7	1.2		0.7	1.2	
I_b	Input bias current	T_{amb} = 25°C			45	250		45	100		45	250	nA
						500			200			500	
V_{os}	Input offset voltage	R_g = 0, V_s = 5V to 30V (*)	T_{amb} = 25°C		2	7		2	3		2	7	V
						9			5			10	
$\frac{\Delta V_{os}}{\Delta T}$	Input offset voltage drift	R_g = 0			7			7	30		7		µV/°C
I_{os}	Input offset current	T_{amb} = 25°C			5	50		5	30		5	50	nA
						150			75			200	
$\frac{\Delta I_{os}}{\Delta T}$	Input offset current drift				10			10	300		10		pA/°C
I_{sc}	Output short circuit to ground current	T_{amb} = 25°C (**)			40	60		40	60		40	60	mA
G_v	Large signal open loop voltage gain	V_s = 15V, $R_L \geqslant$ 2 KΩ	T_{amb} = 25°C	88	100		88	100			100		dB
				83			83			83			
	Input common-mode voltage range	V_s = 30V (*)	T_{amb} = 25°C	0		V_s-1.5	0		V_s-1.5	0		V_s-1.5	V
				0		V_s-2	0		V_s-2	0		V_s-2	
V_o	Output voltage swing	T_{amb} = 25°C	R_L = 2 KΩ			V_s-1.5			V_s-1.5				V
			$R_L \geqslant$ 10 KΩ									V_s-1.5	
		V_s = 30V (*)	R_L = 2 KΩ	26			26			22			V
			$R_L \geqslant$ 10 KΩ	27	28		27	28		23	24		
$V_{o\ sat}$	Output saturation voltage to ground	$R_L \leqslant$ 10 KΩ			5	20		5	20		5	100	mV
CMR	Common mode rejection	T_{amb} = 25°C		65	70		65	85		50	70		dB
SVR	Supply voltage rejection	T_{amb} = 25°C		65	70		65	100		50	70		dB
CS	Channel separation	f = 1 KHz to 20 KHz, T_{amb} = 25°C (Input referred)			120			120			120		dB
I_{o^+}	Output source current	V_s = 15V, V_{i^+} = 1V, V_{i^-} = 0V	T_{amb} = 25°C	20	40		20	40		20	40		mA
				10	20		10	20		10	20		
I_{o^-}	Output sink current	V_{i^+} = 0V, V_{i^-} = 1V, V_o = 200 mV	T_{amb} = 25°C	12	50		12	50					µA
		V_{i^-} = 1V, V_{i^+} = 0V, V_s = 15V	T_{amb} = 25°C	10	20		10	20		10	20		mA
				5	8		5	8		5	8		

(*) V_s = 26V for LM2902.

(**) Short circuits from the output to positive supply voltage can cause excessive heating and eventual destruction. The maximum output current it 40mA typ. independent of the magnitude of V_s. Destructive dissipation can result from simultaneous short on all amplifiers.

Fig. 1 - Supply current vs. supply voltage

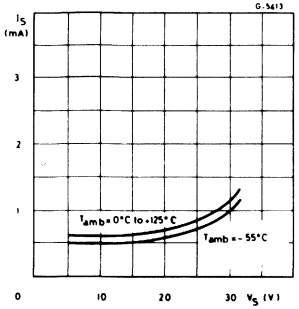


Fig. 2 - Input voltage range vs. supply voltage

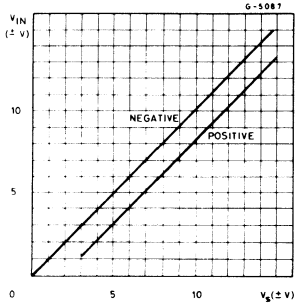


Fig. 3 - Output short circuit current vs. ambient temperature

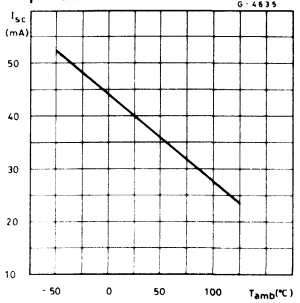


Fig. 4 - Open loop frequency reponse

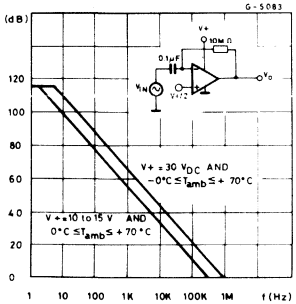


Fig. 5 - Large signal frequency response

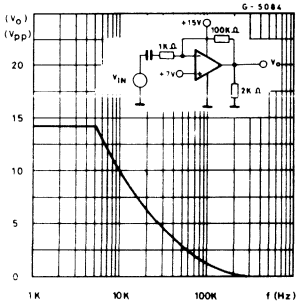


Fig. 6 - Voltage follower pulse response (small signal)

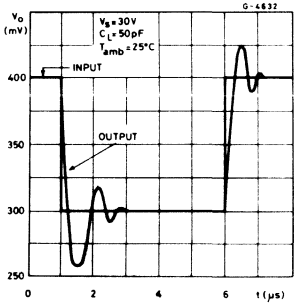


Fig. 7 - Input current

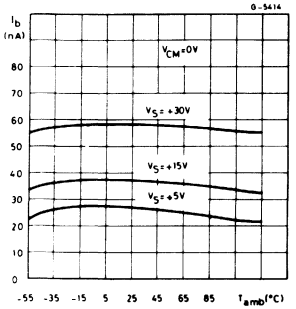


Fig. 8 - Output characteristics vs. current sourcing

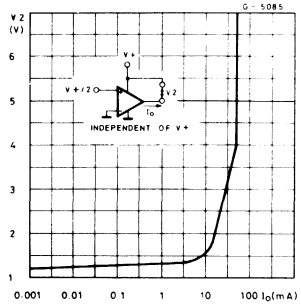
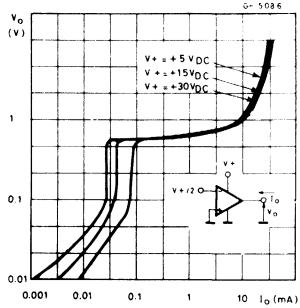


Fig. 9 - Output characteristics vs. current sinking



APPLICATION INFORMATION

The LM124 can operate with a single power supply voltage, has true-differential inputs and remains in the linear mode with an input common-mode voltage of 0V. The four included op amps work over a wide range of power supply voltage with little change in performance characteristics. At 25°C operation is possible down to a minimum supply voltage of 2.3V.

The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_s - 1.5V, but either or both inputs can go to + 32V without damage.

If the voltage at any of the input leads is driven negative ($V_{in} < -0.3V$), the collector-base junction of the input PNP transistor becomes forward biased and thereby acts as an input diode clamps (max current: 50 mA). In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This can cause the output voltage to go to the positive supply voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage gain returns positive ($V_{in} > -0.3V$). The output stage design allows the amplifiers to both source and sink large output currents.

Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

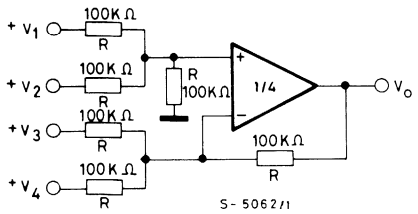
Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperature. **Putting direct short-circuits on more than one amplifier at a time, the total IC power dissipation will increase to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers.**

The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

The circuits presented in the following section emphasize operation on a single power supply voltage. If split supplies are used, all the standard op amps configuration can be realized.

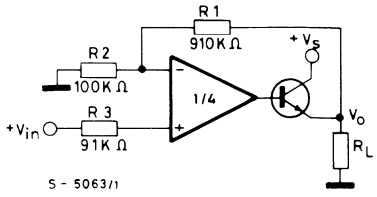
Typical single supply application circuits (V_s = 5V)

Fig. 10 - DC summing amplifier



where: $V_o = V_1 + V_2 - V_3 - V_4$
$(V_1 + V_2)' \geq (V_3 + V_4)$ to keep $V_o > 0V$

Fig. 11 - Power amplifier



V_o = 0V for V_{IN} = 0V
G_V = 20 dB

APPLICATION INFORMATION (continued)

Fig. 12 - LED driver

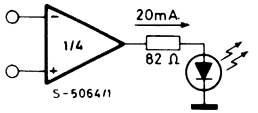


Fig. 13 - Lamp driver

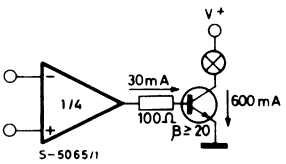
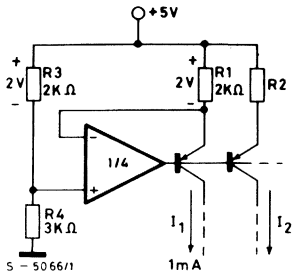
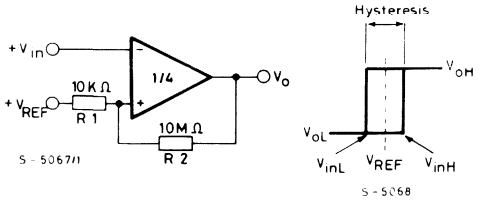


Fig. 14 - Fixed current sources



$$I_2 = \left(\frac{R1}{R2}\right) I_1$$

Fig. 15 - Comparator with Hysteresis

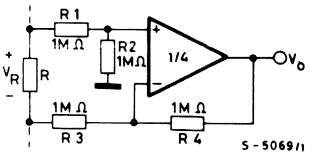


$$V_{in\,L} = \frac{R1}{R1 + R2} (V_{OL} - V_{REF}) + V_{REF}$$

$$V_{in\,H} = \frac{R1}{R1 + R2} (V_{OH} - V_{REF}) + V_{REF}$$

$$\text{Hysteresis} = \frac{R1}{R1 + R2} (V_{OH} - V_{OL})$$

Fig. 16 - Ground referencing a differential input signal



$$V_O = V_R$$

Fig. 17 - Driving TTL

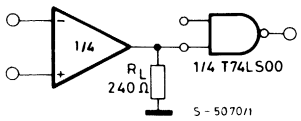
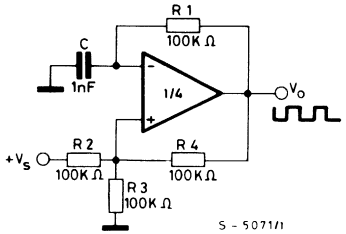
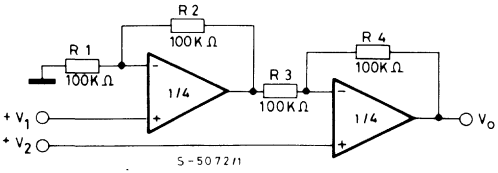


Fig. 18 - Squarewave oscillator



APPLICATION INFORMATION (continued)

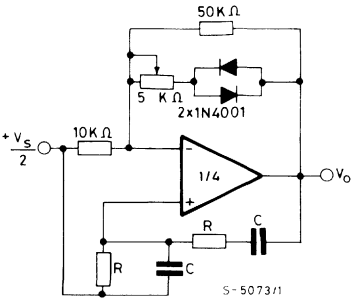
Fig. 19 - High input Z, DC differential amplifier



For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

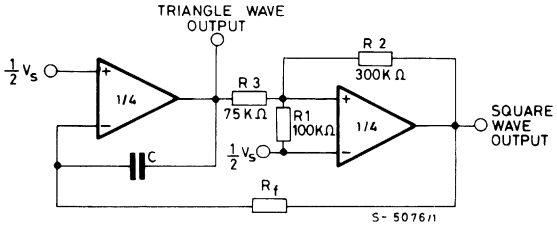
$V_O = 1 + \frac{R4}{R3} (V2 - V1)$

Fig. 20 - Wien bridge oscillator



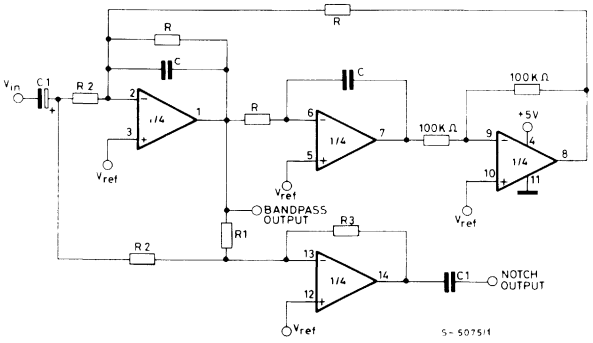
$f_o = \frac{1}{2\pi RC}$

Fig. 21 - Function generator



$f = \frac{R1 + R_C}{4 C R_f R1}$ $R3 = \frac{R2\ R1}{R2 + R1}$

Fig. 22 - Bi-Quad filter



$f_o = \frac{1}{2\pi RC}$; R1= QR; R2= $\frac{R1}{G_{BP}}$;

$V_{ref} = \frac{1}{2} V_s$; R3= G_N R2; C1= 10C

Example:

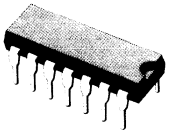
f_o = 1 KHz	R = 160 KΩ
Q = 10	C = 1 nF
G_{BP}= 1	R1= 1.6 MΩ
G_N= 1	R2= 1.6 MΩ
	R3= 1.6 MΩ

Where: G_{BP}= Center Frequency Gain
G_N = Passband Notch Gain

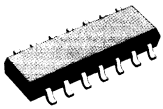
QUAD VOLTAGE COMPARATORS

- SINGLE SUPPLY OPERATION + 2V to + 36V
- DUAL SUPPLY OPERATION ± 1V to ± 18V
- COMPARE VOLTAGES AT GROUND POTENTIAL
- LOW CURRENT DRAIN (800μA TYP.)
- COMPATIBLE WITH ALL FORMS OF LOGIC
- LOW INPUT BIAS CURRENT
- LOW INPUT OFFSET CURRENT
- LOW OFFSET VOLTAGE

The devices of the LM139 series are monolithic integrated circuits in a 14-lead dual in-line plastic and ceramic package and in a 14-lead micropackage. They consists of four independent precision voltage comparators and are specially designed to offer a versatilly as high as possible; application areas include limit comparators, A/D converters, waveforms generators, high voltage logic gates and so on. Furthermore, the open collector output stage provides easy interfacing with all types of logic circuitry.

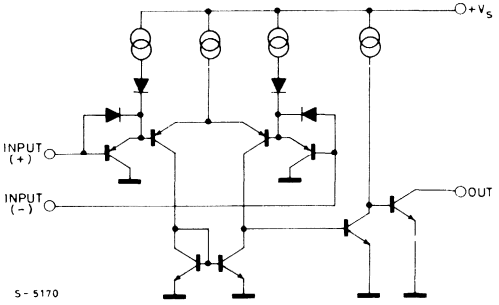


DIP-14
(Ceramic and Plastic)



SO-14

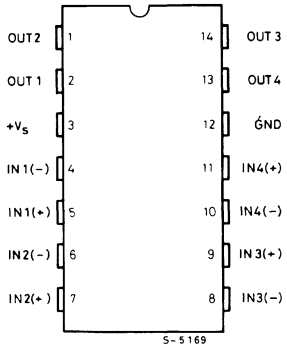
SCHEMATIC DIAGRAM
(each section)



ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 18 or + 36	V
V_i	Input voltage range	-0.3 to 36	V
V_i	Differential input voltage	36	V
I_i	Input current ($V_{in} < -0.3\ V_{dc}$)	50	mA
T_{op}	Operating temperature **LM339/339A**	0 to 70	°C
	LM239/239A	-25 to 85	°C
	LM2901	-40 to 85	°C
	LM139/139A	-55 to 125	°C
T_j	Junction temperature	150	°C
T_{stg}	Storage temperature	-65 to 150	°C

CONNECTION DIAGRAM AND ORDERING NUMBERS



Temperature range	Ceramic DIP-14	Plastic DIP-14	SO-14
Commercial 0 to 70°C	LM339J LM339AJ	LM339N LM339AN	LM339D
Industrial -25 to 85°C	LM239J LM239AJ	LM239N	LM239D
Automotive -40 to 85°C	LM2901J	LM2901N	LM2901D
Military -55 to 125°C	LM139J LM139AJ		

THERMAL DATA

			Ceramic DIP-14	SO-14	Plastic DIP-14
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	150°C/W	165°C/W	200°C/W

ELECTRICAL CHARACTERISTICS (V_s = + 5V; T_{amb} = 25°C, unless otherwise specified)

Parameter		Test conditions		LM139			LM139A			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{os}	Input offset voltage	At out. switch point V_o= 1.4V; R_g= 0			2	5		1	2	mV
		V_{REF}= 1.4V	T_{amb}=-55 to 125°C			9			4	
I_p	Input bias current (1)	Output in linear range			25	100		25	100	nA
			T_{amb} = -55 to 125°C			300			300	
I_{os}	Input offset current				3	25		3	25	nA
			T_{amb}= -55 to 125°C			100			100	
	Input Common-Mode voltage range (2)			0		V_s-1.5	0		V_s-1.5	V
			T_{amb}= -55 to 125°C	0		V_s-2	0		V_s-2	
I_s	Supply current	R_L= ∞			0.8	2		0.8	2	mA
G_V	Voltage gain	R_L ⩾ 15KΩ, V_s = 15V			106		94	106		dB
	Large signal response time	V_{IN}= TTL logic swing; V_{REF}= + 1.4V; R_L = 5.1KΩ V_{RL}= 5V			300			300		ns
T_r	Response time (3)	V_{RL}= 5V	R_L = 5.1V		1.3			1.3		μs
I_o	Output sink current	$V_{IN(-)}$ ⩾ 1V; $V_{IN(+)}$ = 0V V_o ⩽ 1.5V		6	16		6	16		mA
V_{sat}	Output saturation	$V_{IN(-)}$ ⩾ 1V $V_{IN(+)}$ = 0V I_{sink} ⩽ 4mA			250	400		250	400	mV
			T_{amb}= -55 to 125°C			700			700	
$I_{o\ leak}$	Output leakage	$V_{IN(+)}$ ⩾ 1V $V_{IN(-)}$ = 0V	V_o = 5V		0.1			0.1		nA
			T_{amb}= -55 to 125°C V_o= 30V			1			1	μA
V_{ID}	Differantial input voltage	All V_{IN} ⩾ 0V (or − V_s if split supply is used); T_{amb}= -55 to 125°C				+V_s			+V_s	V

Notes: (1) The direction of the current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

(2) If either input of any comparators goes more negative than 0.3V bellow ground, a parasitic transistor turns on causing high input current and possible faulty output. This conditions is not destructive providing the input current is limited to less than 50mA

(3) The response time specified is for a 100mV input step with 5mV overdrive. For larger overdrive signals 300 nsec can be obtained.

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions		LM239/339			LM239A/339A			LM2901			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{os}	Input offset voltage	At out. switch point $V_o \cong 1.4V$; $R_g = 0$			2	5		1	2		2	7	mV
		$V_{REF} = 1.4V$	T_{amb}=full range			9			4		9	15	
I_b	Input bias current (1)	Output in linear range			25	250		25	250		25	250	nA
			T_{amb}=full range			400			400		200	500	
I_{os}	Input offset current				5	50		5	50		5	50	nA
			T_{amb}=full range			150			150		50	200	
	Input Common-Mode voltage range (2)			0		V_s-1.5	0		V_s-1.5	0		V_s-1.5	V
			T_{amb}= full range	0		V_s-2	0		V_s-2	0		V_s-2	
I_s	Supply current	$R_L = \infty$			0.8	2		0.8	2		0.8	2	mA
I_s	Supply current	$V_s = 30V$ $R_L = \infty$										2.5	mA
G_V	Voltage gain	$R_L \geqslant 15 K\Omega$, $V_s = 15V$			106		94	106		88	100		dB
	Large signal response time	V_{IN} = TTL logic swing; $V_{REF} = +1.4V$; $R_L = 5.1K\Omega$ $V_{RL} = 5V$			300			300			300		ns
T_r	Response time (3)	$V_{RL} = 5V$;	$R_L = 5.1V$		1.3			1.3			1.3		μs
I_o	Output sink current	$V_{IN(-)} \geqslant 1V$; $V_o \leqslant 1.5V$	$V_{IN(+)} = 0V$;	6	16		6	16		6	16		mA
V_{sat}	Output saturation	$V_{IN(-)} \geqslant 1V$ $V_{IN(+)} = 0V$ $I_{sink} \leqslant 4mA$			250	400		250	400			400	mV
			T_{amb}= full range			700			700			700	
$I_{o\ leak}$	Output leakage	$V_{IN(+)} \geqslant 1V$ $V_{IN(-)} = 0V$	$V_o = 5V$		0.1			0.1			0.1		nA
			T_{amb}= full range $V_o = 30V$			1			1			1	μA
V_{ID}	Differential input voltage	All $V_{IN} \geqslant 0V$ (or $-V_s$ if split supply is used);	T_{amb}= full range			$\pm V_s$			$+V_s$			$+V_s$	V

LM339/339A T_{op} = 0 to 70°C

LM239/239A T_{op} = 25 to 85°C

Notes: (1) The direction of the current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading change exists on the reference or input lines.

(2) If either input of any comparators goes more negative than 0.3V below ground, a parasitic transistor turns on causing high input current and possible faulty outputs. This conditions is not destructive providing the input current is limited to less than 50mA.

(3) The response time specified is for a 100mV input step with 5mV overdrive. For larger overdrive signals 300 nsec can be obtained.

TYPICAL CHARACTERISTICS (LM339 – LM339A)

Fig. 1 - Supply current vs. supply voltage

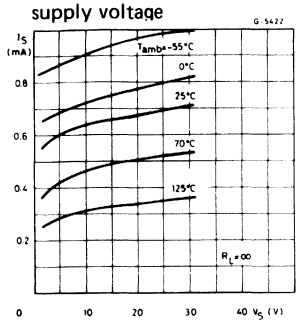


Fig. 2 - Input current vs. supply voltage

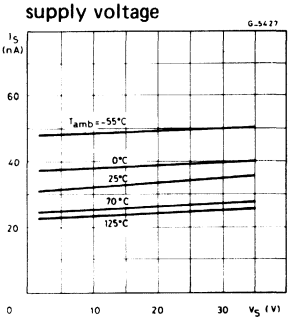


Fig. 3 - Output saturation voltage

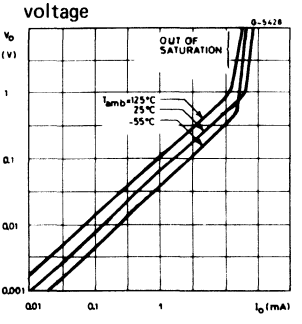


Fig. 4 - Response time

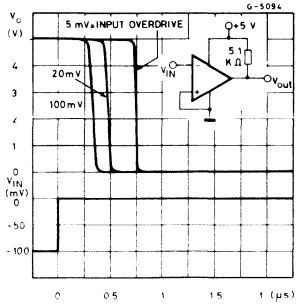
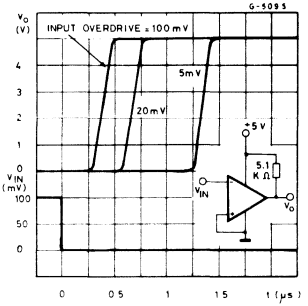


Fig. 5 - Response time



TYPICAL CHARACTERISTICS (LM2901)

Fig. 6 - Supply current vs. supply voltage

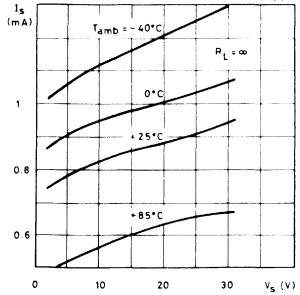


Fig. 7 - Input current vs. supply voltage

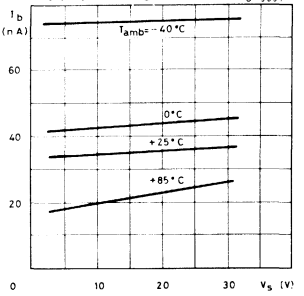
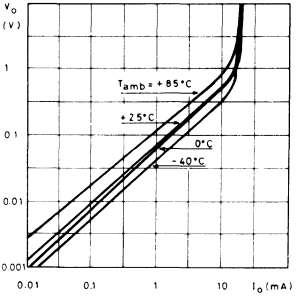


Fig. 8 - Output saturation voltage



APPLICATION INFORMATION

The LM139 series includes four high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output is inadvertently allowed to capacitively couple to the inputs via stray capacitance.

That occurs during the output voltage transitions, when the comparator changes state.

To minimize this problem, PC board layout should be designed to reduce stray input-output coupling; reducing the input resistors to less than 10KΩ reduces the feedback signal levels and finally, adding even a small amount (1 to 10mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible.

It is good design practice to ground all unused pins.

The differential input voltage may be larger than positive supply without damaging the device. Note that voltages more negative than -0.3V should not be used: an input clamping diode can be used as protection.

The output of the LM139 is the uncommitted collector of a NPN transistor with grounded emitter. This allows the device to be used like any open-collector gate providing the OR-wide facility.

The output sink current capability is approximately 16mA; if this limit is exceeded, the output transistor will come out of saturation and the output voltage will rise very rapidly.

Under this limit, the output saturation voltage is limited by the approximatively 60Ω r_{sat} of the output transistor.

Fig. 9 - Basic comparator

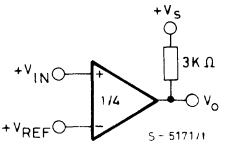


Fig.10- Non-inverting comparator with Hysteresis

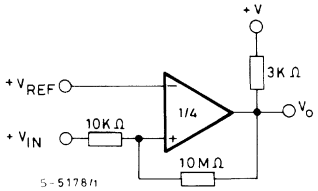


Fig.11- Inverting comparator with Hysteresis

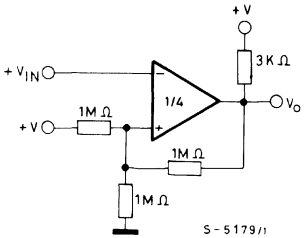


Fig.12- Driving C/MOS

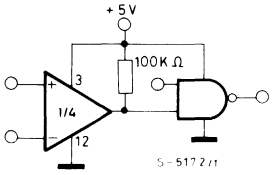
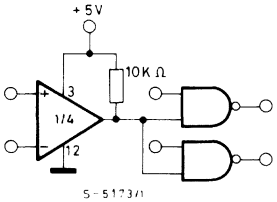


Fig.13- Driving TTL



APPLICATION INFORMATION (continued)

Fig.14- AND gate

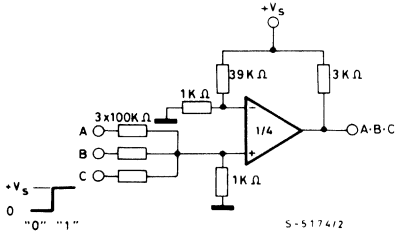


Fig.15- OR gate

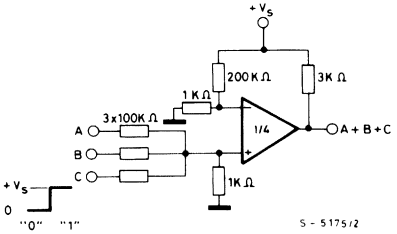


Fig.16- Large fan-in AND gate

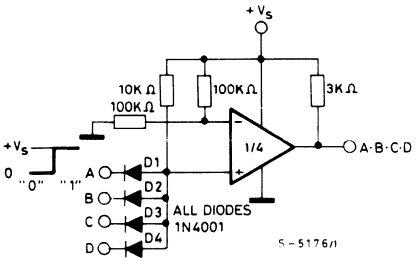


Fig.17- Squarewave oscillator

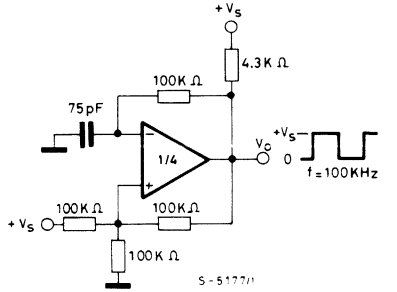


Fig. 18 - Time delay generator

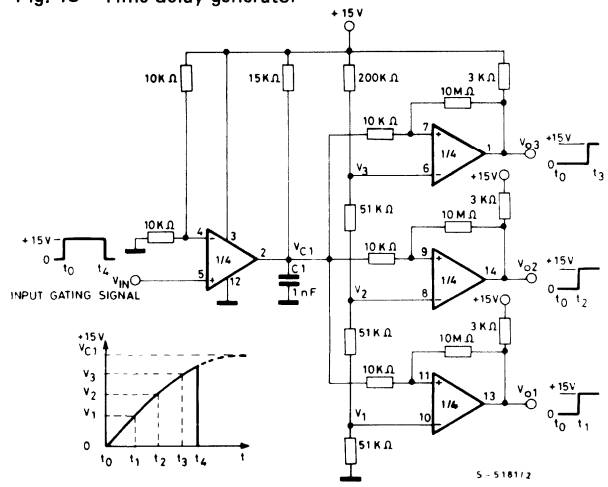
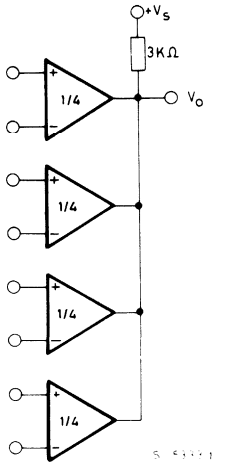


Fig. 19 - ORing the outputs



APPLICATION INFORMATION (continued)

Fig. 20 - Peak audio level display

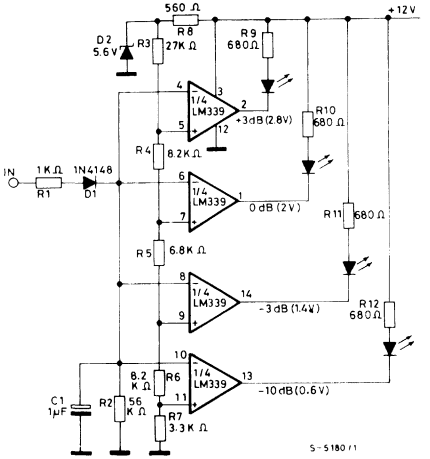


Fig. 21 - PC Board and component layout of the circuit of fig. 20

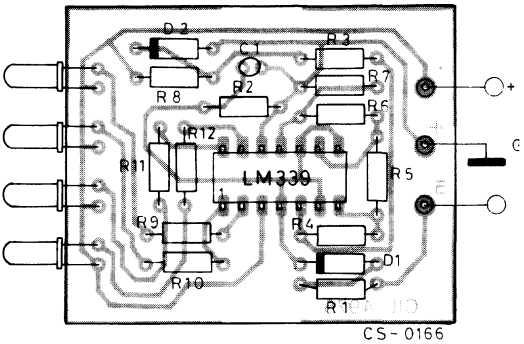
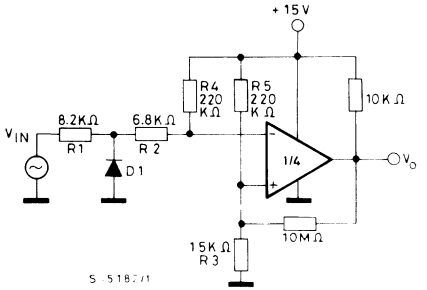


Fig. 22 - Zero crossing detector (single supply)



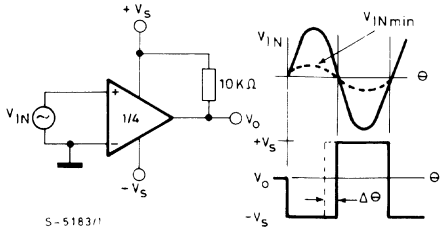
D1 prevents input from going negative by more than 0.6V:

$$R1 + R2 = R3$$

$$R3 \leqslant \frac{R5}{10} \text{ for smaller error in zero crossing}$$

Fig. 23 - Zero crossing detector (split supplies)

$V_{INmin} \approx$ 0.4V peak for 1% phase distortion ($\Delta\ \theta$)



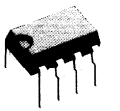
LM158
LM258
LM358
LM2904

DUAL OPERATIONAL AMPLIFIERS

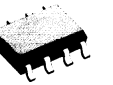
- SINGLE SUPPLY (3V to 30V) OR DUAL SUPPLIES (± 1.5V to 15V)
- VERY LOW SUPPLY CURRENT DRAIN (500μA) ESSENTIALLY INDIPENDENT OF SUPPLY VOLTAGE
- LOW INPUT BIASING CURRENT (TEMPERATURE COMPENSATED)
- LOW INPUT OFFSET VOLTAGE AND OFFSET CURRENT
- DIFFERENTIAL INPUT VOLTAGE RANGE EQUAL TO THE POWER SUPPLY VOLTAGE
- INTERNALLY FREQUENCY COMPENSATED FOR UNITY GAIN
- LARGE OUTPUT VOLTAGE SWING (3.5V WITH $V_s = 5V$)

The LM158 series consists of two independent, high gain, internally frequency compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages. Operation from dual power supplies is also possible and the low power supply current drain is independent of the supply voltage.

In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though opperated from only a single power supply voltage. The unity gain cross frequency is temperature compensated. The input bias current is also temperature compensated. The LM158 is available in minidip plastic or ceramic package and in a 8-lead micropackage version.

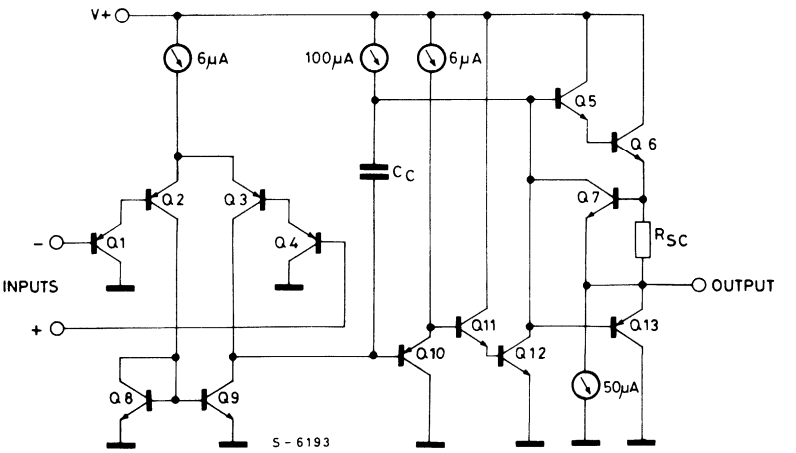


Minidip (Plastic and Ceramic)



SO-8

SCHEMATIC DIAGRAM (One section)

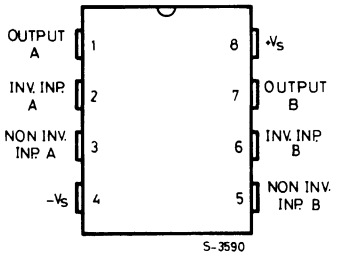


ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	32 or ± 16	V
V_s	Supply voltage: (**LM2904** only)	26 or ± 13	V
V_i	Differential input voltage	32	V
V_i	Input voltage	-0.3 to + 32	V
	Output short-circuit to GND V + < 15V and T_{amb} = 25°C	Continuous	
T_{op}	Operating temperature: **LM358/358A**	0 to 70	°C
	LM2904	-40 to 85	°C
	LM258/258A	-25 to 85	°C
	LM158/158A	-55 to 125	°C
T_j	Junction temperature	150	°C
T_{stg}	Storage temperature	-65 to 150	°C

CONNECTION DIAGRAM AND ORDERING NUMBERS

(top view)



Temperature range	Ceramic Minidip	Plastic Minidip	SO-8
Commercial 0 to 70°C	LM358J LM358AJ	LM358N LM358AN	LM358D
Industrial -25 to 85°C	LM258J LM258AJ	LM258N	LM258D
Automotive -40 to 85°C	LM2904J	LM2904N	LM2904D
Military -55 to 125°C	LM158J LM158AJ	—	—

THERMAL DATA

			Plastic Minidip	Ceramic Minidip	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max.	120°C/W	150°C/W	200°C/W

ELECTRICAL CHARACTERISTICS (V_s = + 5V, T_{amb}= -55 to 125°C for the LM158/LM158A and T_{amb} = -25 to 85°C for the LM258/LM258A, unless otherwise specified)

Parameter		Test conditions		LM158/258			LM158A			LM258A			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_S	Supply current	R_L= ∞	V_s = 30V		1	2		1	2		1	2	mA
					0.7	1.2		0.7	1.2		0.7	1.2	
I_b	Input bias current	T_{amb}= 25°C			45	150		20	50		40	80	nA
					40	300		40	100		40	100	
V_{os}	Input offset voltage	R_g= 0 V_s = 5V to 30V	T_{amb}= 25°C		2	5		1	2		1	3	mV
						7			4			4	
$\frac{\Delta V_{os}}{\Delta T}$	Input offset voltage drift	R_g= 0			7			7	20		7	20	µV/°C
I_{os}	Input offset current	T_{amb}= 25°C			3	30		2	10		2	15	nA
						100			30			30	
$\frac{\Delta I_{os}}{\Delta T}$	Input offset current drift				10			10	200		10	200	pA/°C
I_{sc}	Output short circuit to ground current	T_{amb}= 25°C (*)			40	60		40	60		40	60	mA
G_v	Large signal open loop voltage gain	V_s = 15V R_L ≥ 2 KΩ	T_{amb}= 25°C	94	100		94	100		94	100		dB
				88			88			88			
	Input common-mode voltage range	V_s = 30V	T_{amb}= 25°C	0		V_s-1.5	0		V_s-1.5	0		V_s-1.5	V
				0		V_s-2	0		V_s-2	0		V_s-2	
V_o	Output voltage swing	T_{amb}= 25°C	R_L= 2 KΩ			V_s-1.5			V_s-1.5				V
			R_L ≥ 10 KΩ									V_s-1.5	
		V_s = 30V	R_L= 2 KΩ	26			26			26			V
			R_L ≥ 10 KΩ	27	28		27	28		27	28		
$V_{o\ sat}$	Output saturation voltage to ground	R_L ≤ 10 KΩ			5	20		5	20		5	20	mV
CMR	Common mode rejection	T_{amb}= 25°C		70	85		70	85		70	85		dB
SVR	Supply voltage rejection	T_{amb}= 25°C		65	100		65	100		65	100		dB
CS	Channel separation	f = 1 KHz to 20 KHz T_{amb}= 25°C (Input referred)			120			120			120		dB
I_o^+	Output source current	V_s = 15V V_i^+ = 1V V_i^- = 0V	T_{amb}= 25°C	20	40		20	40		20	40		mA
				10	20		10	20		10	20		
I_o^-	Output sink current	V_i^+ = 0V V_i^- = 1V V_o= 200 mV	T_{amb}= 25°C	12	50		12	50		12	50		µA
		V_i^- = 1V V_i^+ = 0V V_s= 15V	T_{amb}= 25°C	10	20		10	20		10	20		mA
				5	8		10	15		5	8		

(*) Short circuits from the output to positive supply voltage can cause excessive heating and eventual destruction. The maximum output current is 40 mA typ. independent of the magnitude of V_s. Destructive dissipation can result from simultaneous shorts on all amplifiers.

ELECTRICAL CHARACTERISTICS (V_s = 5V, T_{amb} = 0 to 70°C for the **LM358/LM358A** and T_{amb} = -40 to 85°C for the LM2904, unless otherwise specified)

Parameter		Test conditions		LM358			LM358A			LM2904			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_S	Supply current	$R_L = \infty$	V_s = 30V (*)		1	2		1	2		1	2	mA
					0.5	1.2		0.5	1.2		0.5	1.2	
I_b	Input bias current	T_{amb} = 25°C			45	250		45	100		45	250	nA
						500			200			500	
V_{os}	Input offset voltage	R_g = 0 V_s = 5V to 30V (*)	T_{amb} = 25°C		2	7		2	3		2	7	mV
						9			5			10	
$\frac{\Delta V_{os}}{\Delta T}$	Input offset voltage drift	R_g = 0			7			7	30		7		µV/°C
I_{os}	Input offset current	T_{amb} = 25°C			5	50		5	30		5	50	nA
						150			75			200	
$\frac{\Delta I_{os}}{\Delta T}$	Input offset current drift				10			10	300		10		pA/°C
I_{sc}	Output short circuit to ground current	T_{amb} = 25°C (**)			40	60		40	60		40	60	mA
G_v	Large signal open loop voltage gain	V_s = 15V $R_L \geq 2$ KΩ	T_{amb} = 25°C	88	100		88	100			100		dB
				83			83			83			
	Input common-mode voltage range	V_s = 30V (*)	T_{amb} = 25°C	0		V_s-1.5	0		V_s-1.5	0		V_s-1.5	V
				0		V_s-2	0		V_s-2	0		V_s-2	
V_o	Output voltage swing	T_{amb} = 25°C	R_L = 2 KΩ			V_s-1.5			V_s-1.5				V
			$R_L \geq$ 10 KΩ									V_s-1.5	
		V_s = 30V (*)	R_L = 2 KΩ	26			26			22			V
			$R_L \geq$ 10 KΩ	27	28		27	28		23	24		
$V_{o\ sat}$	Output saturation voltage to ground	$R_L \leq$ 10 KΩ			5	20		5	20		5	100	mV
CMR	Common mode rejection	T_{amb} = 25°C		65	70		65	85		50	70		dB
SVR	Supply voltage rejection	T_{amb} = 25°C		65	70		65	100		50	70		dB
CS	Channel separation	f = 1 KHz to 20 KHz T_{amb} = 25°C (Input referred)			120			120			120		dB
I_{o+}	Output source current	V_s = 15V V_i^+ = 1V V_i^- = 0V	T_{amb} = 25°C	20	40		20	40		20	40		mA
				10	20		10	20		10	20		
I_{o-}	Output sink current	V_i^+ = 0V V_i^- = 1V V_o = 200 mV	T_{amb} = 25°C	12	50		12	50					µA
		V_i^- = 1V V_i^+ = 0V V_s = 15V	T_{amb} = 25°C	10	20		10	20		10	20		mA
				5	8		5	8		5	8		

(*) 26V for LM2904.

(**) Short circuits from the output to positive supply voltage can cause excessive heating and eventual destruction. The maximum output current is 40 mA typ. independent of the magnitude of V_s. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Fig. 1 - Supply current vs. supply voltage

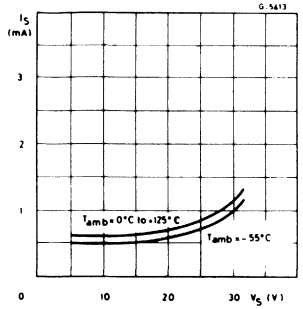


Fig. 2 - Input voltage range vs. supply voltage

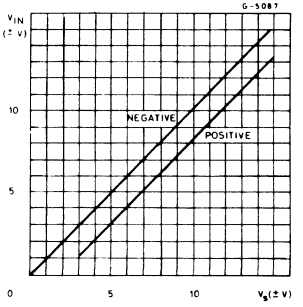


Fig. 3 - Output short circuit current vs. ambient temperature

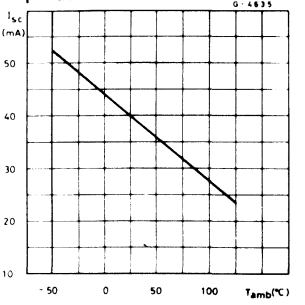


Fig. 4 - Open loop frequency reponse

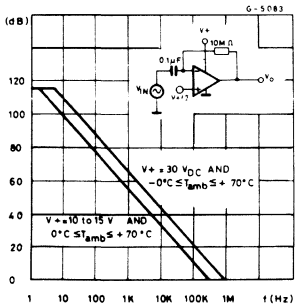


Fig. 5 - Large signal frequency response

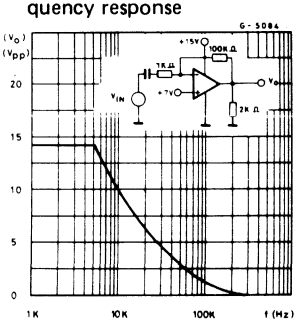


Fig. 6 - Voltage follower pulse response (small signal)

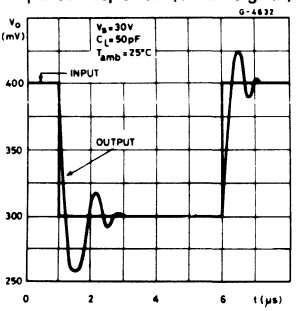


Fig. 7 - Input current

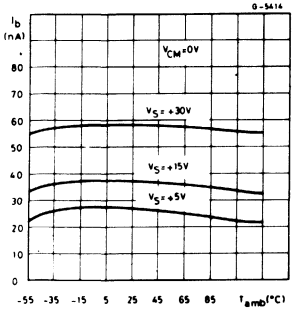


Fig. 8 - Output characteristics vs. current sourcing

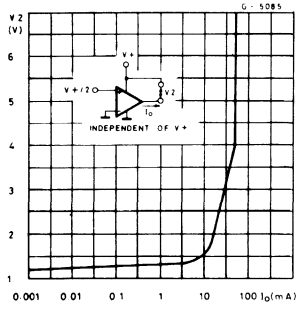
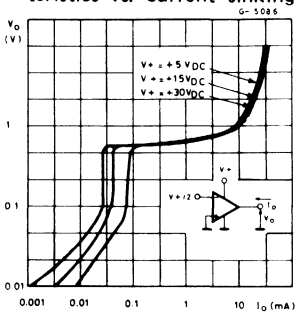


Fig. 9 - Output characteristics vs. current sinking



APPLICATION INFORMATION

The LM158 can operate with a single power supply voltage, has true-differential inputs and remains in the linear mode with an input common-mode voltage of 0V. The two included op amps work over a wide range of power supply voltage with little change in performance characteristics. At 25°C operation is possible down to a minimum supply voltage of 2.3V.

The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_s-15V, but either or both inputs can go to + 32V without damage.

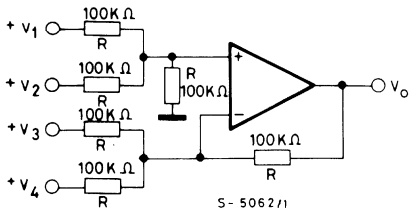
If the voltage at any of the input leads is driven negative ($V_{in} < -0.3$), the collector-base junction of the input PNP transistor becomes forward biased and thereby acts as an input diode clamps (max current: 50mA). In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This can cause the output voltage to go to the positive supply voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage again returns positive ($V_{in} > -0.3V$). The output stage design allows the amplifiers to both source and sink large output currents.

Therefore both NPN and PNP external current boost transistors can be used extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperature. **Putting direct short-circuit on more than one amplifier at a time, the total IC power dissipation will increase to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers.** The larger value of output source current which a available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

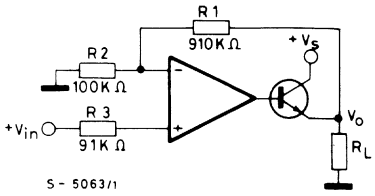
Typical single supply application circuits (V_s = 5V)

Fig. 10 - DC summing amplifier



where: $V_o = V_1 + V_2 - V_3 - V_4$
$(V_1 + V_2)' \geq (V_3 + V_4)$ to keep $V_o > 0V$

Fig. 11 - Power amplifier



V_o= 0V for V_{IN}= 0V
G_V= 20 dB

APPLICATION INFORMATION (continued)

Fig. 12 - LED driver

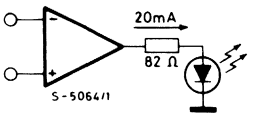


Fig. 13 - Lamp driver

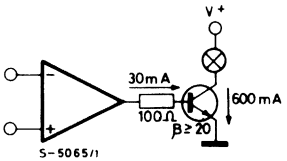
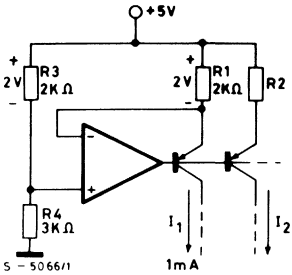
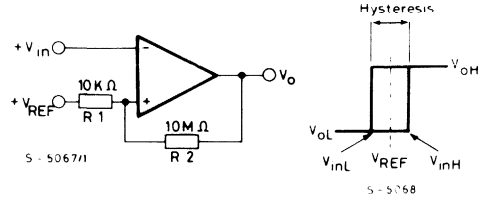


Fig. 14 - Fixed current sources



$$I_2 = \left(\frac{R1}{R2}\right) I_1$$

Fig. 15 - Comparator with Hysteresis

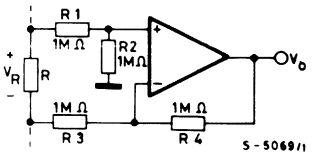


$$V_{in\,L} = \frac{R1}{R1 + R2}(V_{OL} - V_{REF}) + V_{REF}$$

$$V_{in\,H} = \frac{R1}{R1 + R2}(V_{OH} - V_{REF}) + V_{REF}$$

$$\text{Hysteresis} = \frac{R1}{R1 + R2}(V_{OH} - V_{OL})$$

Fig. 16 - Ground referencing a differential input signal



$$V_O = V_R$$

Fig. 17 - Driving TTL

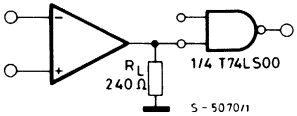
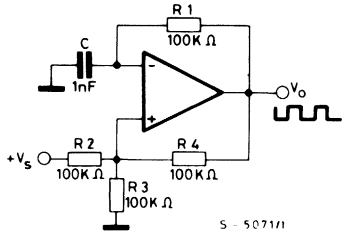
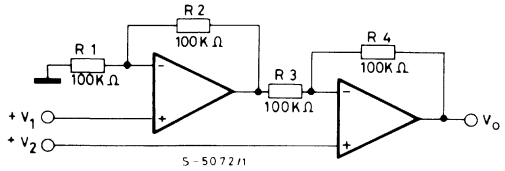


Fig. 18 - Squarewave oscillator



APPLICATION INFORMATION (continued

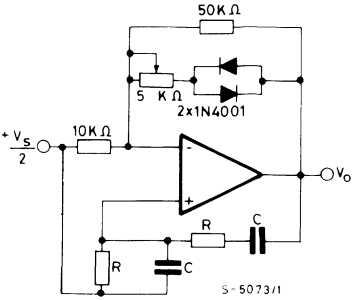
Fig. 19 - High input Z, DC differential amplifier



For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

$V_O = 1 + \frac{R4}{R3} (V2 - V1)$

Fig. 20 - Wien bridge oscillator



$f_o = \frac{1}{2 \pi RC}$

Fig. 21 - Full wave rectifier

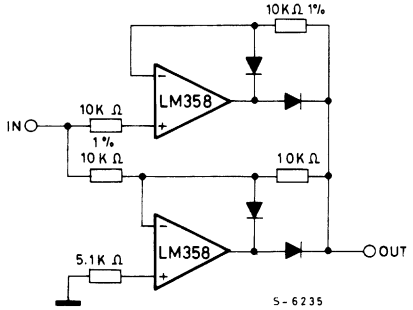


Fig. 22 - Half wave rectifier

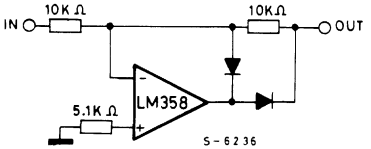
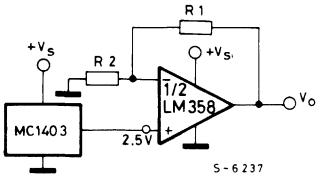
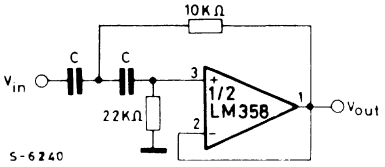


Fig. 23 - Voltage reference



$V_o = 2.5\ V\ (1 + \frac{R1}{R2})$

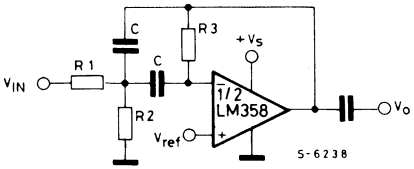
Fig. 24 - High-pass filter



$f_c = 100\ Hz$ with $C = 0.1\ \mu F$

APPLICATION INFORMATION (continued)

Fig. 25 - Multiple feedback bandpass filter



Given f_o = Center Frequency
$A(f_o)$ = Gain at Center Frequency

Choose Value f_o, C
Then:

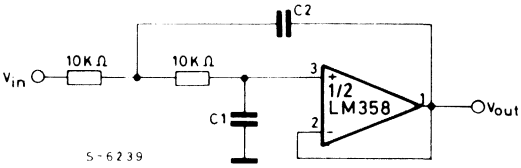
$$R3 = \frac{Q}{\pi f_o C} \; ; \; R1 = \frac{R3}{2A(f_o)} \; ; \; R2 = \frac{R1\,R3}{4Q^2\,R1 - R3}$$

For less than 10% error from operational amplifier

$\frac{Q_o f_o}{BW} < 0.1$ Where f_o and BW are expressed in Hz.

If source impedance varies, filter may be preceeded with voltage follower buffer to stabilize filter parameters.

Fig. 26 - Low-pass filter

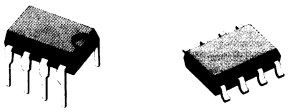


f_c = 3KHz with C1 = 3.9 nF
and C2 = 6.8 nF.

DUAL VOLTAGE COMPARATORS

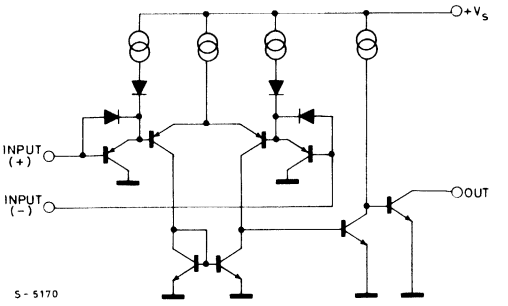
- SINGLE SUPPLY OPERATION + 2V to + 36V
- DUAL SUPPLY OPERATION ± 1V to ± 18V
- COMPARE VOLTAGES AT GROUND POTENTIAL
- LOW CURRENT DRAIN (400μA TYP)
- COMPATIBLE WITH ALL FORMS OF LOGIC
- LOW INPUT BIAS CURRENT
- LOW INPUT OFFSET CURRENT
- LOW OFFSET VOLTAGE

The devices of the LM193 series are monolithic integrated circuits in plastic or ceramic Minidip package and in 8-lead micropackage. They consists of two independent precision voltage comparators and are specially designed to offer a versatility as high as possible; application areas include limit comparators, A/D converters, waveforms generators, high voltage logic gates and so on. Furthermore, the open collector output stage provides easy interfacing with all types of logic circuitry.



Minidip (Plastic and Ceramic) **SO-8**

SCHEMATIC DIAGRAM (each section)

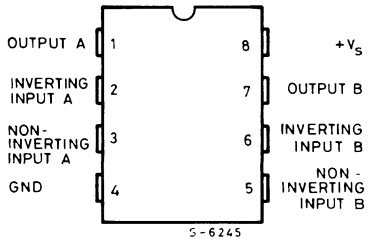


ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 18 or + 36	V
V_i	Input voltage range	-0.3 to 36	V
V_i	Differential input voltage	36	V
V_i	Input current ($V_{in} < -0.3\ V_{dc}$)	50	mA
T_{op}	Operating temperature **LM393/393A**	0 to 70	°C
	LM293/293A	-25 to 85	°C
	LM2903	-40 to 85	°C
	LM193/193A	-55 to 125	°C
T_j	Junction temperature	150	°C
T_{stg}	Storage temperature	-65 to 150	°C

CONNECTION DIAGRAM AND ORDERING NUMBERS

(top view)



Temperature range	Ceramic Minidip	Plastic Minidip	SO-8
Commercial 0 to 70°C	LM393J LM393AJ	LM393N LM393AN	LM393D
Industrial -25 to 85°C	LM293J LM293AJ	LM293N	LM293D
Automotive -40 to 85°C	LM2903J	LM2903N	LM2903D
Military -55 to 125°C	LM193J LM193AJ		

THERMAL DATA

			Plastic Minidip	Ceramic Minidip	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	120°C/W	150°C/W	200°C/W

ELECTRICAL CHARACTERISTICS (V_s = + 5V; T_{amb} = 25°C, unless otherwise specified)

Parameter		Test conditions		LM193			LM193A			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{os}	Input offset voltage	At out. switch point $V_o \cong 1.4V$; $R_g = 0$			2	5		1	2	mV
		V_{REF} = 1.4V	T_{amb}=-55 to 125°C			9			9	
I_b	Input bias current (1)	Output in linear range			25	100		25	100	nA
			T_{amb}=-55 to 125°C			300			300	
I_{os}	Input offset current				3	25		3	25	nA
			T_{amb}=-55 to 125°C			100			100	
	Input Common Mode voltage range (2)			0		V_s-1.5	0		V_s-1.5	V
			T_{amb}=-55 to 125°C	0		V_s-2	0		V_s-2	
I_s	Supply current	$R_L = \infty$			0.4	1		0.4	1	mA
G_V	Voltage gain	$R_L \geq 15K\Omega$; V_s= 15V			106		94	106		dB
	Large signal response time	V_{IN} = TTL logic swing; V_{REF} = 1.4V; R_L = 5.1KΩ V_{RL} = 5V			300			300		ns
T_r	Response time (3)	V_{RL}= 5V R_L = 5.1V			1.3			1.3		μs
I_o	Output sink current	$V_{IN(-)} \geq 1V$; $V_{IN(+)} = 0V$; $V_o \leq 1.5V$		6	16		6	16		mA
V_{sat}	Output saturation	$V_{IN(-)} \leq 1V$ $V_{IN(+)} = 0V$ $I_{sink} \geq 4mA$			250	400		250	400	mV
			T_{amb}=-55 to 125°C			700			700	
$I_{o\ leak}$	Output leakage	$V_{IN(+)} \geq 1V$ $V_{IN(-)} = 0V$	V_o = 5V		0.1			0.1		nA
			T_{amb}=-55 to 125°C V_o = 30V			1			1	μA
V_{ID}	Differential input voltage	All $V_{IN} \geq 0V$ for $-V_s$ if split supply is used; T_{amb}=-55 to 125°C				$+V_s$			$+V_s$	V

Notes:

(1) The direction of the current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading change exists on the reference or input lines.

(2) If either input of any comparators goes more negative than 0.3V below ground, a parasitic transistor turns on causing high input current and possible faulty outputs. This conditions is not destructive providing the input current and possible faulty outputs. This conditions is not desctructive providing the input current is limited to less than 50mA.

(3) The response time specified is for a 100mV input step with 5mV overdrive. For larger overdrive signals 300 nsec can be obtained.

ELECTRICAL CHARACTERISTICS (V_s = + 5V; T_{amb} = 25°C, unless otherwise specified)

Parameter		Test conditions		LM293/393			LM293A/393A			LM2903			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{os}	Input offset voltage	At out. switch point $V_o \cong 1.4V$; $R_g = 0$			2	5		1	2		2	7	mV
		$V_{REF} = 1.4V$	T_{amb}= full range			9			4		9	15	
I_b	Input bias current (1)	Output in linear range			25	250		25	250		25	250	nA
			T_{amb}= full range			400			400		200	500	
I_{os}	Input offset current				5	50		5	50		5	50	nA
			T_{amb}= full range			150			150		50	200	
	Input Common-Mode voltage range (2)			0		V_s-1.5	0		V_s-1.5	0		V_s-1.5	V
			T_{amb}= full range	0		V_s-2	0		V_s-2	0		V_s-2	
I_s	Supply current	$R_L = \infty$			0.8	2		0.8	2		0.8	2	mA
I_s	Supply current	V_s = 30V $R_L = \infty$										2.5	mA
G_v	Voltage gain	$R_L \geq$ 15 KΩ, V_s = 15V			106		94	106		88	100		dB
	Large signal response time	V_{IN} = TTL logic swing; V_{REF} = +1.4V; R_L = 5.1KΩ V_{RL} = 5V			300			300			300		ns
T_r	Response time (3)	V_{RL} = 5V;	R_L = 5.1V		1.3			1.3			1.5		μs
I_o	Output sink current	$V_{IN(-)} \geq$ 1V; $V_{IN(+)}$ = 0V; $V_o \leq$ 1.5V		6	16		6	16		6	16		mA
V_{sat}	Output saturation	$V_{IN(-)} \geq$ 1V $V_{IN(+)}$ = 0V $I_{sink} \leq$ 4mA			250	400		250	400			400	mV
			T_{amb}= full range			700			700			700	
$I_{o\ leak}$	Output leakage	$V_{IN(+)} \geq$ 1V $V_{IN(-)}$ = 0V	V_o = 5V		0.1			0.1			0.1		nA
			T_{amb}= full range V_o = 30V			1			1			1	μA
V_{ID}	Differential input voltage	All $V_{IN} \geq$ 0V (or $-V_s$ if split supply is used);	T_{amb}= full range			$+V_s$			$+V_s$			$+V_s$	V

LM393/393A T_{op} = 0 to 70°C

LM293/293A T_{op} = -25 to 85°C

Notes: (1) The direction of the current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading change exists on the reference or input lines.

(2) If either input of any comparators goes more negative than 0.3V below ground, a parasitic transistor turns on causing high input current and possible faulty outputs. This conditions is not destructive providing the input current is limited to less than 50mA.

(3) The response time specified is for a 100mV input step with 5mV overdrive. For larger overdrive signals 300 nsec can be obtained.

APPLICATION INFORMATION

The LM193 includes two high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output is inadvertently allowed to capacitively couple to the inputs via stray capacitance. That occurs during the output voltage transitions, when the comparator changes state.

To minimize this problem, PC board layout should be designed to reduce stray input-output coupling; reducing the input resistors to less than 10KΩ reduces the feedback signal levels and finally, adding even a small amount (1 to 10mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible.
It is good design practice to ground all unused pins.

The differential input voltage may be larger than positive supply without damaging the device. Note that voltages more negative than -0.3V should not be used: an input clamping diode can be used as protection.

The output of the LM193 is the uncommitted collector of a NPN transistor with grounded emitter. This allows the device to be used like any open-collector gate providing the OR-wide facility.
The output sink current capability is approsimately 16mA; if this limit is exceeded, the output transistor will come out of saturation and the output voltage will rise very rapidly.
Under this limit, the output saturation voltage is limited by the approximatively 60Ω r_{sat} of the output transistor.

Fig. 1 - Basic comparator

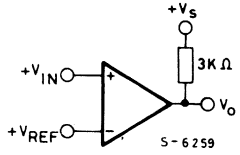


Fig. 2 - Non-inverting comparator with Hysteresis

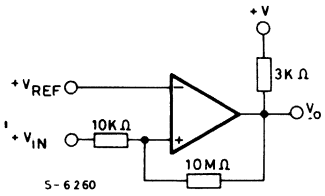


Fig. 3 - Inverting comparator with Hysteresis

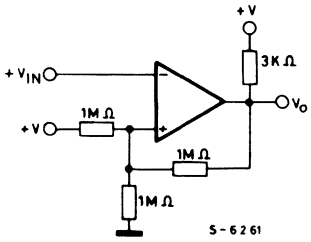


Fig. 4 - Driving C/MOS

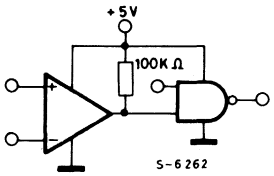
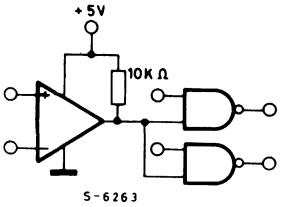


Fig. 5 - Driving TTL



APPLICATION INFORMATION (continued)

Fig. 6 - AND gate

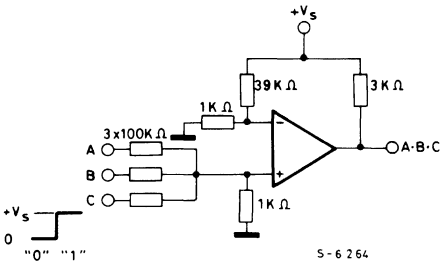


Fig. 7 - OR gate

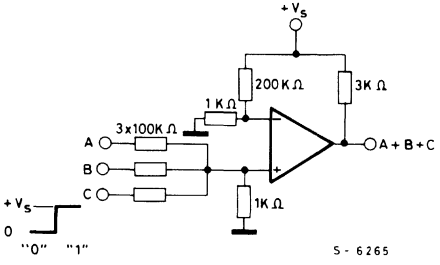


Fig. 8 - Large fan-in AND gate

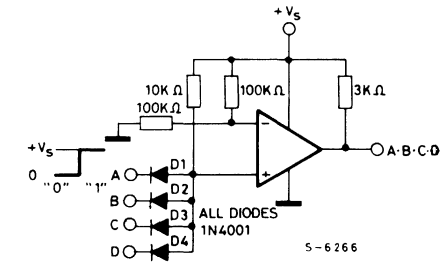


Fig. 9 - Squarewave oscillator

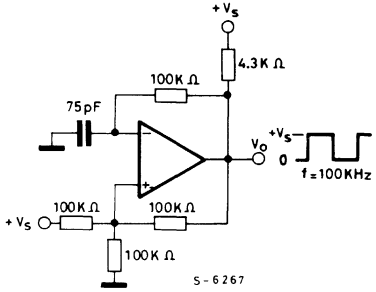


Fig. 10 - Pulse generator

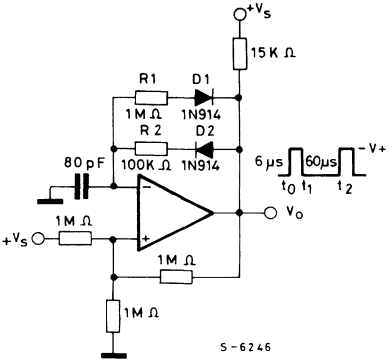
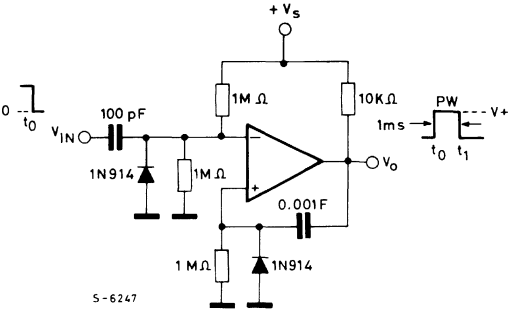


Fig. 11 - One-shot multivibrator



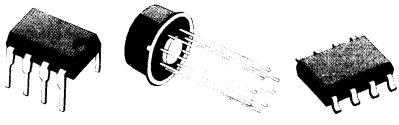
LM311

VOLTAGE COMPARATOR

- OPERATES FROM SINGLE 5V SUPPLY
- MAXIMUM INPUT CURRENT: 250nA
- MAXIMUM OFFSET CURRENT: 50nA
- DIFFERENTIAL INPUT VOLTAGE RANGE: ± 30V
- POWER CONSUMPTION: 135mW AT ± 15V

The LM311 is a voltage comparator that has input currents more than a hundred times lower than devices like the LM306 or LM710C. It is also designed to operate over a wider range of supply voltages: from standard ± 15V op amp supplies down to the single 5V supply used for IC logic. Its output is compatible with DTL and TTL as well as MOS circuits. Further, it can drive lamps or relays, switching voltages up to 40V at currents a high as 50mA.

Both the input and the output of the LM311 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM306 and LM710C (200ns response time vs 40ns) the device is also much less prone to spurious oscillations.



Minidip **TO-99** **SO-8**
(Plastic and Ceramic)

ORDERING NUMBERS: LM311H (TO-99)
LM311N (Plastic Minidip)
LM311J (Ceramic Minidip)
LM311D (SO-8)

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	36	V
	Output negative supply voltage (V_7 - V_4)	40	V
	Ground to negative supply voltage (V_1 - V_4)	30	V
	Differential input voltage	± 30	V
V_i	Input voltage (note1)	± 15	V
T_{op}	Operating temperature range	0 to 70	°C
T_{stg}	Storage temperature range	-65 to 150	°C
T_j	Junction temperature	150	°C
	Voltage at strobe pin	V+ -5	V

TYPICAL APPLICATION (Pin connections are for TO-99 package)

Fig. 1 - Detector for magnetic transducer

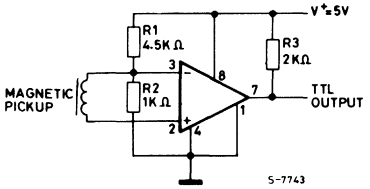
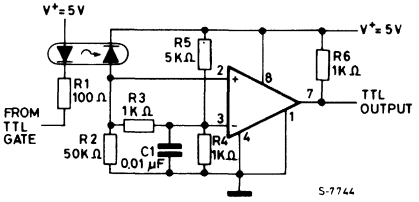
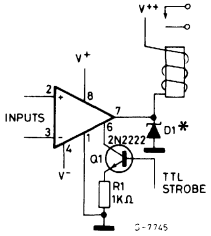


Fig. 2 - Digital transmission isolator



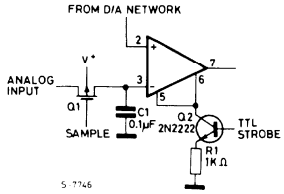
TYPICAL APPLICATION (continued)

Fig. 3 - Relay driver with strobe



* Absorbs inductive kickback of relay and protects IC from severe voltage transients on V^{++} line

Fig. 4 - Strobing off both input and output stages

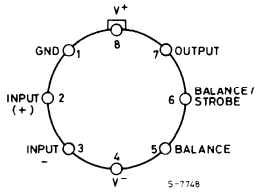


* Typical input current is 50pA with inputs strobed off

Note: Do not ground strobe pin

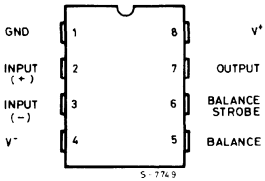
CONNECTION DIAGRAMS

TO-99

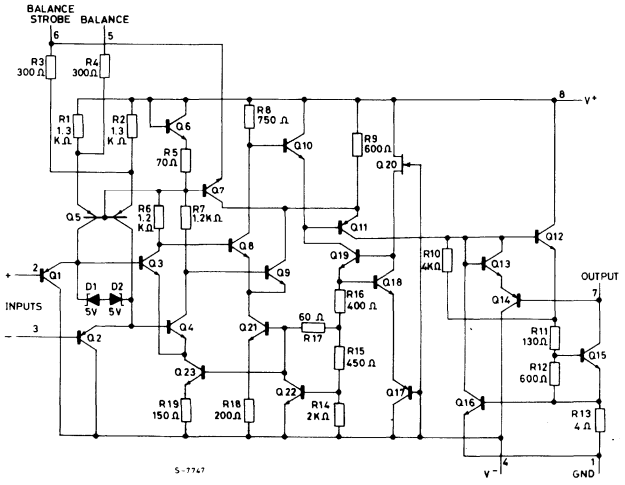


SO-8

Minidip
(Plastic and Ceramic)



SCHEMATIC DIAGRAM (Pin connections are for TO-99 package)



THERMAL DATA

			Plastic Minidip	Ceramic Minidip and TO-99	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	120°C/W	150°C/W	200°C/W

ELECTRICAL CHARACTERISTICS (Note 3)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{OS}	Input Offset Voltage (Note 4)	T_{amb} = 25°C $R_S \leq 50k\Omega$		2.0	7.5	mV
I_{OS}	Input Offset Current (Note 4)	T_{amb} = 25°C		6.0	50	nA
I_b	Input Bia Current	T_{amb} = 25°C		100	250	nA
G_V	Voltage Gain	T_{amb} = 25°C	40	200		V/mV
	Response Time (Note 5)	T_{amb} = 25°C		200		ns
V_{SAT}	Saturation Voltage	$V_{IN} \leq -10mV$ I_{OUT} = 50mA		0.75	1.5	V
I_{SON}	Strobe ON Current	T_{amb} = 25°C		3.0		mA
	Output Leakage Current	$V_{IN} \geq 10mV$ V_{OUT} = 35V T_{amb} = 25°C I_{STROBE} = 3mA		0.2	50	nA
V_{OS}	Input Offset Voltage (Note 4)	$R_S \leq 50k\Omega$			10	mV
I_{OS}	Input Offset Current (Note 4)				70	nA
I_D	Input Bias Current				300	nA
	Input Voltage Range		-14.5	13.8.-14.7	13.0	V
V_{SAT}	Saturation Voltage	$V_i^+ \geq 4.5$ $V^- = 0$ $V_{IN} \leq -10mV$ $I_{SINK} \leq 8mA$		0.23	0.4	V
I_S	Positive Supply Current	T_{amb} = 25°C		5.1	7.5	mA
	Negative Supply Current	T_{amb} = 25°C		4.1	5.0	mA

Note1: This rating applies for ± 15V supplies. The positive input voltage limit is 30V supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LM311 is 110°C. For operating at elevated temperatures, devices in the TO-99 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the Minidip package is 120°C/W, junction to ambient.

Note 3: These specifications apply for V_S = ± 15V and the Ground pin at ground, and 0°C < T_{amb} < 70°C unless otherwise specified. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ± 15V supplies.

Note 4. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

Note 5. The response time specified (see definitions) is for a 100mV overdrive.

Note 6: Do not short the strobe pin to ground; it is should be current driven at 3 to 5mA.

AUXILIARY CIRCUITS (Pin connections are of the TO-99 package)

Fig. 5 - Offset balancing

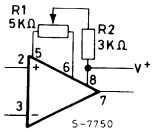
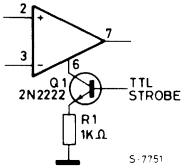
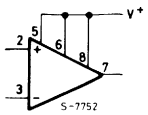


Fig. 6 - Strobing



Note: Do not ground strobe pin.

Fig. 7 - Increasing input stage current *



* Increases typical common mode slew from 7V/μs to 18μs.

Fig. 8 - Input characteristics

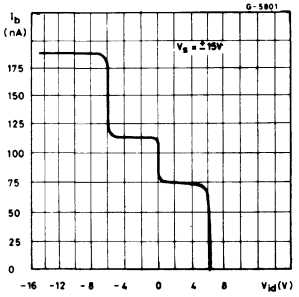


Fig. 9 - Offset error

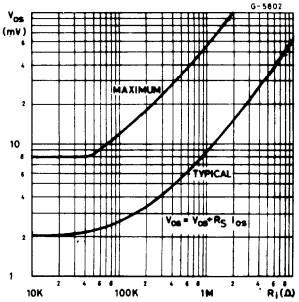


Fig. 10 - Response time for various input overdrives

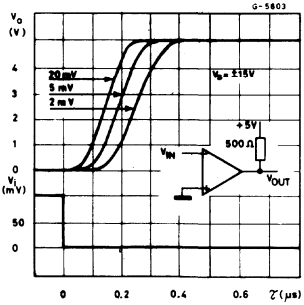


Fig. 11 - Response time for various input overdrives

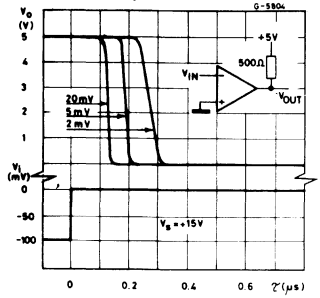


Fig. 12 - Response time for various input overdrives

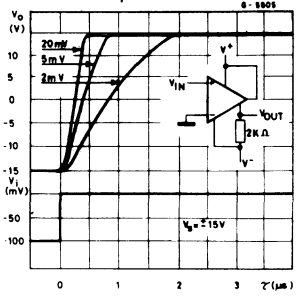


Fig. 13 - Response time for various input overdrives

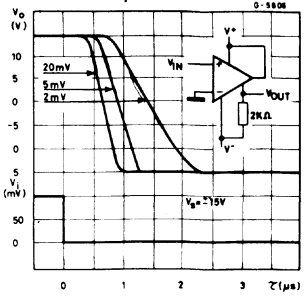


Fig. 14 - Output limiting characteristics

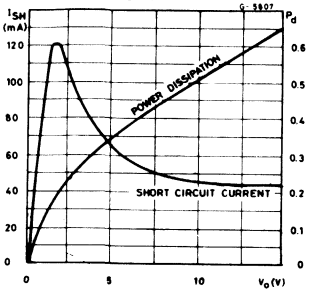


Fig. 15 - Supply current

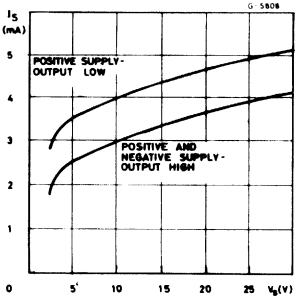
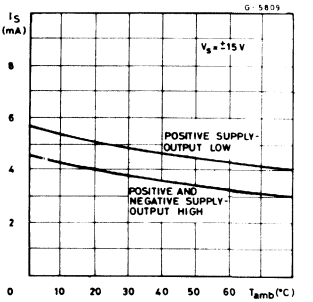


Fig. 16 - Supply current



APPLICATION INFORMATION

Fig. 17 - Zero crossing detector driving MOS logic

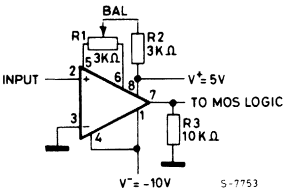
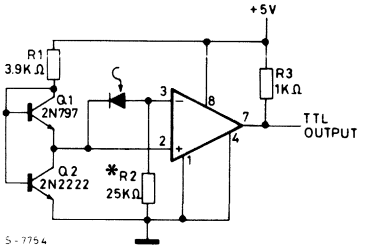


Fig. 18 - Precision photodiode comparator



* R2 sats the comparison level. At comparison, the photodiode has less than 5mV across it, decreasing leakages by an order of magnitude

Fig. 19 - Zero crossing detector driving MOS switch

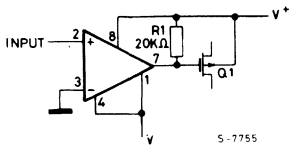
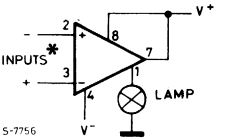
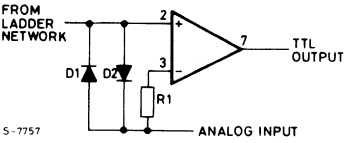


Fig. 20 - Driving ground referred load



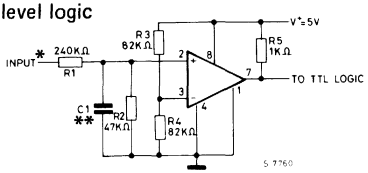
* Input polarity is reversed when using pin 1 as output

Fig. 21 - Using clamp diodes to improve response



APPLICATION INFORMATION (continued)

Fig. 22 - TTL interface with high level logic



* Values shown are for a 0 to 30V logic swing and a 15V threshold

Note: may be added to control speed and reduce susceptibility to noise spikes

Fig. 23 - Crystall oscillator

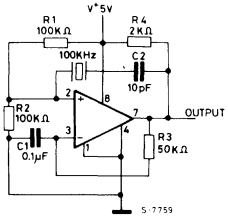
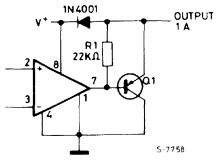


Fig. 24 - Comparator and solenoid driver



Circuit Techniques for Avoiding Oscillations

When a high-speed comparator such as the LM311. is used with fast input signals and low source impedances, the output response will normally be fast and stable, assuming that the power supplies have been bypassed (with 0.1μF disc capacitors), and that the output signal is routed well away from the inputs (pins 2 and 3) and also away from pins 5 and 6.

However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high (1kΩ to 100kΩ), the comparator may burst into oscillation near the crossing-point. This is due to the high gain and wide bandwidth of comparators like the LM311. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in Figure 25 below.

1. The trim pins (pins 5 and 6) act at unwanted auxiliary inputs. If these pins are not connected to a trimpot, they should be shored together. If they are connected to a trim-pot, a 0.01μA capacitor C1 between pins 5 and 6 will minimize the susceptibility to AC coupling. A smaller capacitor is used if pin 5 is used for positive feedback as in Figure 25.

2. Certain sources will produce a cleaner comparator output waveform if a 100pF to 1000pF capacitor C2 is connected directly across the input pins.

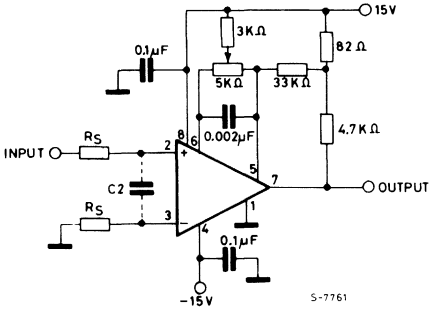
3. When the signal source is applied through a resistive network, R_s, it is usually advantageous to choose an R_s of substantially the same value, both for DC and for dynamic (AC) considerations. Carbon, tin-oxide and metal-film resistors have all been used successfully in comparator input circuitry. Inductive wire-wound resistors are not suitable.

4. When comparator circuits use input resistors (eg. summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words there should be very little lead length or printed-circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if R_s = 10kM, as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to damp. Twisting these input leads tightly is the only (second best) alternative to placing resistors close to the comparator.

5. Since feedback to almost any pin of a comparator can result in oscillation, the printed-circuit layout should be engineered thoughtfully. Preferably there should be a groundplane under the LM311 circuitry, for example, one side of a double-layer circuit card. Ground foil (or, positive supply or negative supply foil) should extend between the output and the inputs, to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should be essentially surrounded by ground foil on all sides, to guard against capacitive coupling from any high-level signals (such as the output). If pins 5 and 6 are not used, they should be shorted together. If they are connected to a trim-pot, the trim-pot should be located at most, a few

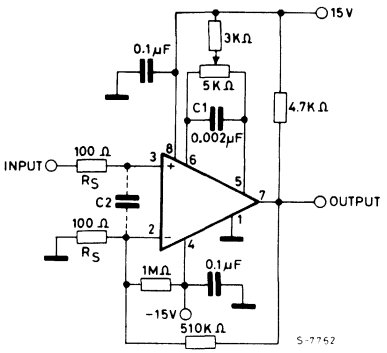
APPLICATION INFORMATION (continued)

Fig. 25 - Improved positive feedback



Pin connections shown are for LM311H in 8-lead TO-99 hermatic package

Fig. 26 - Conventional positive feedback



Pin connections shown are for LM311H in 8-lead TO-99 hermetic package

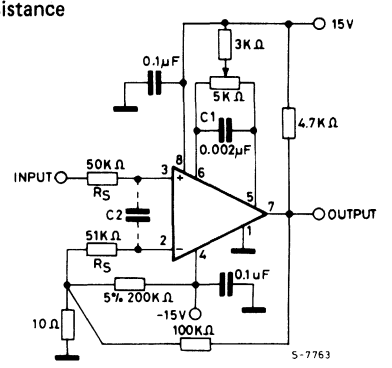
inches away from the LM311 and the 0.01μF capacitor should be installed. If this capacitor cannot be used, a shielding printed-circuit foil may be advisable between pins 6 and 7. The power supply bypass capacitors should be located within a couple inches of the LM311. (Some other comparators require the power-supply bypass to be located immediately adjacent to the comparator).

6. It is a standard procedure to use hysteresis positive feedback) around a comparator, to prevent oscillation, and to avoid excessive noise on the output because the comparator is a good amplifier for its own noise. In the circuit of Figure 26 the feedback from the output to the positive input will cause about 3mV of hysteresis. However, if R_s is larger than 100Ω, such as 50kΩ, it would bot be reasonable to simply increase the value of the positive feedback resistor above 510kΩ. The circuit of Figure 27 could be used, but it is rather awkward. See the notes in paragraph 7 below.

7. When both inputs of the LM311 are connected to active signals, or if a high-impedance signal is driving the positive input of the LM311 so that positive feedback would be distributive, the circuit of Figure 25 is ideal. The positive feedback is to pin 5 (one of the offset adjustment pins). It is sufficient to cause 1 to 2mV hysteresis and sharp transitions with input triangle waves from a few Hz to hundreds of kHz. The positive-feedback signal across the 82Ω resistor swings 240mV below the positive supply. This signal is centered around the nominal voltage at pin 5, so this feedback does not add to the V_{os} of the comparator. As much as 8mV of V_{os} can be trimmed out, using the 5kΩ pot and 3kΩ resistor as shown.

8. These application notes apply specifically to the LM311, and are applicable to all high-speed comparators in general, (with the exception that not all comparators have trim pins).

Fig. 27 - Positive feedback with high source resistance

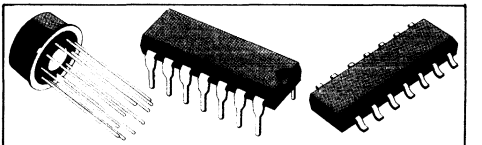


LM723

HIGH PRECISION VOLTAGE REGULATOR

- INPUT VOLTAGE UP TO 40V
- OUTPUT VOLTAGE ADJUSTABLE FROM 2 TO 37V
- POSITIVE OR NEGATIVE SUPPLY OPERATION
- SERIES, SHUNT, SWITCHING OR FLOATING OPERATION
- OUTPUT CURRENT TO 150mA WITHOUT EXTERNAL PASS TRANSISTOR
- ADJUSTABLE CURRENT LIMITING

The LM723 is a monolithic integrated programmable voltage regulator, assembled in 14-lead dual in-line plastic and ceramic package, 10-lead Metal Can (TO-100 type) and SO-14 micropackage. The circuit provides internal current limiting. When the output current excedes 150mA an external NPN or PNP pass elément may be used. Provisions are made for adjustable current limiting and remote shut-down.

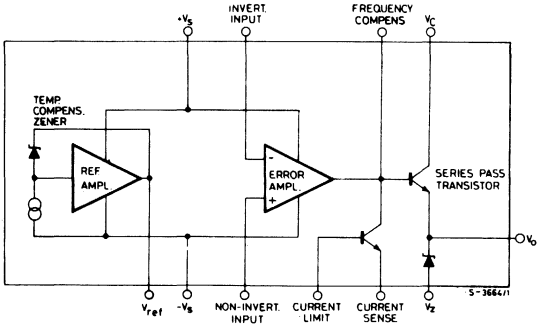


TO-100 **DIP-14** **SO-14**
(Ceramic and Plastic)

ABSOLUTE MAXIMUM RATINGS

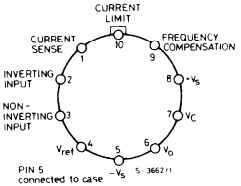
		LM723	LM723C
V_i	Input voltage	40V	40V
ΔV_{i-o}	Dropout voltage	40V	40V
I_o	Output current	150mA	150mA
I_{ref}	Current from V_{ref}	15mA	25mA
T_{op}	Operating temperature	-55 to 125°C	0 to 70°C
T_{stg}	Storage temperature	-65 to 150°C	-65 to 150°C
T_j	Junction temperature	150°C	125°C

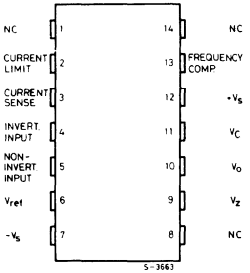
BLOCK DIAGRAM



LM723

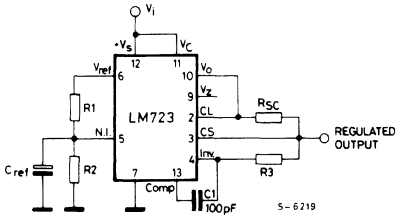
CONNECTION DIAGRAM AND ORDERING NUMBERS
(top views)





Type	TO-100	Creramic DIP-14	Plastic DIP-14	SO-14
LM723	LM723H	LM723J	—	—
LM723C	LM723CH	LM723CJ	LM723CN	LM723CD

TEST CIRCUIT
(Pin configuration relative to the Plastic package)



$V_i = 12V$
$V_o = 5V$
$I_o = 1$ mA
$R_1 // R_2 \leq 10$ KΩ

THERMAL DATA

			Plastic DIP-14	Ceramic DIP-14	TO-100	SO-14
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	200°C/W	150°C/W	155°C/W	165°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_{amb}= 25°C unless otherwise specified)

Parameter		Test conditions	LM 723C			LM 723			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
$\frac{\Delta V_o}{\Delta V_i}$	Line regulation	V_i = 12 to 15V V_i = 12 to 40V		0.01 0.1	0.1 0.5		0.01 0.02	0.1 0.2	%
		V_i = 12 to 15V; $T_{min} \leq T_{amb} \leq T_{max}$			0.3			0.3	
$\frac{\Delta V_o}{V_o}$	Load regulation	I_o = 1 to 50 mA		0.03	0.2		0.03	0.15	%
		$T_{min} \leq T_{amb} \leq T_{max}$ I_o = 1 to 10 mA			0.6			0.6	%
V_{ref}	Reference voltage	I_{ref}= 160 μA	6.8	7.15	7.5	6.95	7.15	7.35	V
SVR	Ripple rejection	f = 100 Hz to 10 KHz C_{ref}= 0 C_{ref}= 5 μF		 74 86			 74 86		 dB dB
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift				150			150	$\frac{ppm}{°C}$
I_{sc}	Short circuit current limiting	R_{sc}= 10Ω V_o= 0		65			65		mA
V_i	Input voltage range		9.5		40	9.5		40	V
V_o	Output voltage range		2		37	2		37	V
V_i-V_o			3		38	3		38	V
I_d	Quiescent drain current	I_o = 0 V_i = 30V		2.3	4		2.3	5	mA
	Long term stability			0.1			0.1		$\frac{\%}{1000 \text{ hrs}}$
e_N	Output noise voltage	BW= 100 Hz to 10 KHz C_{ref}= 0 C_{ref}= 5 μF		 20 2.5			 20 2.5		 μV μV
V_z	Output zener voltage (for plastic package only)	I_z = 1 mA	6.9		7.7				V

Note: T_{min} = 0°C (LM723C); 125°C (LM723)
T_{max} = 70°C (LM723C); -55°C (LM723).

Fig. 1 - Maximum output current vs. voltage drop

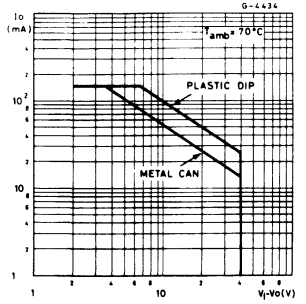


Fig. 2 - Current limiting characteristics

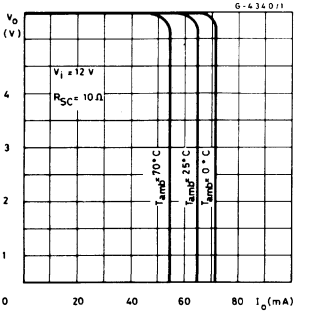


Fig. 3 - Current limiting characteristics vs. junction temperature

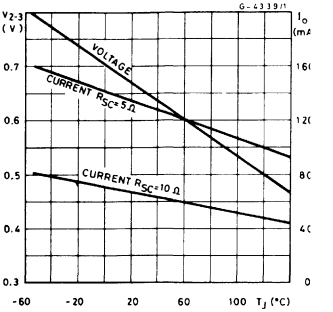


Fig. 4 - Load regulation characteristics without current limiting

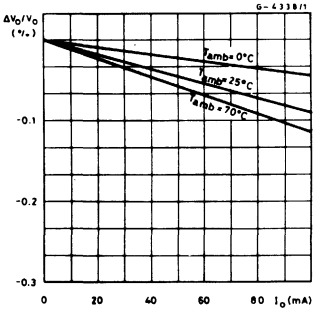


Fig. 5 - Load regulation characteristics with current limiting

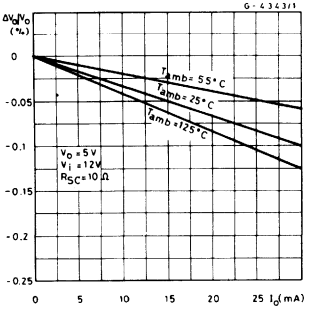


Fig. 6 - Load regulation characteristics with current limiting

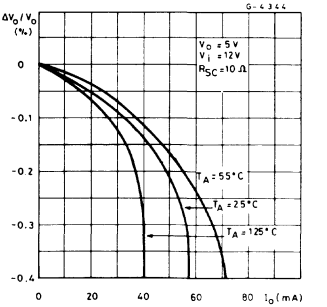


Fig. 7 - Line regulation vs. voltage drop

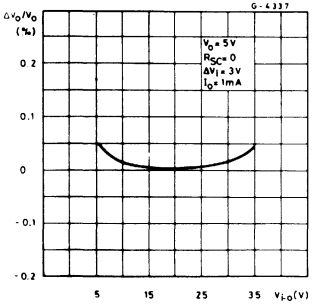


Fig. 8 - Load regulation vs. voltage drop

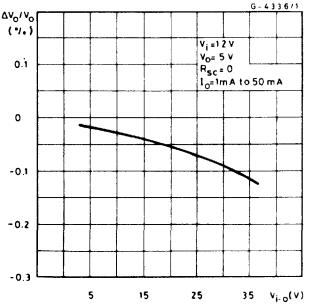


Fig. 9 - Quiescent drain current vs. input voltage

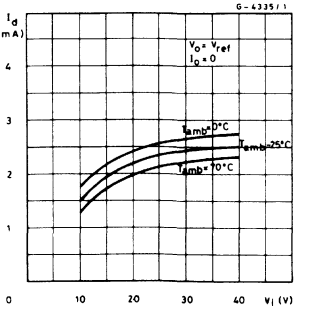


Fig. 10 - Line transient response

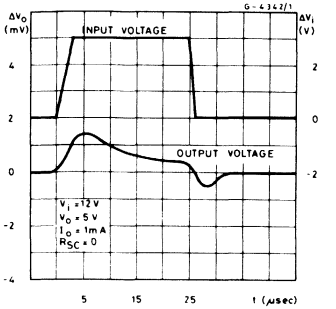


Fig. 11 - Load transient response

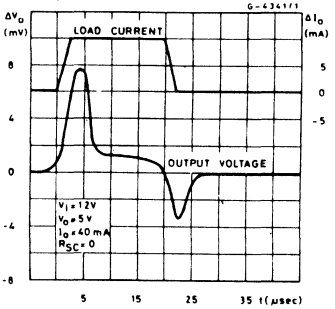


Fig. 12 - Output impedance vs. frequency

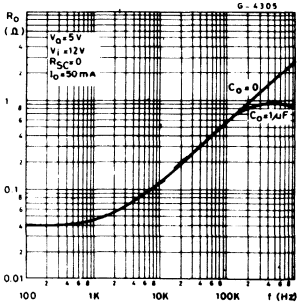


Table I — Resistor values (KΩ) for standard output voltages

Output Voltage	Applicable Figures	Fixed Output ± 5%		Output Adjustable ± 10% (°)			Output Voltage	Applicable Figures	Fixed Output ± 5%		Output Adjustable ± 10% (°)		
		R_1	R_2	R_1	P_1	R_2			R_1	R_2	R_1	P_1	R_2
+ 3	13, 16, 17 18, 21, 23	4.12	3.01	1.8	0.5	1.2	+100	19	3.57	102	2.2	10	91
+ 5	13, 16, 17 18, 21, 23	2.15	4.99	0.75	0.5	2.2	+250	19	3.57	255	2.2	10	240
+ 6	13, 16, 17 18, 21, 23	1.15	6.04	0.5	0.5	2.7	- 6(°°)	15	3.57	2.43	1.2	0.5	0.75
+ 9	14, 16, 17 18, 21, 23	1.87	7.15	0.75	1	2.7	- 9	15	3.48	5.36	1.2	0.5	2
+12	14, 16, 17 18, 21, 23	4.87	7.15	2	1	3	- 12	15	3.57	8.45	1.2	0.5	3.3
+15	14, 16, 17 18, 21, 23	7.87	7.15	3.3	1	3	- 15	15	3.65	11.5	1.2	0.5	4.3
+28	14, 16, 17 18, 21, 23	21	7.15	5.6	1	2	- 28	15	3.57	24.3	1.2	0.5	10
+45	19	3.57	48.7	2.2	10	39	- 45	20	3.57	41.2	2.2	10	33
+75	19	3.57	78.7	2.2	10	68	-100	20	3.57	97.6	2.2	10	91
							-250	20	3.57	249	2.2	10	240

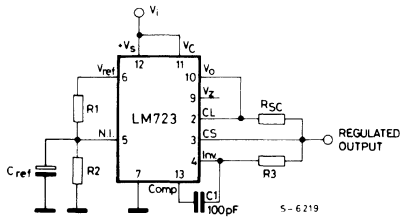
Note: (°) Replace R_1/R_2 divider with the circuit of fig. 24.
(°°) V^+ must be connected to a +3V or greater supply.

Table II — Formulae for intermediate output voltages

Outputs from +2 to +7 volts Fig. 13, 17, 18, 21, 23, 16 $V_O = [V_{ref} \times \frac{R_2}{R_1 + R_2}]$	Outputs from +4 to +250 volts Fig. 19 $V_O = [\frac{V_{ref}}{2} \times \frac{R_2 - R_1}{R_1}]$; $R_3 = R_4$	Current Limiting $I_{LIMIT} = \frac{V_{SENSE}}{R_{sc}}$
Outputs from +7 to +37 volts Fig. 14, 16, 17, 18, 21, 23 $V_O = [V_{ref} \times \frac{R_1 + R_2}{R_2}]$	Output from -6 to -250 volts Fig. 15, 20 $V_O = [\frac{V_{ref}}{2} \times \frac{R_1 + R_2}{R_1}]$; $R_3 = R_4$	Foldback Current Limiting $I_{KNEE} = [\frac{V_O}{R_{sc}} \frac{R_3}{R_4} + \frac{V_{SENSE}}{R_{sc}} \frac{(R_3 + R_4)}{R_4}]$ $I_{SHORT\ CKT} = [\frac{V_{SENSE}}{R_{sc}} \times \frac{R_3 + R_4}{R_4}]$

APPLICATION INFORMATION (Pin numbers relative to the plastic package)

Fig. 13 - Basic low voltage regulator
(V_o = 2 to 7V)

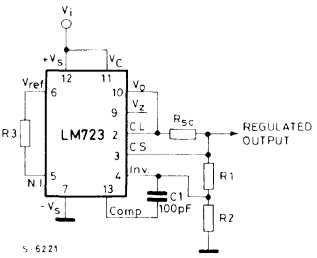


NOTE: $R3 = \frac{R1 \cdot R2}{R1 + R2}$ for minimum temperature drift.

R3 may be eliminated for minimum component count.

Typical performance
Regulated Output Voltage 5V
Line Regulation (ΔV_i = 3V) . . . . . .0.5 mV
Load Regulation (ΔI_O = 50 mA) . . . .1.5 mV

Fig. 14 - Basic high voltage regulator
(V_o = 7 to 37V)

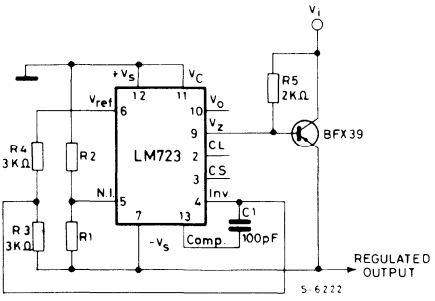


NOTE: $\frac{R1 \cdot R2}{R1 + R2}$ for minimum temperature drift.

R3 may be eliminated for minimum component count.

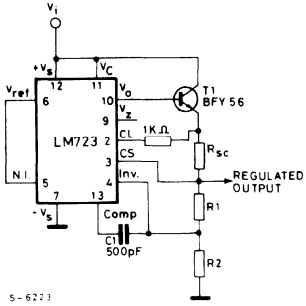
Typical performance
Regulated Output Voltage 15V
Line Regulation (ΔV_i = 3V) . . . . . .1.5 mV
Load Regulation (ΔI_O = 50 mA) . . . .4.5 mV

Fig. 15 - Negative voltage regulator



Typical performance
Regulated Output Voltage . . . . . .-15V
Line Regulation (ΔV_i = 3V) . . . . . .1 mV
Load Regulation (ΔI_O = 100 mA) . . . .2 mV

Fig. 16 - Positive voltage regulator (External NPN Pass Transistor)



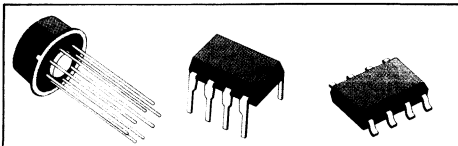
Typical performance
Regulated Output Voltage . . . . . .+15V
Line Regulation (ΔV_i = 3V) . . . . . .1.5 mV
Load Regulation (ΔI_O = 1A) . . . . . .15 mV

LM741

FREQUENCY COMPENSATED OPERATIONAL AMPLIFIERS

- NO FREQUENCY COMPENSATION REQUIRED
- SHORT CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGE
- NO LATCH-UP

The LM741 series consists of general purpose operational amplifiers, intended for a wide range of analog applications. High common mode voltage range and absence of "latch-up" tendencies make the LM741 series ideal for use as a voltage follower. The high gain and wide range of operating voltage provide superior performance in integrators, summing amplifiers, and general feedback applications.

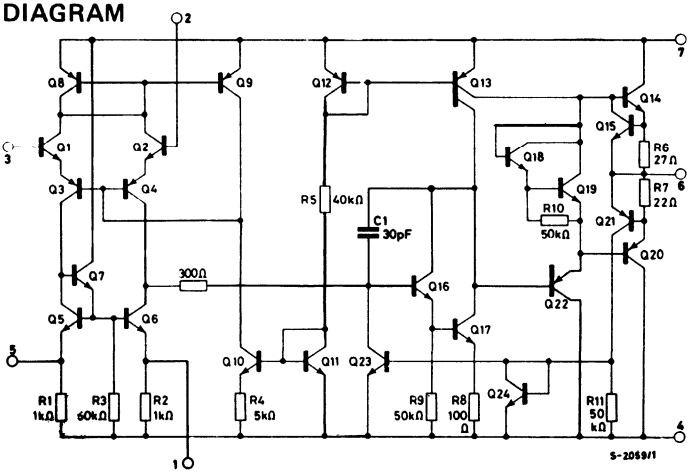


TO-99 **Minidip** **SO-8**
(Plastic and Ceramic)

ABSOLUTE MAXIMUM RATINGS		LM741/A	LM741E	LM741I	LM741C
V_s	Supply voltage	± 22V	± 22V	± 18V	± 18V
V_i (1)	Input voltage	± 15V	± 15V	± 15V	± 15V
ΔV_i	Differential input voltage	± 30V	± 30V	± 30V	± 30V
T_{op}	Operating temperature	-55 to 125°C	0 to 70°C	-25 to 85°C	0 to 70°C
	Output short circuit duration (2)	indefinite			
T_j	Junction temperature	150°C			
T_{stg}	Storage temperature	-65 to 150°C			

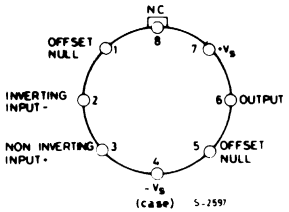
(1) For supply voltage less than ± 15V, input voltage es equal to the supply voltage
(2) The short circuit duration is limited by thermal dissipation

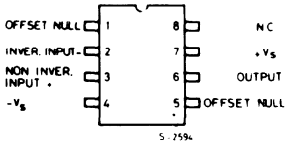
SCHEMATIC DIAGRAM



LM741

CONNECTION DIAGRAMS
(top view)





ORDERING NUMBERS:

Type	TO-99	Ceramic Minidip	Plastic Minidip	SO-8
LM741	LM741 H	LM741 J	–	–
LM741A	LM741 AH	–	–	–
LM741C	LM741 CH	LM741 CJ	LM741 CN	LM741 CD
LM741E	–	LM741 EJ	LM741 EN	–
LM741I	–	–	–	LM741 ID

THERMAL DATA

			Plastic Minidip	Ceramic Minidip	TO-99	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction ambient	max	120°C/W	150°C/W	155°C/W	200°C/W

ELECTRICAL CHARACTERISTICS (see note)

Parameter		Test conditions	LM741/LM741I			LM741A/741E			LM 741C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{os}	Input offset voltage	T_{amb}= 25°C $R_g \leq 10\ k\Omega$ $R_g \leq 50\ \Omega$		1	5		0.8	3		2	6	mV mV
		T_{amb}= T_{min} to T_{max} $R_g \leq 10\ k\Omega$ $R_g \leq 50\ \Omega$			6			4			7.5	mV mV
ΔV_{os}	Input offset voltage adjust. range	V_s= ± 20V V_s= ± 15V T_{amb}= 25°C		±15		±10				±15		mV
$\frac{\Delta V_{os}}{\Delta T}$	Average input offset voltage drift							15				$\frac{\mu V}{°C}$
I_{os}	Input offset current	T_{amb}= 25°C T_{amb}= T_{min} to T_{max}		20 85	200 500		3	30 70		20	200 300	nA nA
$\frac{\Delta I_{os}}{\Delta T}$	Average input offset current drift							0.5				$\frac{nA}{°C}$
I_b	Input bias current	T_{amb}= 25°C T_{amb}= T_{min} to T_{max}		80	500 1.5		30	80 0.21		80	500 0.8	nA μA
R_i	Input resistance	T_{amb}= 25°C T_{amb}= T_{min} to T_{max}	0.3	2		1 0.5	6		0.3	2		MΩ MΩ
V_i	Input voltage range	T_{amb}= T_{min} to T_{max}	±12	±13		±12	±13		±12	±13		V
G_v	Large signal voltage gain	T_{amb}= 25°C $R_L \geq 2\ k\Omega$ V_s= ±15V V_o= ±10V	94	106		94			86	106		dB
		T_{amb}= T_{min} to T_{max} $R_L \geq 2\ k\Omega$ V_s= ±15V V_o= ±10V V_s= ±5V V_o= ±2V	88			90 80			84			dB
V_o	Output voltage swing	V_s= ±15V $R_L \geq 10\ k\Omega$ $R_L \geq 2\ k\Omega$	±12 ±10	±14 ±13		±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
I_{sc}	Output short circuit current	T_{amb}= 25°C T_{amb}= T_{min} to T_{max}		25		10 10	25	35 40		25		mA mA
CMR	Common mode rejection	V_s = ±20V $R_g \leq 10\ k\Omega$ V_{CM}=±12V	70	90		80	95		70	90		dB
SVR	Supply voltage rejection	$R_g \leq 50\Omega$ V_s=±5 to ±20V $R_g \leq 10k\Omega$ V_s=±5 to ±15V	77	96		86	96		77	96		dB dB

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	LM741/741I			LM741A/741E			LM 741C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
	Transient respon. (unity gain) Rise time Overshoot	T_{amb}= 25°C		 0.3 5			 0.25 6	 0.8 20		 0.3 5		 µs %
B	Bandwidth	T_{amb}= 25°C				0.437	1.5					MHz
SR	Slew rate	T_{amb}= 25°C		0.5		0.3	0.7			0.5		V/µs
I_s	Supply current	T_{amb}= 25°C		1.7	2.8					1.7	2.8	mA
P_{tot}	Power consumption	T_{amb}= 25°C V_s= ±20V V_s= ±15V		 50	 85		 80	 150		 50	 85	 mW mW
		V_s= ±20V T_{amb}= T_{min} T_{amb}= T_{max}						 165 135				 mW mW
		V_s= ±15V T_{amb}= T_{min} T_{amb}= T_{max}		 60 45	 100 75							 mW mW

Note: These specifications, unless otherwise specified, apply for V_s= ±15V and T_{amb}= -55 to 125°C for LM 741 and LM741A. For the LM741C and LM741E these specifications apply for T_{amb} = 0 to 70°C.

Fig. 1 - Open loop voltage gain vs. supply voltage

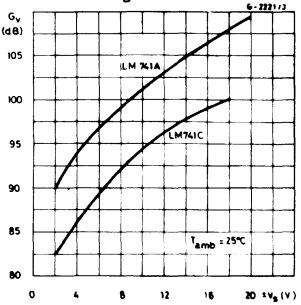


Fig. 2 - Output voltage swing vs. supply voltage

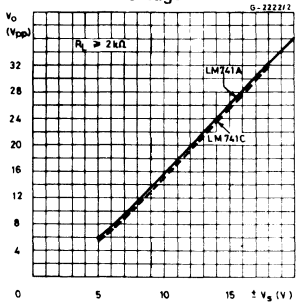


Fig. 3 - Power consumption vs. supply voltage

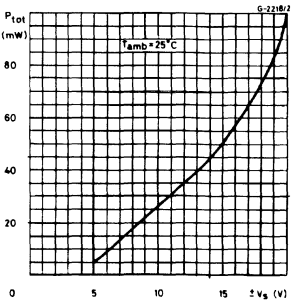


Fig. 4 - Open loop voltage gain vs. frequency

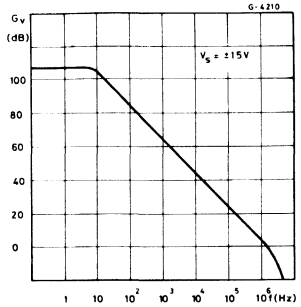


Fig. 5 - Open loop phase response vs. frequency

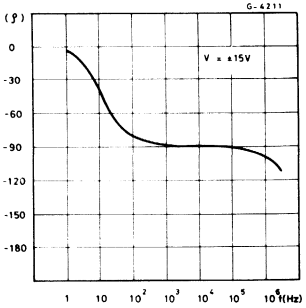


Fig. 6 - Input offset current vs. supply voltage (for LM741 and LM741C)

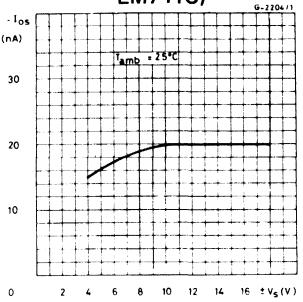


Fig. 7 - Input resistance and capacitance vs. frequency (for LM741 and LM741C)

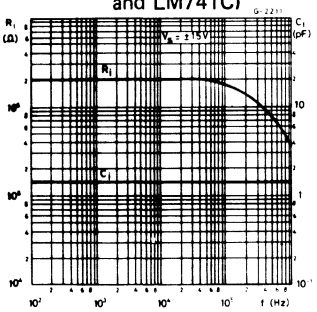


Fig. 8 - Output resistance vs. frequency

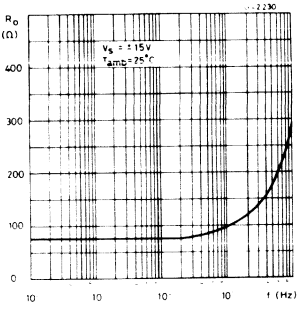


Fig. 9 - Output voltage swing vs. load resistance

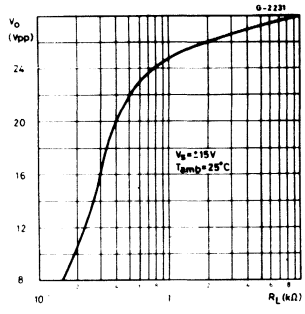


Fig. 10 - Output voltage swing vs. frequency

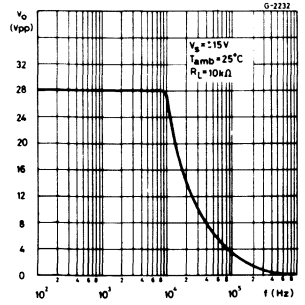


Fig. 11 - Input noise voltage vs. frequency

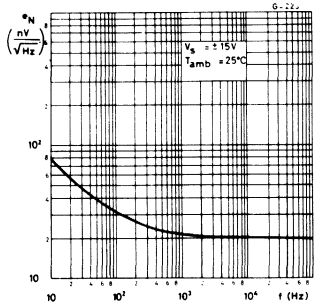


Fig. 12 - Input noise current vs. frequency

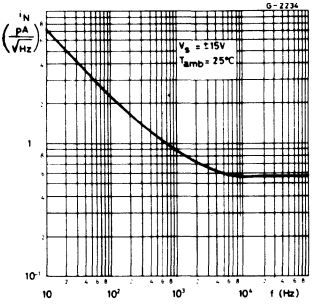


Fig. 13 - Transient response

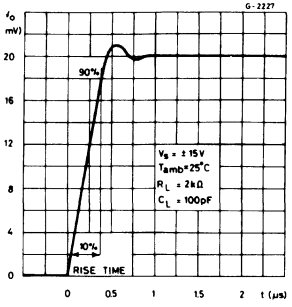


Fig. 14 - Common mode rejection ratio vs. frequency

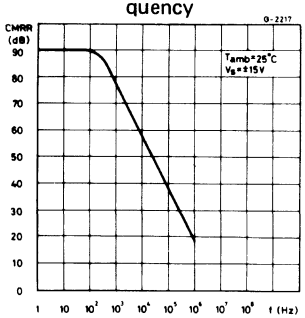
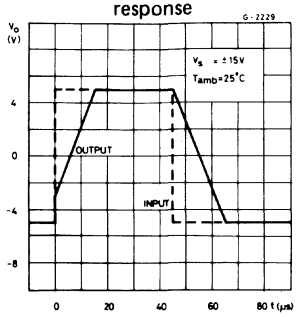


Fig. 15 - Voltage follower large signal pulse response



Typical performance curves for LM741 and LM741A

Fig. 16 - Input bias current vs. ambient temperature

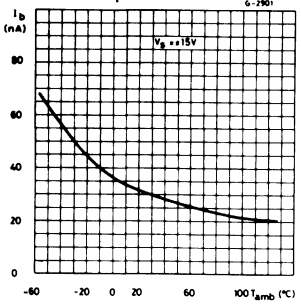


Fig. 17 - Input resistance vs. ambient temperature

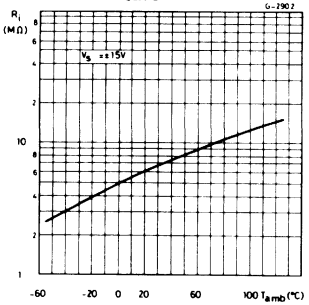


Fig. 18 - Input offset current vs. ambient temperature

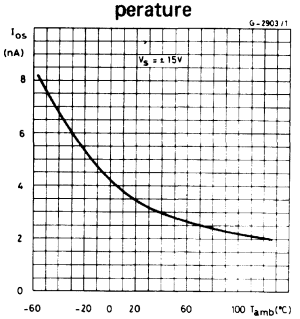


Fig. 19 - Output short-circuit current vs. ambient temperature

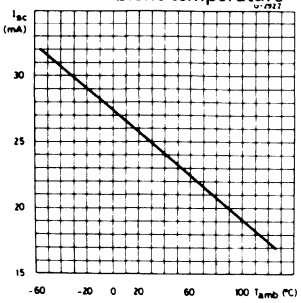


Fig. 20 - Power consumption vs. ambient temperature

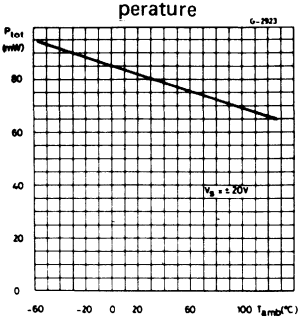
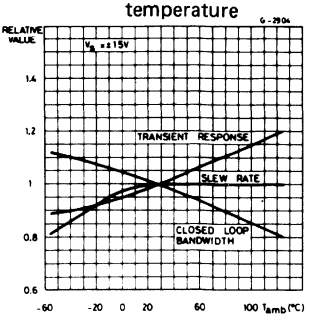


Fig. 21 - Frequency characteristics vs. ambient temperature



Typical performance curves for LM741C

Fig. 22 - Input bias current vs. ambient temperature

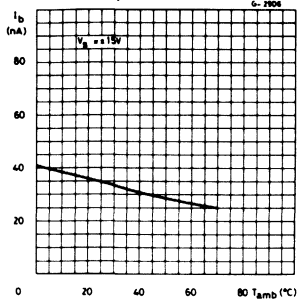


Fig. 23 - Input resistance vs. ambient temperature

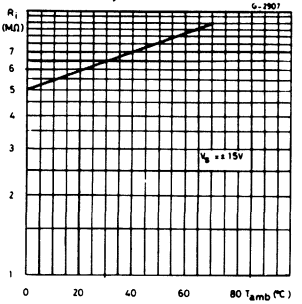


Fig. 24 - Input offset current vs. ambient temperature

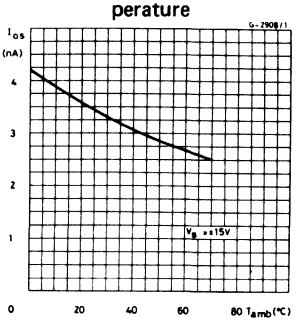


Fig. 25 - Output short circuit current vs. ambient temperature

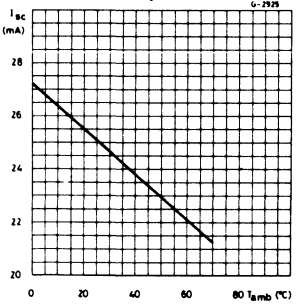


Fig. 26 - Power consumption vs. ambient temperature

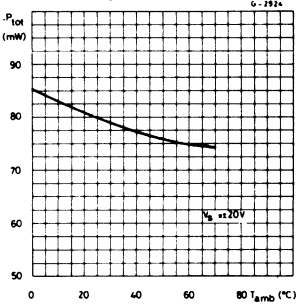
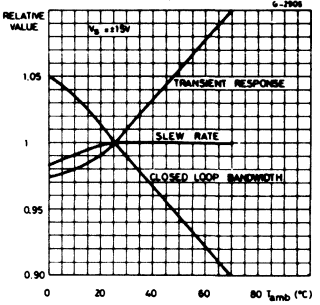


Fig. 27 - Frequency characteristics vs. ambient temperature



TYPICAL APPLICATIONS

Fig. 28 - Clipping amplifier

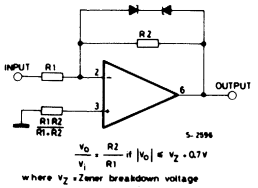


Fig. 29 - Simple integrator

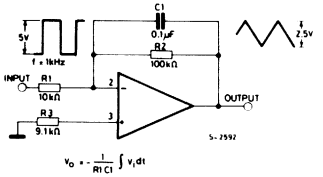
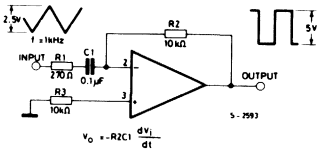


Fig. 30 - Simple differentiator

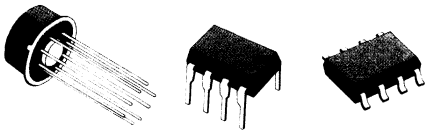


LM748

OPERATIONAL AMPLIFIERS

- SHORT CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGE
- NO LATCH-UP
- SLEW-RATE = 5.5V/μs ($G_v = 10, C_c = 3.3pF$)

The LM748 series consists of general purpose operational amplifiers, intended for a wide range of analog applications where tailoring of frequency characteristics is desirable. High common mode voltage range and absence of "Latch-up" tendencies make the LM748 series ideal for use as a voltage follower. The high gain and wide range of operating voltage provide superior performance in integrators, summing amplifiers and general feedback applications. Unity gain frequency compensation is achieved by means of a single 30pF capacitors.



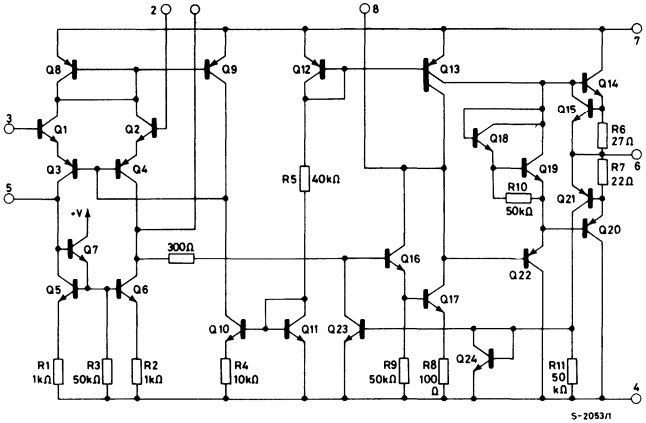
TO-99 **Minidip (Plastic and Ceramic)** **SO-8**

ABSOLUTE MAXIMUM RATINGS

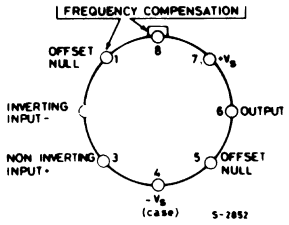
		LM748/A	LM748I	LM748C
V_s	Supply voltage	± 22V	± 22V	± 22V
V_i (1)	Input voltage	± 15V	± 15V	± 15V
ΔV_i	Differential input voltage	± 30V	± 30V	± 30V
T_{op}	Operating temperature	-55 to 125°C	-25 to 85°C	0 to 70°C
	Output short circuit duration (2)	indefinite	indefinite	indefinite
T_j	Junction temperature	150°C	150°C	150°C
T_{stg}	Storage temperature	-65 to 150°C	-65 to 150°C	-65 to 150°C

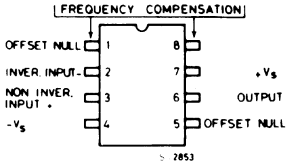
(1) For supply voltages less than ± 15V, input voltage is equal to the supply voltage
(2) The short circuit duration is limited by thermal dissipation

SCHEMATIC DIAGRAM



CONNECTION DIAGRAMS
(top views)





ORDERING NUMBERS

Type	TO-99	Ceramic Minidip	Plastic Minidip	SO-8
LM748	LM748 H	LM748J	–	–
LM748C	LM748 CH	LM748 CJ	LM748 CN	LM748 CD
LM748A	LM748 AH	–	–	–
LM748I	–	–	–	LM748ID

THERMAL DATA

			Plastic Minidip	Ceramic Minidip	TO-99	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max.	120°C/W	150°C/W	155°C/W	200°C/W

ELECTRICAL CHARACTERISTICS (see note)

Parameter		Test conditions	LM748/748I			LM748A			LM748C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{os}	Input offset voltage	T_{amb}= 25°C $R_g \leq 10\ k\Omega$ $R_g \leq 50\Omega$		1	5		0.5	2		2	6	mV mV
		$T_{amb}= T_{min}$ to T_{max} $R_g \leq 10\ k\Omega$ $R_g \leq 50\Omega$		1	6		0.5	3			7.5	mV mV
ΔV_{os}	Input offset voltage adjust. range	T_{amb}= 25°C		±15			±25			±15		mV
$\frac{\Delta V_{os}}{\Delta T}$	Average input offset voltage drift	$R_g \leq 50\Omega$					2.5	15				$\frac{\mu V}{°C}$
I_{os}	Input offset current	T_{amb}= 25°C $T_{amb}= T_{min}$ to T_{max}		20 50	200 500		2	10 25		20	200 300	nA nA
$\frac{\Delta I_{os}}{\Delta T}$	Average input offset current drift							0.15				$\frac{nA}{°C}$
I_b	Input bias current	T_{amb}= 25°C $T_{amb}= T_{min}$ to T_{max}		80	500 1.5		20	75 0.1		80	500 0.8	nA μA
R_i	Input resistance	T_{amb}= 25°C	0.3	2		2	10		0.3	2		MΩ
V_i	Input voltage range		±12	±13		±12	±13		±12	±13		V
G_v	Large signal voltage gain	T_{amb}= 25°C $R_L \geq 2\ k\Omega$ V_s= ±15V V_o= ±10V $T_{amb}= T_{min}$ to T_{max} $R_L \geq 2\ k\Omega$ V_s= ±15V V_o= ±10V	94 88	104		94 88	108		86 84	104		dB dB
V_o	Output voltage swing	V_s= ±15V $R_L \geq 10\ k\Omega$ $R_L \geq 2\ k\Omega$	±12 ±10	±14 ±13		±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
I_{sc}	Output short circuit current			25			25			25		mA
CMR	Common mode rejection	$R_g \leq 10\ k\Omega$ V_{CM}= ±12V	70	90		80	95		70	90		dB
SVR	Supply voltage rejection	V_s= ±5 to ± 20V $R_g \leq 10\ k\Omega$	76	90		80	97		76	90		dB
SR	Slew rate	T_{amb}= 25°C, $R_L \geq 2\ k\Omega$, G_v= 1		0.5			0.5			0.5		V/μs
		T_{amb}= 25°C, $R_L \geq 2\ k\Omega$, G_v= 10*		5.5			5.5			5.5		V/μs

* C_C = 3.5 pF

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	LM748/748I			LM748A			LM748C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
	Transient respon. (unity gain)	T_{amb}= 25°C V_i= 20 mV C_c= 30 pF R_L= 2 kΩ $C_L \leqslant$ 100 pF										
	Rise time			0.2			0.2			0.2		µs
	Overshoot			5			5			5		%
I_s	Supply current	T_{amb}= 25°C		1.9	2.8		1.9	2.8		1.9	2.8	mA
P_S	Power consumption	T_{amb}= 25°C V_s= ±20V					60	85				mW
		V_s= ±15V		60	85					60	85	mW
		V_s= ±15V T_{amb}= T_{min}		60	100		60	100		60	100	mW
		T_{amb}= T_{max}		45	75		40	75				mW

Note. These specifications, unless otherwise specified, apply for V_s = ± 15V and T_{amb} = -55 to 125°C for LM748 and LM748A. For LM748C and LM748I these specifications apply for T_{amb} = 0 to 70°C (C_c = 30pF).

Fig. 1 - Voltage offset null circuit

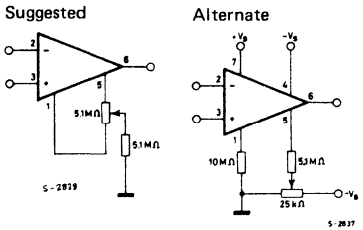
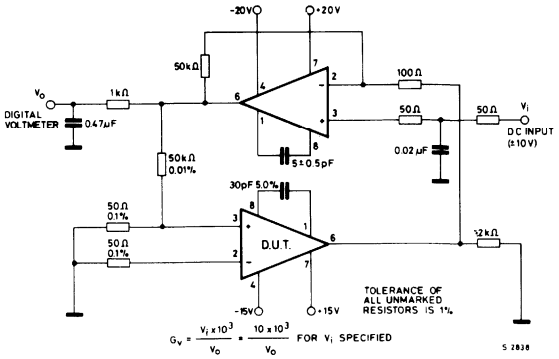


Fig. 2 - Gain test circuit



Typical performance curves for LM748

Fig. 3 - Input bias current vs. ambient temperature

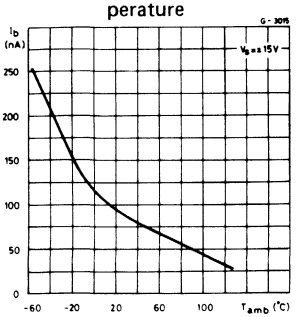


Fig. 4 - Input resistance vs. ambient temperature

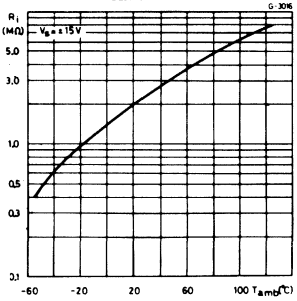


Fig. 5 - Output short-circuit current vs. ambient temperature

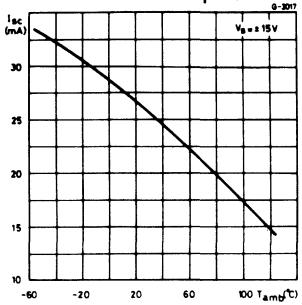


Fig. 6 - Input offset current vs. ambient temperature

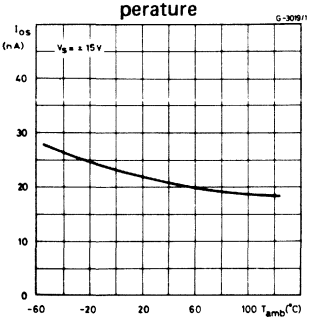


Fig. 7 - Power consumption vs. ambient temperature

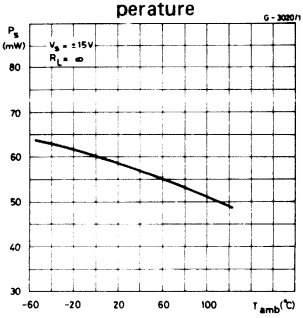
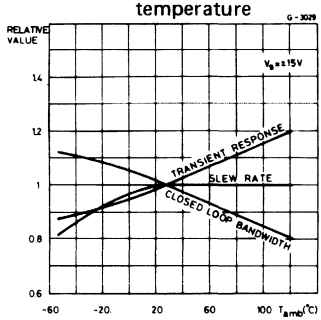


Fig. 8 - Frequency characteristics vs. ambient temperature



Typical performance curves for LM748C

Fig. 9 - Input bias current vs. ambient temperature

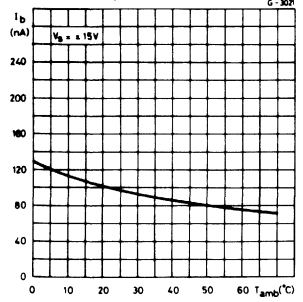


Fig. 10 - Input resistance vs. ambient temperature

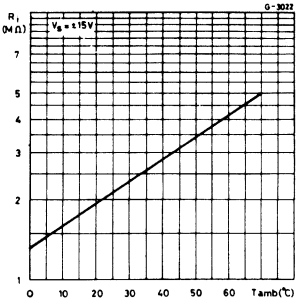


Fig. 11 - Output short-circuit current vs. ambient temperature

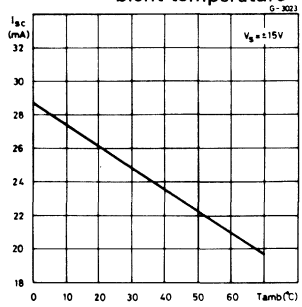


Fig. 12 - Input offset current vs. ambient temperature

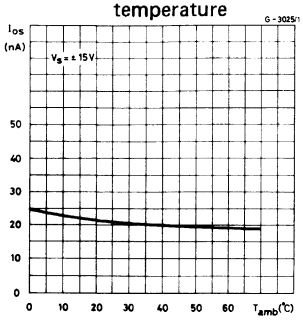


Fig. 13 - Power consumption vs. ambient temperature

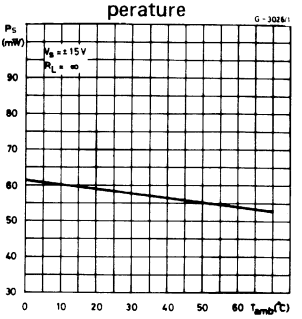
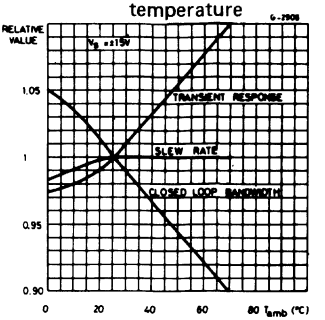


Fig. 14 - Frequency characteristics vs. ambient temperature



Typical performance curves for LM748 and LM748C

Fig. 15 - Open loop voltage gain vs. supply voltage

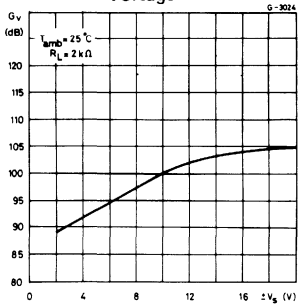


Fig. 16 - Output voltage swing vs. supply voltage

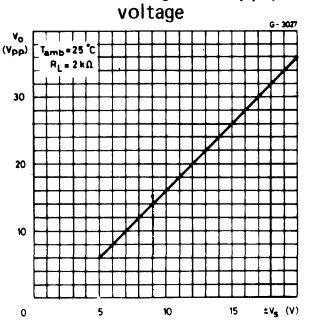


Fig. 17 - Power consumption vs. supply voltage

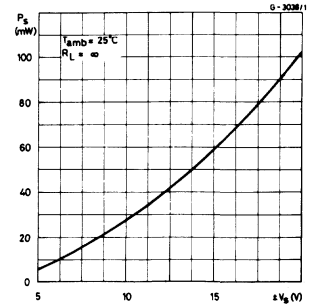


Fig. 18 - Output voltage swing vs. load resistance

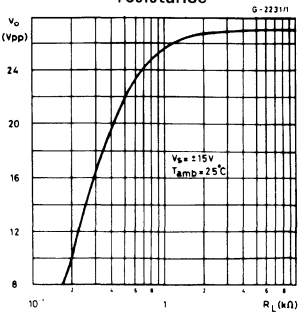


Fig. 19 - Input offset current vs. supply voltage

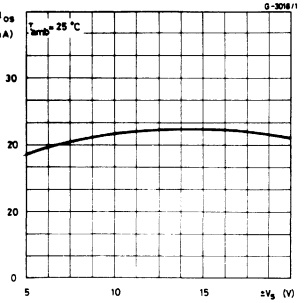


Fig. 20 - Input common mode voltage range vs. supply voltage

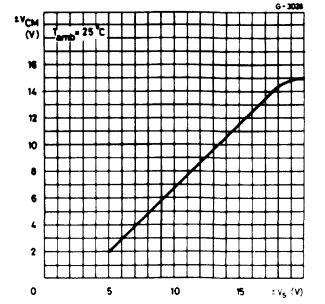


Fig. 21 - Input noise voltage vs. frequency

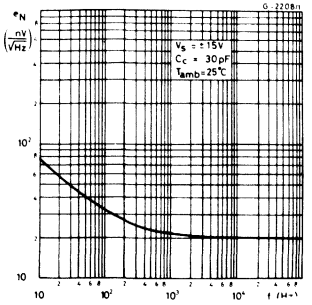


Fig. 22 - Input noise current vs. frequency

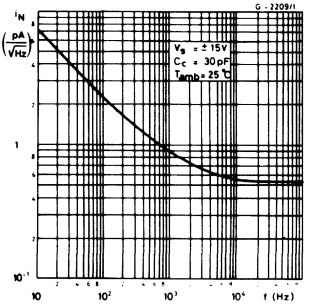


Fig. 23 - Broadband noise for various bandwidths

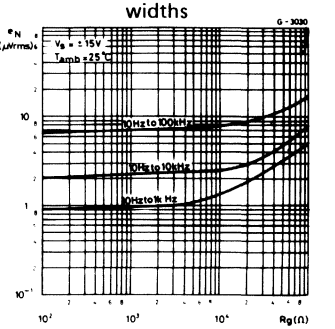


Fig. 24 - Open loop frequency and phase response vs. frequency

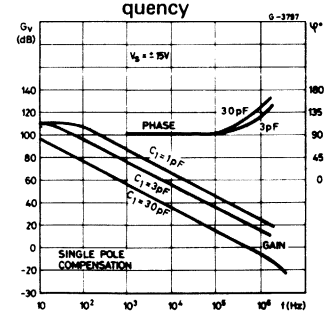


Fig. 25 - Output voltage swing vs. frequency

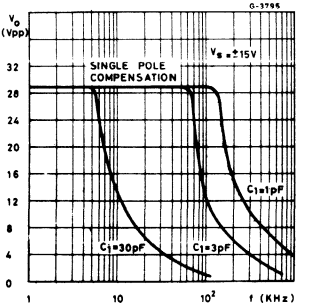


Fig. 26 - Slew-rate

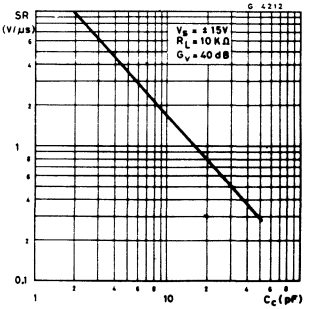


Fig. 27 - Compensation capacitance vs. closed loop voltage gain

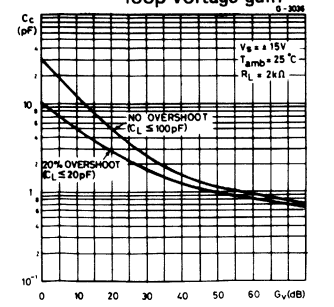


Fig. 28 - Input resistance and input capacitance vs. frequency

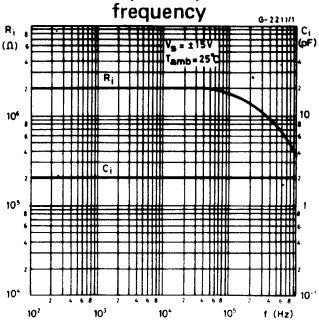


Fig. 29 - Output resistance vs. frequency

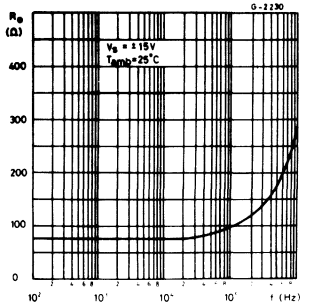


Fig. 30 - Frequency characteristics vs. supply voltage

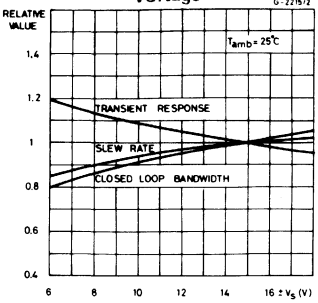


Fig. 31 - Voltage follower transient response (unity gain)

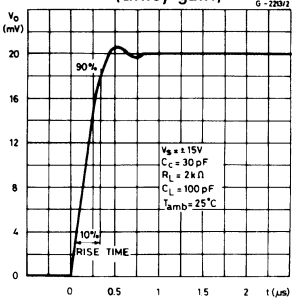


Fig. 32 - Transient response test circuit

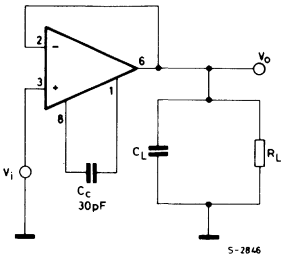


Fig. 33 - Voltage follower large-signal pulse response

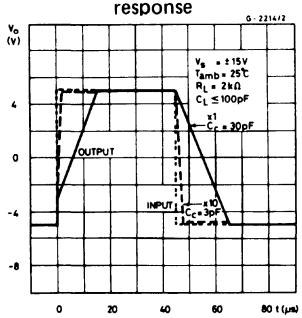


Fig. 34 - Feed forward compensation

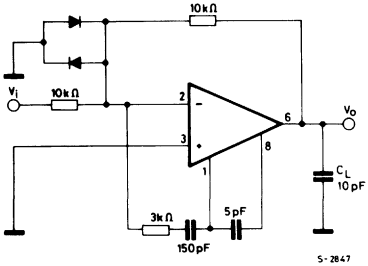
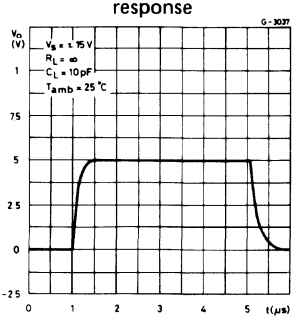
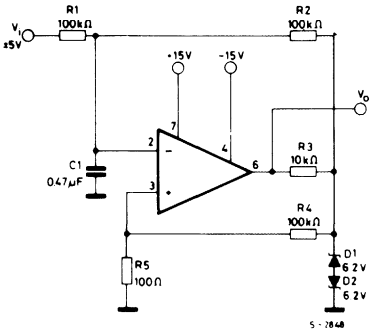


Fig. 35 - Large signal feed forward transient response



TYPICAL APPLICATIONS

Fig. 36 - Pulse width modulator



$f_c = \frac{1}{2\pi R2\,C1}$

$f_n = \frac{1}{2\pi R1\,C1} = \frac{1}{2\pi R2\,C2}$

$f_c < f_n < f_{unity\ gain}$

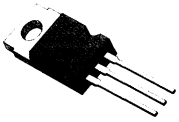
LM2930A

PRELIMINARY DATA

VERY LOW DROP VOLTAGE REGULATOR

- INPUT/OUTPUT DROP TYP. 0.2V AT 150mA
- OUTPUT CURRENT IN EXCESS OF 400mA
- 40V LOAD DUMP PROTECTION
- -40 TRANSIENT PROTECTION
- REVERSE POLARITY PROTECTION
- OVERVOLTAGE PROTECTION
- FOLDBACK CURRENT LIMITING
- THERMAL SHUTDOWN

The LM2930A is an improved version of the LM2930 5V voltage regulator which features an output current rating of 400mA with a dropout voltage of typically 0.4V. At 150mA the dropout voltage falls to 0.2V. Moreover, the LM2930A includes load dump protection plus reverse polarity protection, input overvoltage protection, thermal shutdown and foldback current limiting. Designed primarily for automotive applications, the LM2930A protects both itself and the load from load dump transients and incorrect battery connection. The low voltage drop of this device allows correct operation even during starting when the battery voltage can fall below 6V. The LM2930A is available in a TO-220 plastic power package.



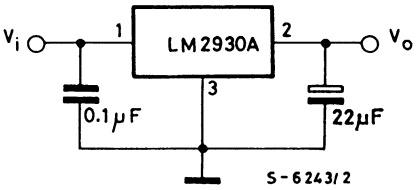
TO-220

ORDERING NUMBER: LM2930A

ABSOLUTE MAXIMUM RATINGS

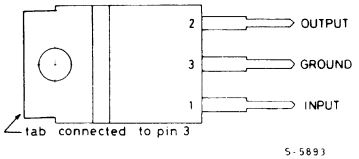
V_i	Forward input voltage	26	V
	Overvoltage protection (t = 100ms)	± 40	V
T_{op}	Operating temperature range	-40 to +85	°C
T_j	Maximum junction temperature	125	°C
T_{stg}	Storage temperature range	-65 to +150	°C

APPLICATION CIRCUIT

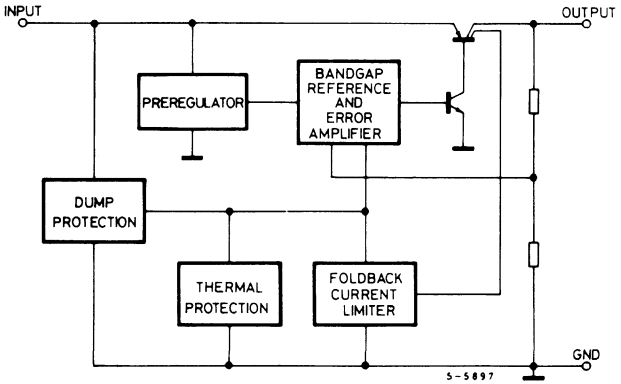


LM2930A

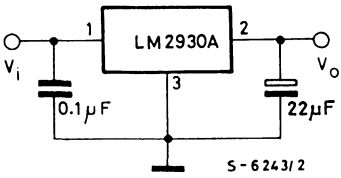
CONNECTION DIAGRAM
(top view)



BLOCK DIAGRAM



TEST AND APPLICATION CIRCUIT



The output capacitor is required for stability. Though the 47μF shown is the minimum recommended value, actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) also factors in the IC stability. Since ESR varies from one brand to the next, some bench work may be required to determine the minimum capacitor value to use in production. Worst-case is usually determined at the minimum ambient temperature and maximum load expected.

Output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltages during brief conditions of negative input transients that might be characteristic of a particular system.

Capacitors must also be rated at all ambient temperature expected in the system. Many aluminum type electrolytics will freeze at temperatures less than -30°C, reducing their effective capacitance to zero. To maintain regulator stability down to -40°C, capacitors rated at that temperature (such as tantalums) must be used.

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

ELECTRICAL CHARACTERISTICS (V_i = 14.4V, I_o = 150mA, T_j = 25°C unless otherwise specified).

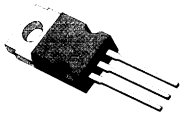
Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output voltage	$6V \leq V_i \leq 26V$, $5mA \leq I_o \leq 150mA$ $-40°C \leq T_j \leq +125°C$	4.5	5	5.5	V
ΔV_o	Line regulation	$9V \leq V_i \leq 16V$, I_o = 5mA		7	25	mV
		$6V \leq V_i \leq 26V$, I_o = 5mA		30	80	mV
ΔV_o	Load regulation	$5mA \leq I_o \leq 150mA$		14	50	mV
R_o	Output impedance	$100mA_{DC}$ & 10mArms, 100Hz - 10KHz		200		mΩ
I_d	Quiescent current	I_o = 10mA I_o = 150mA		4 18	7 40	mA mA
e_N	Output noise voltage	10Hz - 100KHz		140		μVrms
	Long term stability			20		mV/ 1000 hr
SVR	Supply voltage rejection	f_o = 120Hz		56		dB
I_o	Current limit			650		mA
V_i-V_o	Dropout voltage	I_o = 150mA I_o = 400mA		0.2 0.4	0.5	V V

LM2931A

VERY LOW DROP VOLTAGE REGULATOR

- VERY LOW QUIESCENT CURRENT
- OUTPUT CURRENT IN EXCESS OF 400mA
- INPUT/OUTPUT DROP TYP. 0.2V AT 150mA
- REVERSE POLARITY PROTECTION
- 60V LOAD DUMP PROTECTION
- -60V TRANSIENT PROTECTION
- OVERVOLTAGE PROTECTION
- FOLDBACK CURRENT LIMITING
- THERMAL SHUTDOWN

The LM2931A is an improved version of the LM2931 5V voltage regulator which features an output current rating of 400mA with a dropout voltage of typically 0.4V. At 150mA the dropout voltage falls to 0.2V. A special feature of this device is the low quiescent current of 2mA at 10mA output current which makes it ideal for standby at backup applications. Designed for automotive applications, the LM2931A protects itself and the load from ± 60V load dump transients, abttery reversal and input overvoltage. It also includes a thermal shutdown circuit and a foldback current limiter. The low voltage drop of the LM2931A allows correct operation of 5V automotive equipment during starting when the battery voltage can fall below 6V. The LM2931A is available in a TO-220 plastic power package.



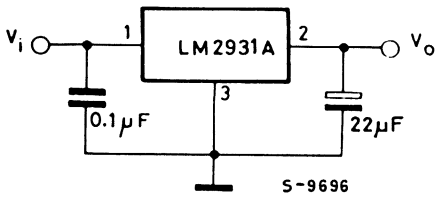
TO-220

ORDERING NUMBER: LM2930A

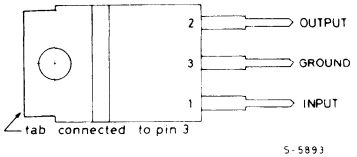
ABSOLUTE MAXIMUM RATINGS

V_i	Forward input voltage	26	V
	Overvoltage protection (t = 100ms)	± 60	V
T_{op}	Operating temperature range	-40 to +85	°C
T_j	Maximum junction temperature	125	°C
T_{stg}	Storage temperature range	-65 to +150	°C

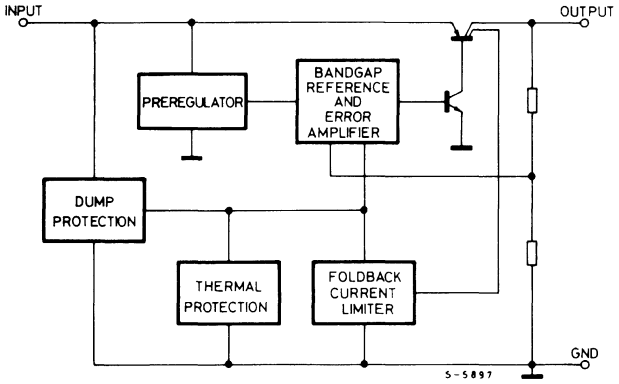
APPLICATION CIRCUIT



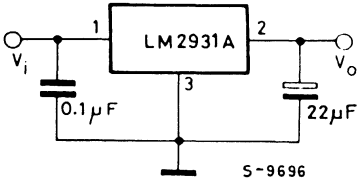
CONNECTION DIAGRAM
(top view)



BLOCK DIAGRAM



TEST AND APPLICATION CIRCUIT



The output capacitor is required for stability. Though the 47μF shown is the minimum recommended value, actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) also factors in the IC stability. Since ESR varies from one brand to the next, some bench work may be required to determine the minimum capacitor value to use in production. Worst-case is usually determined at the minimum ambient temperature and maximum load expected.

Output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltages during brief conditions of negative input transients that might be characteristic of a particular system.

Capacitors must also be rated at all ambient temperature expected in the system. Many aluminum type electrolytics will freeze at temperatures less than -30°C, reducing their effective capacitance to zero. To maintain regulator stability down to -40°C, capacitors rated at that temperature (such as tantalums) must be used.

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	4	°C/W

ELECTRICAL CHARACTERISTICS (V_i = 14.4V, I_o = 10mA, T_j = 25°C unless otherwise specified).

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output voltage	$6V \leqslant V_i \leqslant 26V$, $I_o \leqslant 150$ mA $-40°C \leqslant T_j \leqslant +125°C$	4.75	5	5.25	V
ΔV_o	Line regulation	$9V \leqslant V_i \leqslant 16V$		2	10	mV
		$6V \leqslant V_i \leqslant 26V$		4	30	mV
ΔV_o	Load regulation	$5mA \leqslant I_o \leqslant 150mA$		14	50	mV
R_o	Output impedance	$100mA_{DC}$ & 10mArms, 100Hz - 10KHz		200		mΩ
I_d	Quiescent current	I_o = 10mA $6V \leqslant V_i \leqslant 26V$ $-40°C \leqslant T_j \leqslant +125°C$ I_o = 150mA, V_i = 14V, T_j = 25°C		0.8 20	2 40	mA mA
e_N	Output noise voltage	10Hz - 100KHz		500		μVrms
	Long term stability			20		mV/ 1000 hr
SVR	Supply voltage rejection	f_o = 120Hz		80		dB
V_i-V_o	Dropout voltage	I_o = 10mA I_o = 150mA I_o = 400mA		0.05 0.2 0.4	0.1 0.4	V V V
I_o	Current limit			650		mA

LM2935

LOW DROPOUT DUAL REGULATOR

- TWO REGULATED OUTPUTS
- OUTPUT CURRENT IN EXCESS OF 750mA
- LOW QUIESCENT CURRENT STANDBY REGULATOR
- INPUT-OUTPUT DIFFERENTIAL LESS THAN 0.6V AT 0.5A
- REVERSE BATTERY PROTECTION
- 60V LOAD DUMP PROTECTION
- -50V REVERSE TRANSIENT PROTECTION
- SHORT CIRCUIT PROTECTION
- THERMAL OVERLOAD PROTECTION
- ON/OFF SWITCH FOR HIGH CURRENT OUTPUT
- RESET ERROR FLAG

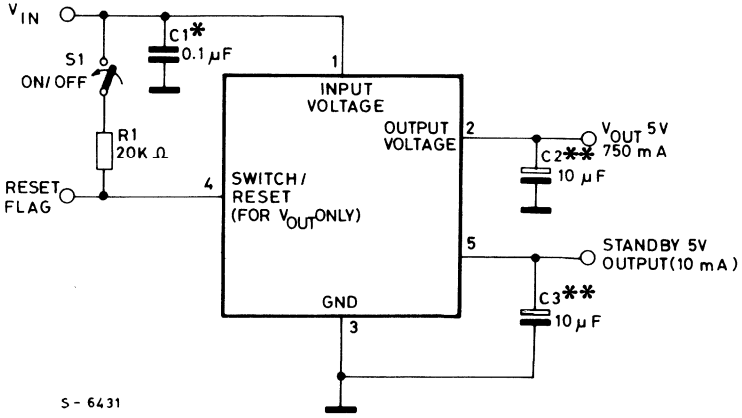
The LM2935 positive voltage regulator in Pentawatt® package features a low quiescent current of 3 mA or less when supplying 10 mA loads from the standby regulator output. This unique characteristic and the extremely low input-output differential required for proper regulation (0.55V for output currents of 10 mA) make the LM2935 the ideal regulator for power systems that include standby memory. Applications include processor power supplies demanding as much as 750 mA of output current.

Designed primarily for automotive applications, the LM2935 and all regulated circuitry are protected from reverse battery installations or 2 battery jumps. During line transients, such as a load dump (60V) when the input voltage to the regulator can momentarily exceed the specified maximum operating voltage, the 0.75A regulator will automatically shut down to protect both internal circuits and the load while the standby regulator will continue to power any standby load. The LM2935 cannot be harmed by temporary mirror-image insertion. Familiar regulator features such as short circuit and thermal overload protection are also provided.

Pentawatt®

ORDERING NUMBER: LM2935

TEST CIRCUIT



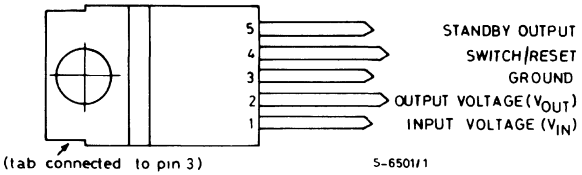
* Required if regulator is located far from power supply filter.

** Required for stability. May be increased without bound. Capacitor must be rated to operate at the minimum temperature expected for the regulator system.

ABSOLUTE MAXIMUM RATINGS

V_i	DC input voltage	26	V
	Transient overvoltage protection	60	V
V_i	Reverse polarity input voltage (DC)	-15	V
V_i	Reverse polarity input voltage (transient)	-50	V
P_{tot}	Total power dissipation	internally limited	
T_{op}	Operating junction temperature	-40 to 125	°C
T_{stg}, T_j	Storage and junction temperature	-55 to 150	°C

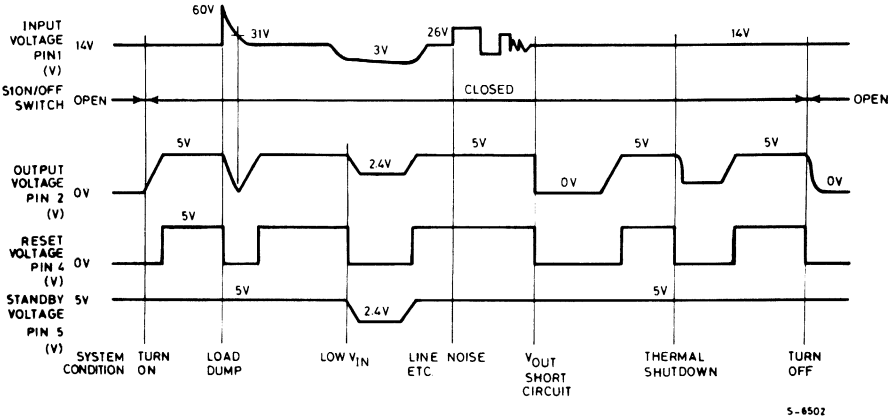
CONNECTION DIAGRAM (top view)



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50	°C/W

TYPICAL CIRCUIT WAVEFORMS



ELECTRICAL CHARACTERISTICS FOR V_O (V_i = 14V, I_O = 500 mA, T_j = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_O	Output voltage (pin 2)	$6V \leqslant V_i \leqslant 26V$, $I_O \leqslant 500$ mA T_j = -40 +125°C	4.75	5	5.25	V
ΔV_O	Line regulation	$9V \leqslant V_i \leqslant 16V$, I_O = 5 mA		4	25	mV
		$6V \leqslant V_i \leqslant 26V$, I_O = 5 mA		10	50	mV
ΔV_O	Load regulation	$5\text{ mA} \leqslant I_O \leqslant 500\text{ mA}$		10	50	mV
R_O	Output impedance	500 mA DC and 10 mA rms 10 Hz to 100 KHz		200		mΩ
I_q	Quiescent current	$I_O \leqslant 10$ mA, No load on standby		3		mA
		I_O = 500 mA, No load on standby		55	100	mA
		I_O = 750 mA, No load on standby		120		mA
e_N	Output noise voltage	10 Hz to 100 KHz		100		μVrms
	Long term stability			20		$\frac{mV}{1000hr}$
SVR	Ripple rejection	f = 120 Hz		66		dB

ELECTRICAL CHARACTERISTICS FOR V_O (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_i-V_o	Dropout voltage	I_o = 500 mA I_o = 750 mA		0.45 0.82	0.6	V V
I_L	Current limit		0.75	1.4		A
V_R	Reset output voltage Low	R1 = 20 KΩ, V_i = 4.5V		0.8	1	V
	High	R1 = 20 KΩ, V_i = 14V	4.5	5	5.5	V
I_R	Reset output current	V_i = 4.5V, reset in low state		5		mA
R1	ON/OFF resistor			20	30	KΩ

ELECTRICAL CHARACTERISTICS FOR STANDBY OUTPUT (V_i = 14V, I_o = 10 mA, T_j = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_o	Output voltage (pin 5)	$I_o \leqslant$ 10 mA, T_j = -40 + 125°C 6V $\leqslant V_i \leqslant$ 26V	4.75	5	5.25	V
V_T	Tracking	V_o - Standby output voltage		50	200	mV
ΔV_o	Line regulation	6V $\leqslant V_i \leqslant$ 26V		4	50	mV
ΔV_o	Load regulation	1 mA $\leqslant I_o \leqslant$ 10 mA		10	50	mV
R_o	Output impedance	10 mA DC and 1 mA rms 100 Hz - 10 KHz		1		Ω
I_q	Quiescent current	$I_o \leqslant$ 10 mA, T_j = -40 +125°C V_o = OFF		2	3	mA
e_N	Output noise voltage	10 Hz to 100 KHz		300		μV
	Long term stability			20		$\frac{mV}{1000hr}$
SVR	Ripple rejection	f = 120 Hz		66		dB
V_i-V_o	Dropout voltage	$I_o \leqslant$ 10 mA		0.55	0.7	V
I_L	Current limit		25	70		mA

Fig. 1 - Dropout voltage (V_o)

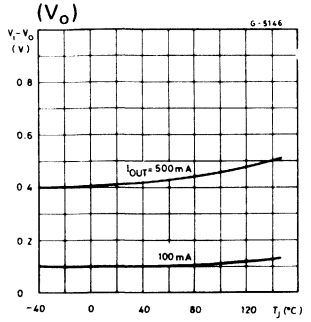


Fig. 2 - Dropout voltage (V_o)

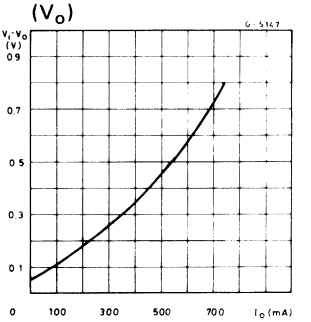


Fig. 3 - Dropout voltage (V_{STBY})

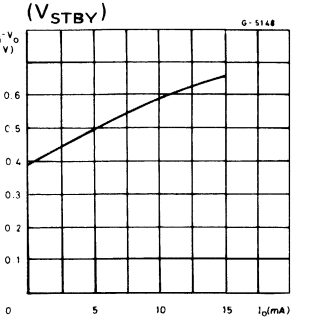


Fig. 4 - Low voltage behavior

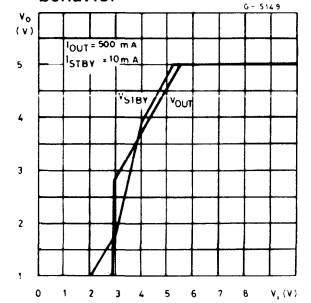


Fig. 5 - Line transient response (V_o)

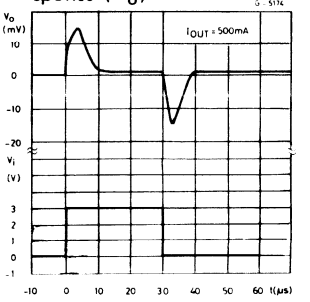


Fig. 6 - Line transient response (V_{STBY})

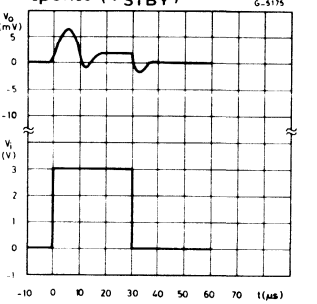


Fig. 7 - Load transient response (V_o)

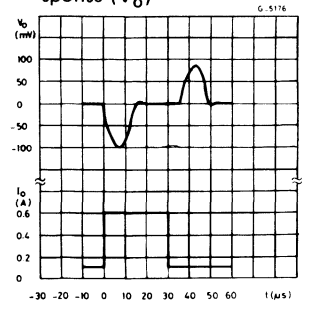


Fig. 8 - Load transient response (V_{STBY})

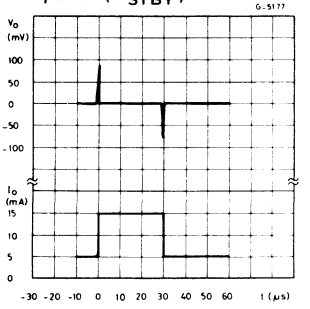


Fig. 9 - Quiescent current (V_o)

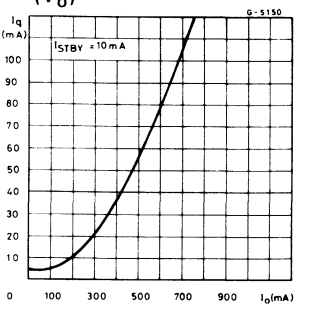


Fig. 10 - Quiescent current (V_{STBY})

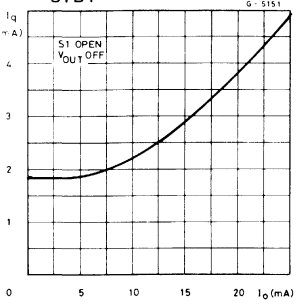


Fig. 11 - Quiescent current (V_O)

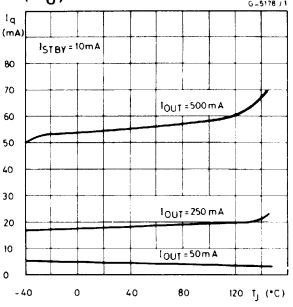


Fig. 12 - Quiescent current (V_{STBY})

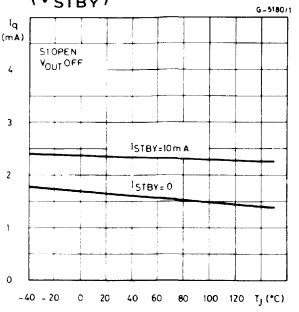


Fig. 13 - Quiescent current (V_{STBY})

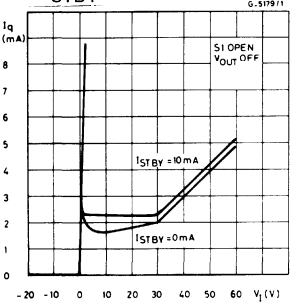


Fig. 14 - Ripple rejection

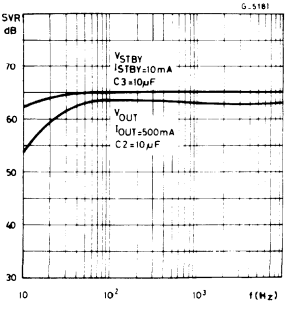


Fig. 15 - Ripple rejection (V_O)

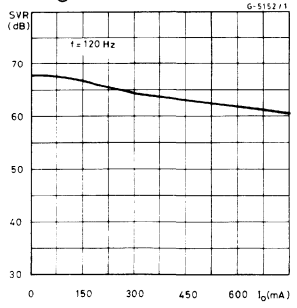


Fig. 16 - Ripple rejection (V_{STBY})

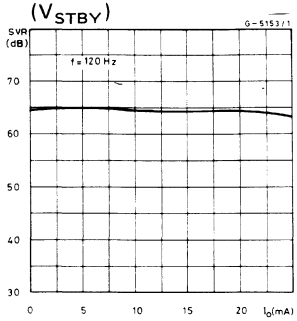


Fig. 17 - Output impedance

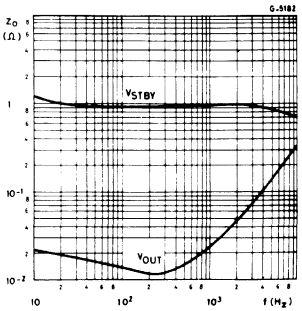
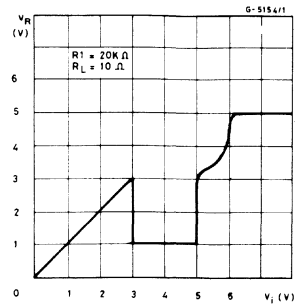


Fig. 18 - Reset on startup



APPLICATION INFORMATION

EXTERNAL CAPACITORS

The LM2935 output capacitors are required for stability. Without them, the regulator outputs will oscillate, sometimes by many volts. Though the 10 μF shown are the minimum recommended values, actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) also factors in the IC stability. Since ESR varies from one brand to the next, some bench work may be required to determine the minimum capacitor value to use in production. Worst-case is usually determined at the minimum ambient temperature and maximum load expected.

Output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltages during brief conditions of negative input transients that might be characteristic of a particular system.

Capacitors must also be rated at all ambient temperatures expected in the system. Many aluminum type electrolytics will freeze at temperatures less than -30°C, reducing their effective capacitance to zero. To maintain regulator stability down to -40°C, capacitors rated at that temperature (such as tantalums) must be used.

No capacitor must be attached to the ON/OFF and ERROR FLAG pin due to the internal circuits of the IC.

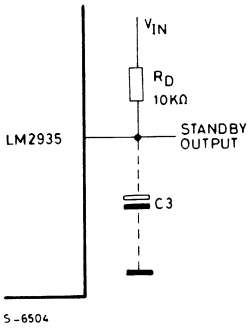
STANDBY OUTPUT

The LM2935 differs from most fixed voltage regulators in that it is equipped with two regulator outputs instead of one. The additional output is intended for use in systems requiring standby memory circuits. While the high current regulator output can be controlled with the ON/OFF pin described below, the standby output remains on under all conditions as long as sufficient input voltage is applied to the IC. Thus, memory and other circuits powered by this output remain unaffected by positive line transients, thermal shutdown, etc.

The standby regulator circuit is designed so that the quiescent current to the IC is very low (< 3 mA) when the other regulator output is off.

In applications where the standby output is not needed, it may be disabled by connecting a resistor from the standby output to the supply voltage. This eliminates the need for a more expensive capacitor on the output to prevent unwanted oscillations. The value of the resistor depends upon the minimum input voltage expected for a given system. Since the standby output is shunted with an internal 5.7V zener, the current through the external resistor should be sufficient to bias the circuit. Approximately 60 μA will suffice, resulting in a 10kΩ external resistor for most applications (Fig. 19).

Fig. 19 - Disabling standby output to eliminate C3



HIGH CURRENT OUTPUT

Unlike the standby regulated output, which must remain on whenever possible, the high current regulated output is fault protected against overvoltage and also incorporates thermal shutdown. If the input voltage rises above approximately 30V (e.g. load dump), this output will automatically shutdown. This protects the internal circuitry and enables the IC to survive higher voltage transients than would otherwise be expected. Thermal shutdown is effective against die overheating since the high current output is the dominant source of power dissipation in the IC.

ON/OFF AND ERROR FLAG PIN

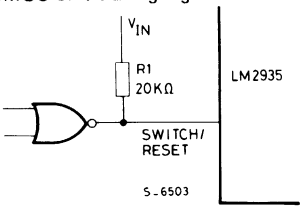
This pin has the ability to serve a dual purpose if desired. When controlled in the manner shown in the test circuit (common in automotive systems

APPLICATION INFORMATION (continued)

where S1 is the ignition switch), the pin also serves as an output flag that is active low whenever a fault condition is detected with the high current regulated output. In other words, under normal operating conditions the output voltage of this pin is high (5V). This is set by an internal clamp. If the high current output becomes unregulated for any reason (line transients, short circuit, thermal shutdown, low input voltage, etc.) the pin switches to the active low state, and is capable of sinking several milliamps. This output signal can be used to initiate any reset or start-up procedure that may be required of the system.

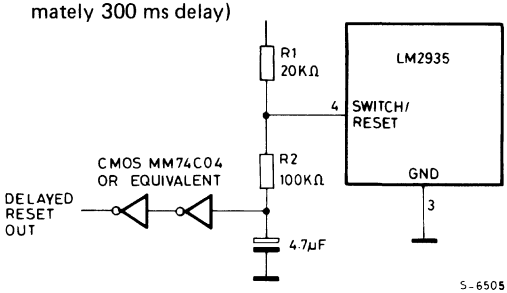
The ON/OFF pin can also be driven directly from logic circuits. The only requirement is that the 20 kΩ pull-up resistor remain in place (Fig. 20).

Fig. 20 - Controlling ON/OFF terminal with a typical CMOS or TTL logic gate



This will not affect the logic gate since the voltage on this pin is limited by the internal clamp in the LM2935 to 5V. The error flag is sacrificed in this arrangement since the maximum sink capability of the pin in the active low state (approximately 5 mA) is usually not sufficient to pull down the active high logic gate. Of course, the flag can be retained if the driving gate is open collector logic.

Fig. 21 - Reset pulse on power-up (with approximately 300 ms delay)

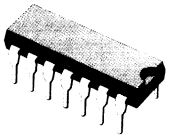


LM3045
LM3046

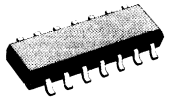
FIVE TRANSISTOR ARRAYS

- TWO MATCHED PAIRS OF TRANSISTORS:
  - V_{BE} MATCHED 5mV
  - INPUT OFFSET CURRENT 2μA
- FIVE GENERAL PURPOSE MONOLITHIC TRANSISTORS
- OPERATION FROM DC TO 120MHz
- WIDE OPERATING CURRENT RANGE
- LOW NOISE
- FULL MILITARY TEMPERATURE RANGE (LM3045)-55 TO + 125°C
- DIRECT REPLACEMENT FOR CA3045/6 AND TBA331

The LM3045 and LM3046, consist of five general purpose silicon NPN transistors' on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair. The transistors are well suited to a wide variety of applications in low power system in the DC thruogh VHF range. They may be used as directe transistors in conventional circuits however, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching. The LM3045 is supplied in a 14-lead dual-in-line ceramic package rated for operation over the full military temperature range. The LM3046 is electrically identical to the LM3045 but for applications requiring only a limited temperature range.



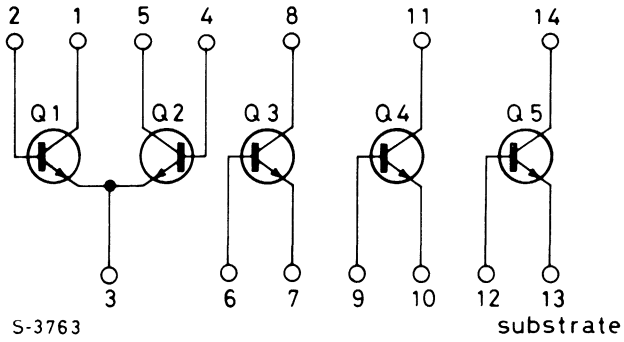
DIP-14
(Plastic and Ceramic)



SO-14

ORDERING NUMBERS: LM3045J (Ceramic)
LM3046N (Plastic)
LM3046J (Ceramic)
LM3046D (Micropackage)

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		LM3045		LM3046	
		Each Transistor	Total Package	Each Transistor	Total Package
P_{tot}	Total power dissipation at T_{amb} = 25°C (DIP)	300mW	750mW	300mW	750mW
	(Micropackage)			250mW	500mW
V_{CEO}	Collector-emitter voltage	15V		15V	
V_{CBO}	Collector-base voltage	20V		20V	
V_{CSS}*	Collector-substrate voltage	20V		20V	
V_{EBO}	Emitter-base voltage	5V		5V	
I_C	Collector current	50mA		50mA	
T_{op}	Operating temperature	-55 to + 125°C		-40 to + 85°C	
T_{stg}	Storage temperature	-65 to + 150°C		-65 to + 150°C	

(*) The collector of each transistor is isolated from the substrate by an integrated diode. The substrate (pin 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

THERMAL DATA

			DIP-14		SO-14
			Each	Total	
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max.	315°C/W	126°C/W	200°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_{CBO}	Collector cutoff current (I_E = 0)	V_{CB} = 10 V		0.002	40	nA
I_{CEO}	Collector cutoff current (I_B = 0)	V_{CE} = 10 V		see curve	0.5	μA
$\lvert I_{B1}-I_{B2}\rvert$	Input offset current	I_C = 1 mA V_{CE} = 3 V		0.3	2	μA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
h_{FE}	DC current gain	I_C = 10 mA V_{CE} = 3 V		100		–
		I_C = 1 mA V_{CE} = 3 V	40	100		–
		I_C = 10 μA V_{CE} = 3 V		54		–
f_T	Transition frequency	I_C = 3 mA V_{CE} = 3 V	300	550		MHz
NF	Noise figure	I_C = 100 μA V_{CE} = 3 V f = 1 KHz R_g = 1 kΩ		3.25		dB
H_{ie}	Input impedance	I_C = 1 mA V_{CE} = 3 V f = 1 kHz		3.5		kΩ
h_{fe}	Forward current transfer ratio	I_C = 1 mA V_{CE} = 3 V f = 1 kHz		110		–
h_{re}	Reverse voltage transfer ratio	I_C = 1 mA V_{CE} = 3 V f = 1 kHz		1.8×10^{-4}		–
h_{oe}	Output admittance	I_C = 1 mA V_{CE} = 3V f = 1 kHz		15.6		μS
y_{ie}	Input admittance	I_C = 1 mA V_{CE} = 3 V f = 1 MHz		0.3+j0.04		mS
y_{fe}	Forward transadmittance	I_C = 1 mA V_{CE} = 3 V f = 1 MHz		31-j1.5		mS
y_{re}	Reverse transadmittance	I_C = 1 mA V_{CE} = 3 V f = 1 MHz		see curve		mS

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{CBO}	Collector-base breakdown voltage (I_E = 0)	I_C = 10 μA	20	60		V
V_{CEO}	Collector-emitter brealdown voltage (I_B = 0)	I_C = 1 mA	15	24		V
V_{CSS}	collector-substrate breakdown voltage (I_{CSS} = 0)	I_C = 10 μA	20	60		V
$V_{CE\ (sat)}$	Collector-emitter saturation voltage	I_B = 1 mA I_C = 10 mA		0.23		V
V_{EBO}	Emitter-base breakdown voltage (I_C = 0)	I_E = 10 μA	5	7		V
V_{BE}	Base-emitter voltage	I_E = 1 mA V_{CE} = 3 V I_E = 10 mA V_{CE} = 3 V		0.715 0.8		V V
$\lvert V_{BE1}-V_{BE2}\rvert$	Input offset voltage	I_C = 1 mA V_{CE} = 3 V		0.45	5	mV
$\lvert V_{BE3}-V_{BE4}\rvert$	Input offset voltage	I_C = 1 mA V_{CE} = 3 V		0.45	5	mV
$\lvert V_{BE4}-V_{BE5}\rvert$	Input offset voltage	I_C = 1 mA V_{CE} = 3 V		0.45	5	mV
$\lvert V_{BE5}-V_{BE4}\rvert$	Input offset voltage	I_C = 1 mA V_{CE} = 3 V		0.45	5	mV
$\frac{\Delta V_{BE}}{\Delta T}$	Base-emitter voltage temperature coefficient	I_C = 1 mA V_{CE} = 3 V		-1.9		mV/°C
$\frac{\lvert V_{BE1}-V_{BE2}\rvert}{\Delta T}$	Input offset voltage temperature coefficient	I_C = 1 mA V_{CE} = 3 V		1.1		μV/°C

ELECTRICAL CHARACTERISTICS (continued)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit.
Y_{oe}	Output admittance	I_C = 1 mA V_{CE} = 3 V f = 1 MHz		0.001+j0.03		mS
C_{EBO}	Emitter-base capacitance	I_C = 0 V_{EB} = 3 V		0.6		pF
C_{CBo}	Collector-base capacitance	I_E = 0 V_{CB} = 3 V		0.58		pF
C_{CSS}	Collector-sustrate capacitance	I_C = 0 V_{CSS} = 3 V		2.8		pF

Fig. 1 - Collector-base cutoff current vs. temperature for each transistors

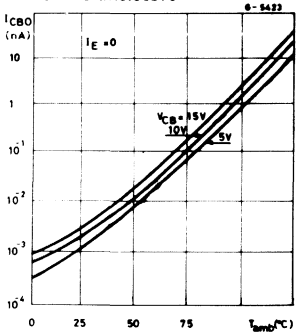


Fig. 2 - Collector-emitter cutoff current vs. temperature for each transistors

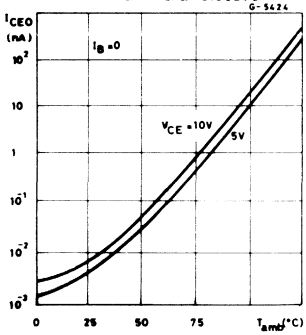


Fig. 3 - DC current gain vs. emitter current

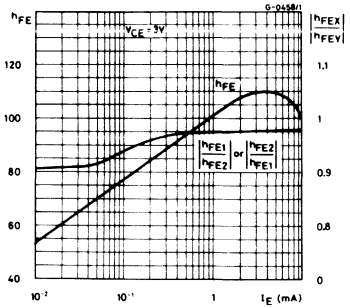


Fig. 4 - Input voltage and input offset voltage vs. emitter current

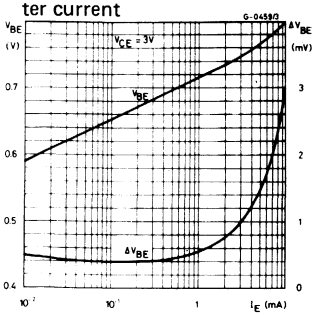


Fig. 5 - Input characteristic for each transistor

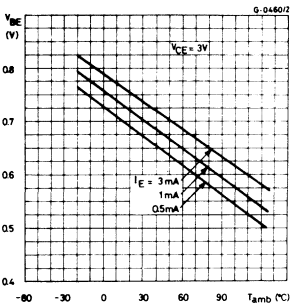


Fig. 6 - Input offset voltage vs. ambient temperature

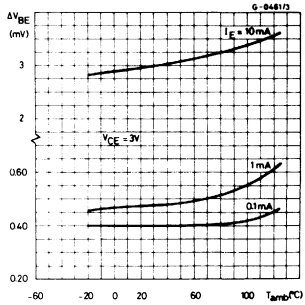


Fig. 7 - Input offset current for matched transistor pair

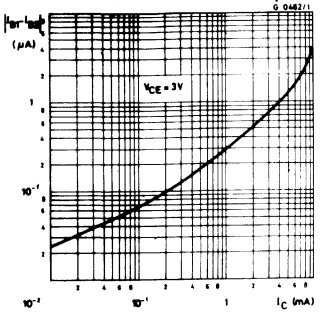


Fig. 8 - Forward admittance

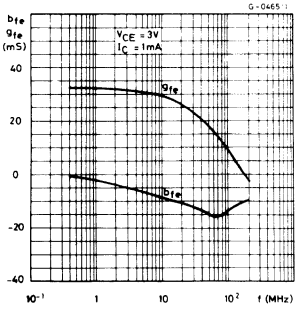


Fig. 9 - Input admittance

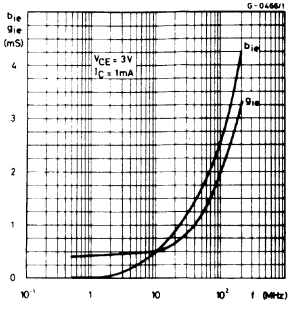


Fig. 10 - Output admittance

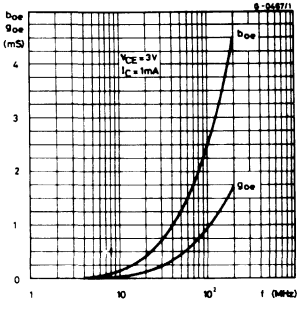


Fig. 11 - Reverse admittance

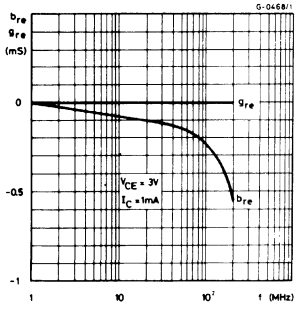


Fig. 12 - Gain-bandwidth vs. collector current

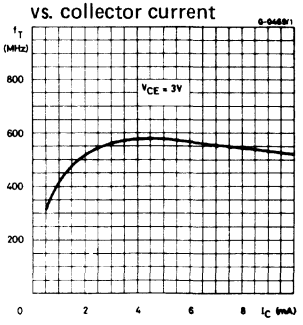


Fig. 13 - Noise figure vs. collector current

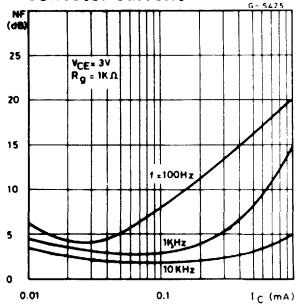
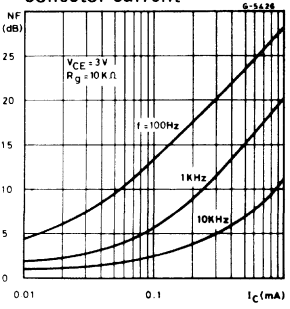


Fig. 14 - Noise fugure vs. collector current



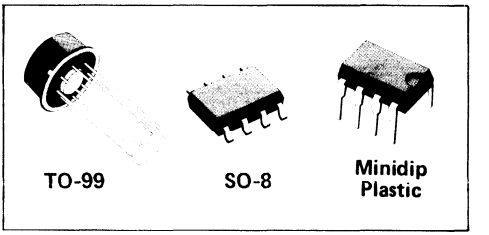
LS204

HIGH PERFORMANCE DUAL OPERATIONAL AMPLIFIER

- SINGLE OR SPLIT SUPPLY OPERATION
- LOW POWER CONSUMPTION
- SHORT CIRCUIT PROTECTION
- LOW DISTORTION, LOW NOISE
- HIGH GAIN-BANDWIDTH PRODUCT
- HIGH CHANNEL SEPARATION

The LS204 is a high performance dual operational amplifier with frequency and phase compensation built into the chip. The internal phase compensation allows stable operation as voltage follower in spite of its high gain-bandwidth products.

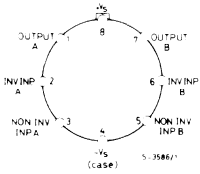
The circuit presents very stable electrical characteristics over the entire supply voltage range, and it particularly intended for professional and telecom applications (active filters, etc).

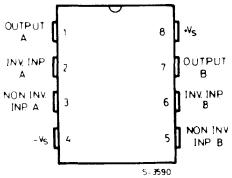


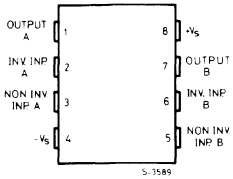
ABSOLUTE MAXIMUM RATINGS			TO-99	Minidip	μpackage
V_s	Supply voltage			± 18V	
V_i	Input voltage			± V_s	
V_i	Differential input voltage			± (V_s - 1)	
T_{op}	Operating temperature for	**LS 204**		-25 to 85°C	
		LS 204A		-55 to 125°C	
		LS 204C		0 to 70 °C	
P_{tot}	Power dissipation at T_{amb} = 70°C		520 mW	665 mW	400 mW
T_j	Junction temperature		150°C	150°C	150°C
T_{stg}	Storage temperature		-65 to 150°C	-55 to 150°C	-55 to 150°C

LS204

CONNECTION DIAGRAMS AND ORDERING NUMBERS
(top views)

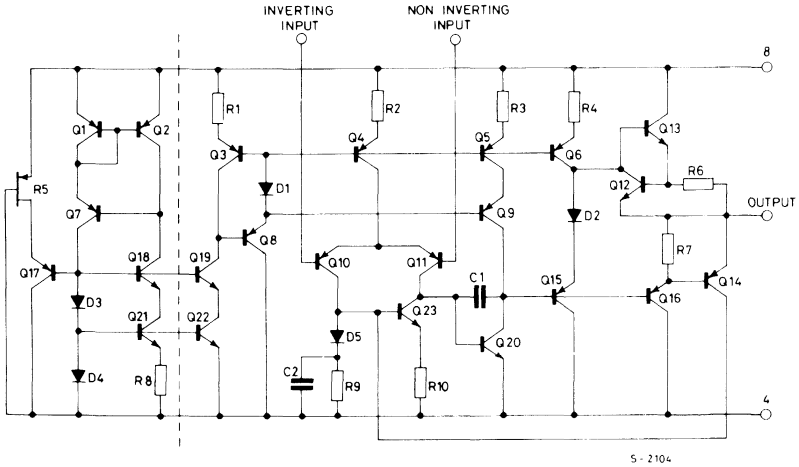






Type	TO-99	Minidip	SO-8
LS 204	LS 204 TB	—	LS 204 M
LS 204 A	LS 204 ATB	—	—
LS 204 C	LS 204 CTB	LS 204 CB	LS 204 CM

SCHEMATIC DIAGRAM (one section)



THERMAL DATA		TO-99	Minidip	SO-8
$R_{th\ j\text{-}amb}$ Thermal resistance junction-ambient	max	155 °C/W	120 °C/W	200 °C/W

ELECTRICAL CHARACTERISTICS (V_s= ± 15V, T_{amb}= 25°C, unless otherwise specified)

Parameter		Test conditions	LS 204/LS204A			LS 204C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_s	Supply current			0.7	1		0.8	1.5	mA
I_b	Input bias current			50	150		100	300	nA
		$T_{min} < T_{op} < T_{max}$			300			700	nA
R_i	Input resistance	f = 1 KHz		1			0.5		MΩ
V_{os}	Input offset voltage	$R_g \leq 10$ KΩ		0.5	2.5		0.5	3.5	mV
		$R_g \leq 10$ KΩ $T_{min} < T_{op} < T_{max}$			3.5			5	mV
$\frac{\Delta V_{os}}{\Delta T}$	Input offset voltage drift	R_g = 10 KΩ $T_{min} < T_{op} < T_{max}$		5			5		µV/°C
I_{os}	Input offset current			5	20		12	50	nA
		$T_{min} < T_{op} < T_{max}$			40			100	nA
$\frac{\Delta I_{os}}{\Delta T}$	Input offset current drift	$T_{min} < T_{op} < T_{max}$		0.08			0.1		$\frac{nA}{°C}$
I_{sc}	Output short circuit current			23			23		mA
G_v	Large signal open loop voltage gain	$T_{min} < T_{op} < T_{max}$ R_L= 2KΩ V_s= ±15V V_s= ± 4V	90	100 95		86	100 95		dB
B	Gain-bandwidth product	f = 20 KHz	1.8	3		1.5	2.5		MHz
e_N	Total input noise voltage	f = 1 KHz R_g = 50Ω R_g = 1 KΩ R_g = 10 KΩ		8 10 18	15		10 12 20		$\frac{nV}{\sqrt{Hz}}$
d	Distortion	G_v= 20 dB R_L= 2KΩ V_o= 2 Vpp f = 1 KHz		0.03	0.1		0.03	0.1	%
V_o	DC output voltage swing	R_L= 2KΩ V_s= ±15V V_s= ± 4V	±13	±3		±13	±3		V
V_o	Large signal voltage swing	R_L= 10 KΩ f = 10 KHz		28			28		Vpp
SR	Slew rate	unity gain R_L= 2KΩ	0.8	1.5			1		V/µs
CMR	Common mode rejection	V_i= 10V $T_{min} < T_{op} < T_{max}$	90			86			dB
SVR	Supply voltage rejection	V_i= 1V f = 100 Hz $T_{min} < T_{op} < T_{max}$	90			86			dB
CS	Channel separation	f = 1 KHz	100	120			120		dB

Note:

	LS 204	LS 204A	LS 204C
$T_{min.}$	-25°C	-55°C	0°C
$T_{max.}$	+85°C	+125°C	+70°C

Fig. 1 - Supply current vs. supply voltage

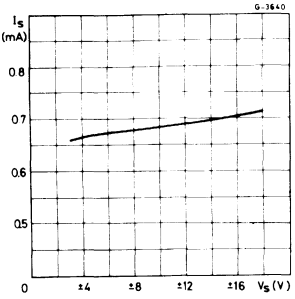


Fig. 2 - Supply current vs. ambient temperature

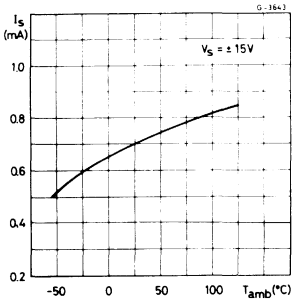


Fig. 3 - Output short circuit current vs. ambient temperature

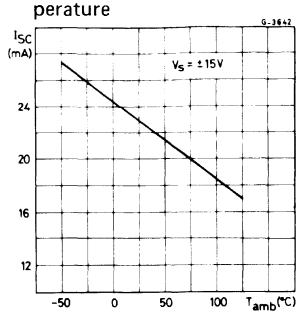


Fig. 4 - Open loop frequency and phase response

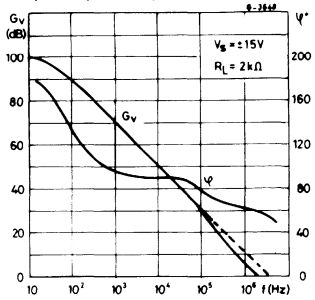


Fig. 5 - Open loop gain vs. ambient temperature

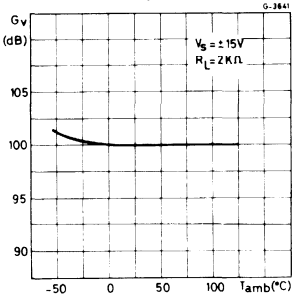


Fig. 6 - Supply voltage rejection vs. frequency

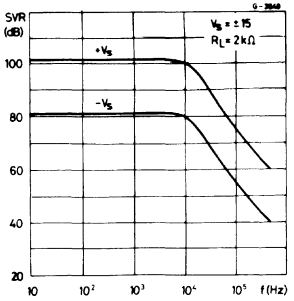


Fig. 7 - Large signal frequency response

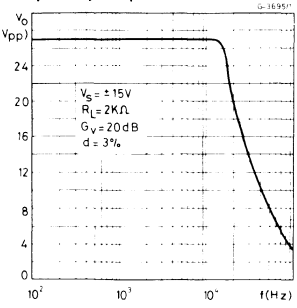


Fig. 8 - Output voltage swing vs. load resistance

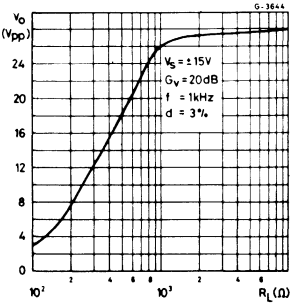
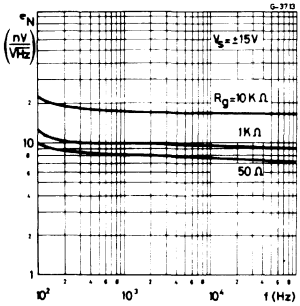


Fig. 9 - Total input noise vs. frequency



APPLICATION INFORMATION

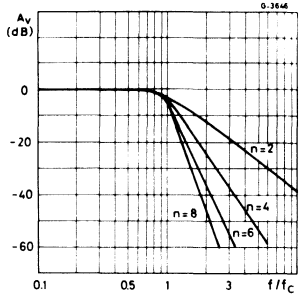
Active low-pass filter:

BUTTERWORTH

The Butterworth is a "maximally flat" amplitude response filter. Butterworth filters are used for filtering signals in data acquisition systems to prevent aliasing errors in sampled-data applications and for general purpose low-pass filtering.
The cutoff frequency, f_c, is the frequency at which the amplitude response is down 3 dB. The attenuation rate beyond the cutoff frequency is -n6 dB per octave of frequency where n is the order (number of poles) of the filter.
Other characteristics:

- Flattest possible amplitude response.
- Excellent gain accuracy at low frequency end of passband

Fig. 10 - Amplitude response



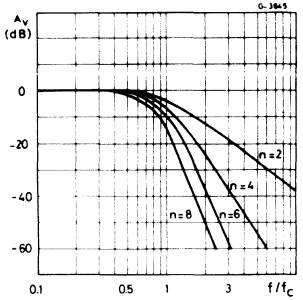
BESSEL

The Bessel is a type of "linear phase" filter. Because of their linear phase characteristics, these filters approximate a constant time delay over a limited frequency range. Bessel filters pass transient waveforms with a minimum of distortion. They are also used to provide time delays for low pass filtering of modulated waveforms and as a "running average" type filter.

The maximum phase shift is $\frac{-n\pi}{2}$ radians where n is the order (number of poles) of the filter. The cutoff frequency, f_c, is defined as the frequency at which the phase shift is one half of this value. For accurate delay, the cutoff frequency should be twice the maximum signal frequency. The following table can be used to obtain the -3 dB frequency of the filter.

	2 pole	4 pole	6 pole	8 pole
-3 dB frequency	0.77 f_c	0.67 f_c	0.57 f_c	0.50 f_c

Fig. 11 - Amplitude response



Other characteristics:

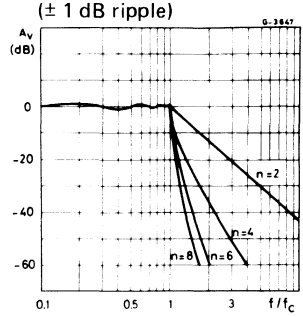
- Selectivity not as great as Chebyschev or Butterworth.
- Very little overshoot response to step inputs
- Fast rise time.

CHEBYSCHEV

Chebyschev filters have greater selectivity than either Bessel or Butterworth at the expense of ripple in the passband.
Chebyschev filters are normally designed with peak-to-peak ripple values from ± 0.2 dB to ± 2 dB.
Increased ripple in the passband allows increased attenuation above the cutoff frequency.
The cutoff frequency is defined as the frequency at which the amplitude response passes through the specified maximum ripple band and enters the stop band.
Other characteristics:

- Greater selectivity
- Very nonlinear phase response
- High overshoot response to step inputs

Fig. 12 - Amplitude response (± 1 dB ripple)



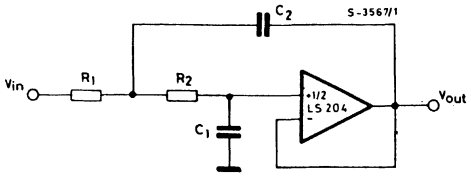
APPLICATION INFORMATION (continued)

The table below shows the typical overshoot and settling time response of the low pass filters to a step input.

	NUMBER OF POLES	PEAK OVERSHOOT	SETTLING TIME (% of final value)		
		% Overshoot	± 1%	± 0.1%	± 0.01%
BUTTERWORTH	2	4	$1.1/f_c$ sec.	$1.7/f_c$ sec.	$1.9/f_c$ sec.
	4	11	$1.7/f_c$	$2.8/f_c$	$3.8/f_c$
	6	14	$2.4/f_c$	$3.9/f_c$	$5.0/f_c$
	8	16	$3.1/f_c$	$5.1\ f_c$	$7.1/f_c$
BESSEL	2	0.4	$0.8/f_c$	$1.4/f_c$	$1.7/f_c$
	4	0.8	$1.0/f_c$	$1.8/f_c$	$2.4/f_c$
	6	0.6	$1.3/f_c$	$2.1/f_c$	$2.7/f_c$
	8	0.3	$1.6/f_c$	$2.3/f_c$	$3.2/f_c$
CHEBYSCHEV (RIPPLE ± 0.25 dB)	2	11	$1.1/f_c$	$1.6/f_c$	-
	4	18	$3.0/f_c$	$5.4/f_c$	-
	6	21	$5.9/f_c$	$10.4/f_c$	-
	8	23	$8.4/f_c$	$16.4/f_c$	-
CHEBYSCHEV (RIPPLE ± 1 dB)	2	21	$1.6/f_c$	$2.7/f_c$	-
	4	28	$4.8/f_c$	$8.4/f_c$	-
	6	32	$8.2/f_c$	$16.3/f_c$	-
	8	34	$11.6/f_c$	$24.8/f_c$	-

Design of 2nd order active low pass filter
(Sallen and Key configuration unity gain op-amp)

Fig. 13 - Filter configuration



$$\frac{V_o}{V_i} = \frac{1}{1 + 2\xi\frac{S}{\omega_c} + \frac{S^2}{\omega_c{}^2}}$$

where:
$\omega_c = 2\pi\ f_c$ with f_c = cutoff frequency

ξ = damping factor.

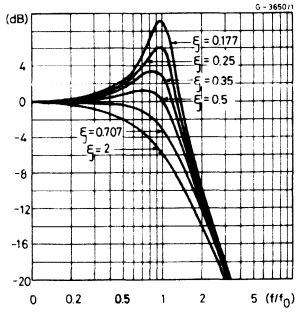
APPLICATION INFORMATION (continued)

Three parameters are needed to characterise the frequency and phase response of a 2nd order active filter: the gain (G_v), the damping factor (ξ) or the Q-factor ($Q = (2\xi)^{-1}$), and the cutoff frequency (f_c).
The higher order responses are obtained with a series of 2nd order sections. A simple RC section is introduced when an odd filter is required.
The choice of 'ξ' (or Q-factor) determines the filter response (see table).

Tab. I

Filter response	ξ	Q	Cutoff frequency f_c
Bessel	$\frac{\sqrt{3}}{2}$	$\frac{1}{\sqrt{3}}$	Frequency at which phase shift is -90°
Butterworth	$\frac{\sqrt{2}}{2}$	$\frac{1}{\sqrt{2}}$	Frequency at which G_v= -3 dB
Chebyschev	$< \frac{\sqrt{2}}{2}$	$> \frac{1}{\sqrt{2}}$	Frequency at which the amplitude response passes through specified max. ripple band and enters the stop band

Fig. 14 - Filter response vs. damping factor



Fixed $R = R_1 = R_2$, we have (see fig. 13)

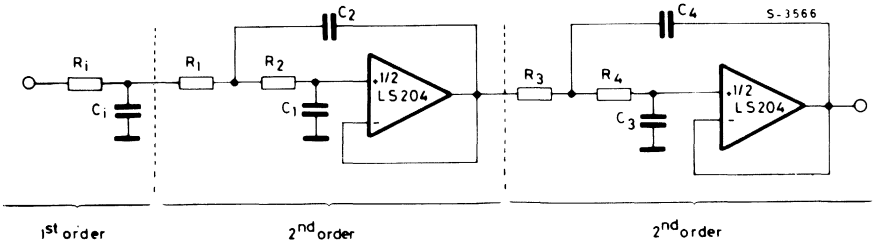
$$C_1 = \frac{1}{R}\,\frac{\xi}{\omega_c}$$

$$C_2 = \frac{1}{R}\,\frac{1}{\xi\,\omega_c}$$

The diagram of fig. 14 shows the amplitude response for different values of damping factor ξ in 2nd order filters.

EXAMPLE:

Fig. 15 - 5th order low pass filter (Butterworth) with unity gain configuration.



APPLICATION INFORMATION (continued)

In the circuit of fig. 15, for f_c = 3.4 KHz and $R_i = R_1 = R_2 = R_3 = R_4 = 10\ K\Omega$, we obtain:

$$C_i = 1.354 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 6.33\ nF$$

$$C_1 = 0.421 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.97\ nF$$

$$C_2 = 1.753 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 8.20\ nF$$

$$C_3 = 0.309 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.45\ nF$$

$$C_4 = 3.325 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 15.14\ nF$$

The attenuation of the filter is 30 dB at 6.8 KHz and better than 60 dB at 15 KHz.

Tab. II
Damping factor for low-pass Butterworth filters

Order	C_i	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
2		0.707	1.41						
3	1.392	0.202	3.54						
4		0.92	1.08	0.38	2.61				
5	1.354	0.421	1.75	0.309	3.235				
6		0.966	1.035	0.707	1.414	0.259	3.86		
7	1.336	0.488	1.53	0.623	1.604	0.222	4.49		
8		0.98	1.02	0.83	1.20	0.556	1.80	0.195	5.125

The same method, referring to Tab. II and fig. 16, is used to design high-pass filter. In this case the damping factor is found by taking the reciprocal of the numbers in Tab. II. For f_c = 5KHz and $C_i = C_1 = C_2 = C_3 = C_4 = 1$ nF we obtain:

$$R_i = \frac{1}{1.354} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 23.5\ K\Omega$$

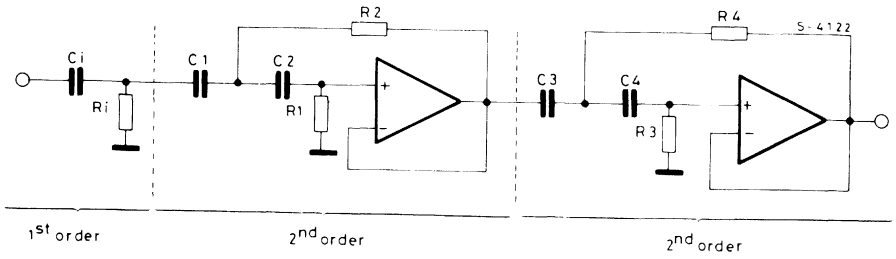
$$R_1 = \frac{1}{0.421} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 75.6\ K\Omega$$

$$R_2 = \frac{1}{1.753} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 18.2\ K\Omega$$

$$R_3 = \frac{1}{0.309} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 103\ K\Omega$$

$$R_4 = \frac{1}{3.325} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 9.6\ K\Omega$$

Fig. 16 - 5th order high-pass filter (Butterworth) with unity gain configuration.

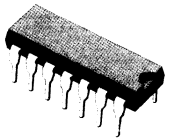


LS404

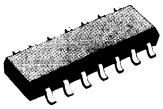
HIGH PERFORMANCE QUAD OPERATIONAL AMPLIFIERS

- SINGLE OR SPLIT SUPPLY OPERATION
- VERY LOW POWER CONSUMPTION
- SHORT CIRCUIT PROTECTION
- LOW DISTORTION, LOW NOISE
- HIGH GAIN-BANDWIDTH PRODUCT
- HIGH CHANNEL SEPARATION

The LS404 is a high performance quad operational amplifier with frequency and phase compensation built into the chip. The internal phase compensation allows stable operation as voltage follower in spite of its high gain-bandwidth product. The circuit presents very stable electrical characteristics over the entire supply voltage range, and it is partucularly intended for professional and telecom applications (active filters, etc.).
The patented input stage circuit allows small input signal swings below the negative supply voltage and prevents phase inversion when the input is over driven.



DIP-14 Plastic



SO-14

ABSOLUTE MAXIMUM RATINGS

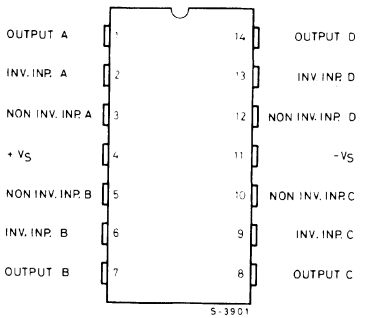
V_s	Supply voltage		± 18	V
V_i	Input voltage	(positive)	$+ V_s$	
		(negative)	$-V_s - 0.5$	V
V_i	Differential input voltage		± (V_s - 1)	
T_{op}	Operating temperature	**LS 404**	-25 to + 85	°C
		LS 404C	0 to + 70	°C
P_{tot}	Power dissipation	(T_{amb} = 70°C)	400	mW
T_{stg}	Storage temperature		-55 to + 150	°C

LS404

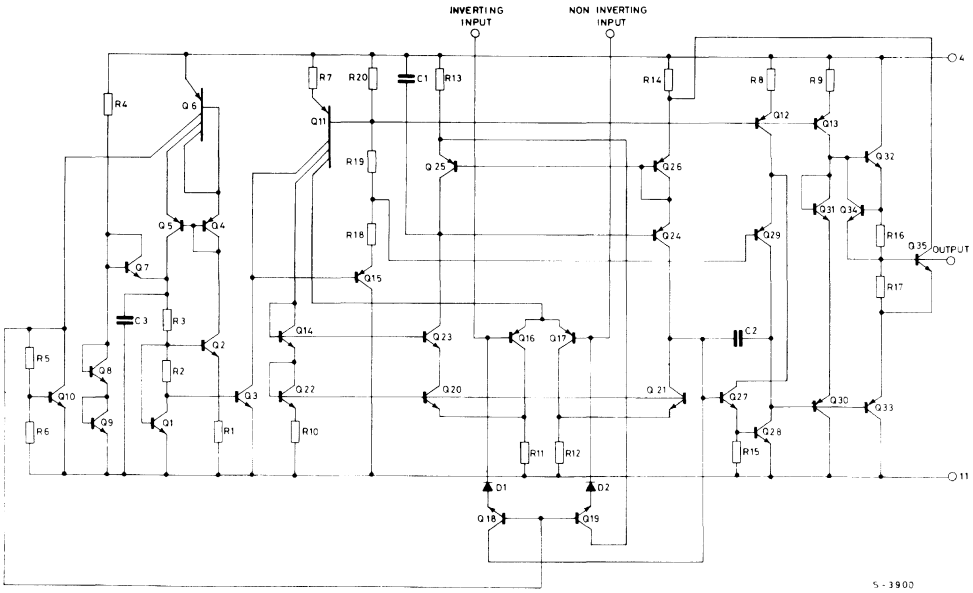
CONNECTION DIAGRAM AND ORDERING NUMBERS

(top view)

Type	DIP 14	SO-14
LS 404 LS 404C	— LS 404CB	LS 404M LS 404CM



SCHEMATIC DIAGRAM (one section)



THERMAL DATA

			DIP 14	SO-14
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	200°C/W	200°C/W

ELECTRICAL CHARACTERISTICS ($V_s = \pm 12V$, $T_{amb} = 25°C$, unless otherwise specified)

Parameter		Test conditions	LS 404			LS 404C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_s	Supply current			1.3	2		1.5	3	mA
I_b	Input bias current			50	200		100	300	nA
R_i	Input resistance	f = 1KHz		0.7			0.5		MΩ
V_{os}	Input offset voltage	R_g = 10KΩ		1	2.5		1	5	mV
$\frac{\Delta V_{os}}{\Delta T}$	Input offset voltage drift	R_g = 10KΩ $T_{min} < T_{op} < T_{max}$		5			5		μV/°C
I_{os}	Input offset current			10	40		20	80	nA
$\frac{\Delta I_{os}}{\Delta T}$	Input offset current drift	$T_{min} < T_{op} < T_{max}$		0.08			0.1		$\frac{nA}{°C}$
I_{sc}	Output short circuit current			23			23		mA
G_v	Large signal open loop voltage gain	R_L = 2KΩ V_s = ±12V V_s = ±4V	90	100 95		86	100 95		dB
B	Gain-bandwidth product	f = 20KHz	1.8	3		1.5	2.5		MHz
e_N	Total input noise voltage	f = 1KHz R_g = 50Ω R_g = 1KΩ R_g = 10KΩ		8 10 18	15		10 12 20		$\frac{nV}{\sqrt{Hz}}$
d	Distortion	unity gain R_L = 2KΩ f = 1 KHz V_o = 2Vpp f = 20 KHz		0.01 0.03	0.04		0.01 0.03		%
V_o	DC output voltage swing	R_L = 2KΩ V_s = ± 12V V_s = ± 4V	± 10	± 3		± 10	± 3		V
V_o	Large signal voltage swing	f = 10KHz R_L = 10 KΩ R_L = 1 KΩ		22 20			22 20		Vpp
SR	Slew rate	unity gain R_L = 2KΩ	0.8	1.5			1		V/μs
CMR	Comm. mode rejection	V_i = 10V	90	94		80	90		dB
SVR	Supply voltage rejection	V_i = 1V f = 100Hz	90	94		86	90		dB
CS	Channel separation	f = 1KHz	100	120			120		dB

Fig. 1 - Supply current vs. supply voltage

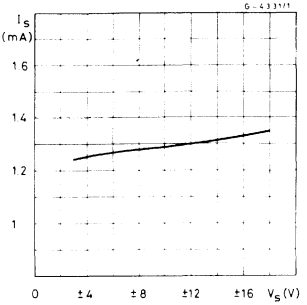


Fig. 2 - Supply current vs. ambient temperature

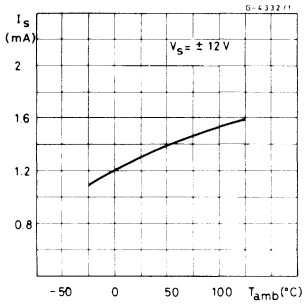


Fig. 3 - Output short circuit current vs. ambient temperature

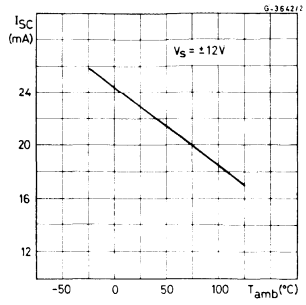


Fig. 4 - Open loop frequency and phase response

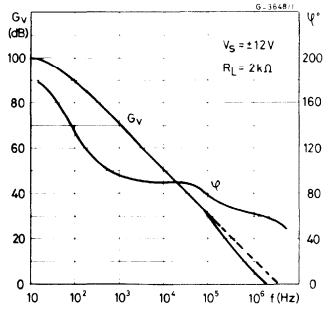


Fig. 5 - Open loop gain vs. ambient temperature

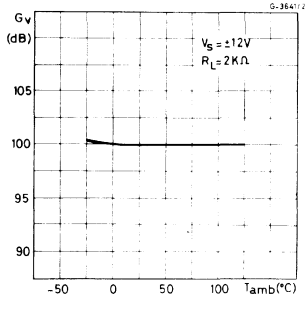


Fig. 6 - Supply voltage rejection vs. frequency

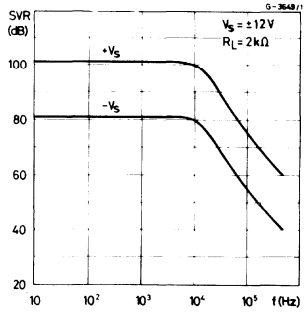


Fig. 7 - Large signal frequency response

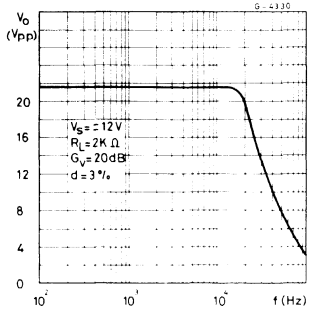


Fig. 8 - Output voltage swing vs. load resistance

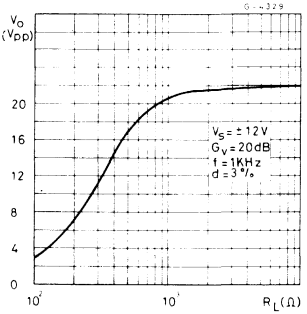
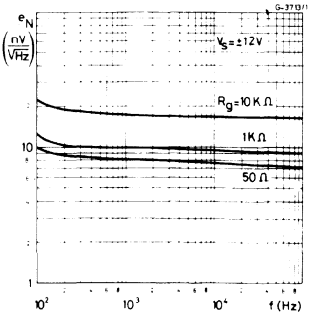


Fig. 9 - Total input noise vs. frequency



APPLICATION INFORMATION

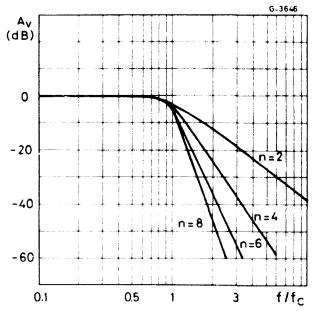
Active low-pass filter:

BUTTERWORTH

The Butterworth is a "maximally flat" amplitude response filter. Butterworth filters are used for filtering signals in data acquisition systems to prevent aliasing errors in sampled-data applications and for general purpose low-pass filtering.
The cutoff frequency, f_c, is the frequency at which the amplitude response in down 3 dB. The attenuation rate beyond the cutoff frequency is -n6 dB per octave of frequency where n is the order (number of poles) of the filter.
Other characteristics:

- Flattest possible amplitude response.
- Excellent gain accuracy at low frequency end of passband.

Fig. 10 - Amplitude response



BESSEL

The Bessel is a type of "linear phase" filter. Because of their linear phase characteristics, these filters approximate a constant time delay over a limited frequency range. Bessel filters pass transient waveforms with a minimum of distortion. They are also used to provide time delays for low pass filtering of modulated waveforms and as a "running average" type filter.

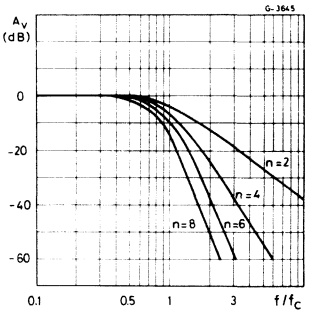
The maximum phase shift is $\frac{-n\pi}{2}$ radians where n is the order (number of poles) of the filter. The cutoff frequency, f_c, is defined as the frequency at which the phase shift is one half to this value. For accurate delay, the cutoff frequency should be twice the maximum signal frequency. The following table can be used to obtain the -3 dB frequency of the filter.

	2 pole	4 pole	6 pole	8 pole
-3 dB frequency	0.77 f_c	0.67 f_c	0.57 f_c	0.50 f_c

Other characteristics:

- Selectivity not as great as Chebyschev or Butterworth.
- Very small overshoot response to step inputs
- Fast rise time.

Fig. 11 - Amplitude response

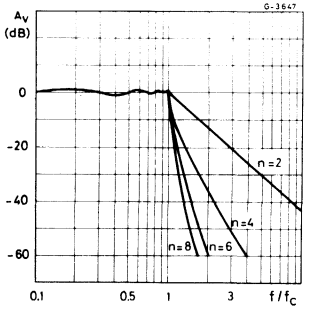


CHEBYSCHEV

Chebyschev filters have greater selectivity than either Bessel or Butterworth at the expense of ripple in the passband.
Chebyschev filters are normally designed with peak-to-peak ripple values from 0.2 dB to 2 dB.
Increased ripple in the passband allows increased attenuation above the cutoff frequency.
The cutoff frequency is defined as the frequency at which the amplitude response passes through the specified maximum ripple band and enters the stop band.
Other characteristics:

- Greater selectivity
- Very nonlinear phase response
- High overshoot response to step inputs.

Fig. 12 - Amplitude response (± 1 dB ripple)



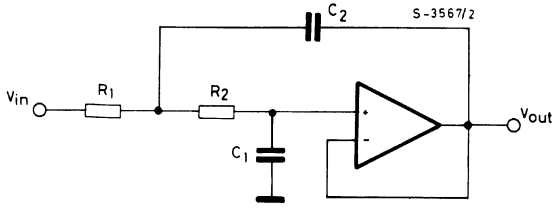
APPLICATION INFORMATION (continued)

The table below shows the typical overshoot and settling time response of the low pass filter to a step input.

	NUMBER OF POLES	PEAK OVERSHOOT	SETTLING TIME (% of final value)		
		% Overshoot	± 1%	± 0.1%	± 0.01%
BUTTERWORTH	2	4	$1.1/f_c$ sec.	$1.7/f_c$ sec.	$1.9/f_c$ sec.
	4	11	$1.7/f_c$	$2.8/f_c$	$3.8/f_c$
	6	14	$2.4/f_c$	$3.9/f_c$	$5.0/f_c$
	8	16	$3.1/f_c$	$5.1/f_c$	$7.1/f_c$
BESSEL	2	0.4	$0.8/f_c$	$1.4/f_c$	$1.7/f_c$
	4	0.8	$1.0/f_c$	$1.8/f_c$	$2.4/f_c$
	6	0.6	$1.3/f_c$	$2.1/f_c$	$2.7/f_c$
	8	0.3	$1.6/f_c$	$2.3/f_c$	$3.2/f_c$
CHEBYSCHEV (RIPPLE ± 0.25 dB)	2	11	$1.1/f_c$	$1.6/f_c$	–
	4	18	$3.0/f_c$	$5.4/f_c$	–
	6	21	$5.9/f_c$	$10.4/f_c$	–
	8	23	$8.4/f_c$	$16.4/f_c$	–
CHEBYSCHEV (RIPPLE ± 1 dB)	2	21	$1.6/f_c$	$2.7/f_c$	–
	4	28	$4.8/f_c$	$8.4/f_c$	–
	6	32	$8.2/f_c$	$16.3/f_c$	–
	8	34	$11.6/f_c$	$24.8/f_c$	–

Design of 2nd order active low pass filter
(Sallen and Key configuration unity gain op-amp)

Fig. 13 - Filter configuration



$$\frac{V_o}{V_i} = \frac{1}{1 + 2\xi\frac{S}{\omega_c} + \frac{S^2}{\omega_c^2}}$$

where:

$\omega_c = 2\pi f_c$ with f_c = cutoff frequency

ξ = damping factor.

APPLICATION INFORMATION (continued)

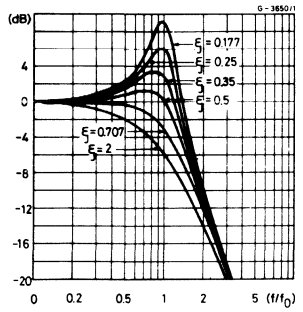
Three parameters are needed to characterize the frequency and phase response of a 2nd order active filter: the gain (G_v), the damping factor (ξ) or the Q-factor ($Q = (2\xi)^{-1}$), and the cutoff frequency (f_c).

The higher order responses are obtained with a series of 2nd order sections. A simple RC section is introduced when an odd filter is required. The choice of 'ξ' (or Q-factor) determines the filter response (see table).

TAB. 1

Filter response	ξ	Q	Cutoff frequency f_c
Bessel	$\frac{\sqrt{3}}{2}$	$\frac{1}{\sqrt{3}}$	Frequency at which phase shift is -90°
Butterworth	$\frac{\sqrt{2}}{2}$	$\frac{1}{\sqrt{2}}$	Frequency at which G_v = -3 dB
Chebyschev	$<\frac{\sqrt{2}}{2}$	$>\frac{1}{\sqrt{2}}$	Frequency at which the amplitude response passes through specified max. ripple band and enters the stop band

Fig. 14 - Filter response vs. damping factor



Fixed $R = R_1 = R_2$, we have (see fig. 13)

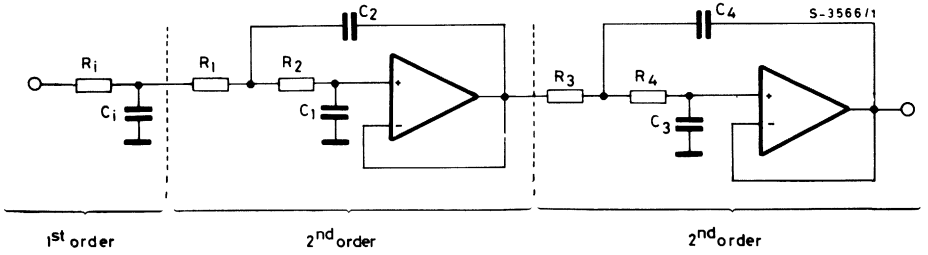
$$C_1 = \frac{1}{R}\frac{\xi}{\omega_c}$$

$$C_2 = \frac{1}{R}\frac{1}{\xi\,\omega_c}$$

The diagram of fig. 14 shows the amplitude response for different values of damping factor ξ in 2nd order filters.

EXAMPLE:

Fig. 15 - 5th order low pass filter (Butterworth) with unity gain configuration.



APPLICATION INFORMATION (continued)

In the circuit of fig. 15, for f_c = 3.4 KHz and $R_i = R_1 = R_2 = R_3 = R_4 = 10\ K\Omega$, we obtain:

$$C_i = 1.354 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 6.33\ nF$$

$$C_1 = 0.421 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.97\ nF$$

$$C_2 = 1.753 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 8.20\ nF$$

$$C_3 = 0.309 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.45\ nF$$

$$C_4 = 3.325 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 15.14\ nF$$

The attenuation of the filter is 30 dB at 6.8 KHz and better than 60 dB at 15 KHz.

Tab. II
Damping factor for low-pass Butterworth filters

Order	C_i	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
2		0.707	1.41						
3	1.392	0.202	3.54						
4		0.92	1.08	0.38	2.61				
5	1.354	0.421	1.75	0.309	3.235				
6		0.966	1.035	0.707	1.414	0.259	3.86		
7	1.336	0.488	1.53	0.623	1.604	0.222	4.49		
8		0.98	1.02	0.83	1.20	0.556	1.80	0.195	5.125

The same method, referring to Tab. II and fig. 16, is used to design high-pass filter. In this case the damping factor is found by taking the reciprocal of the numbers in Tab. II. For f_c = 5KHz and $C_i = C_1 = C_2 = C_3 = C_4 = 1$ nF we obtain:

$$R_i = \frac{1}{1.354} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 23.5\ K\Omega$$

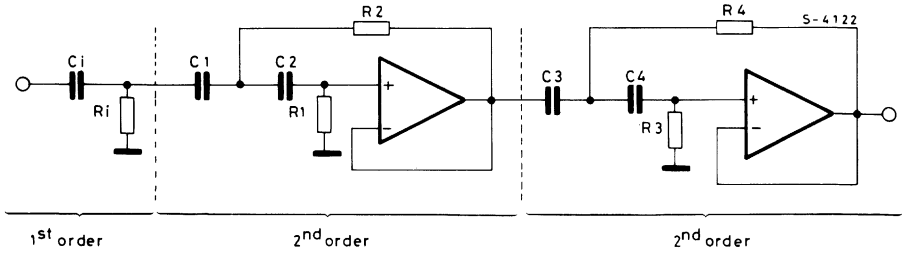
$$R_1 = \frac{1}{0.421} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 75.6\ K\Omega$$

$$R_2 = \frac{1}{1.753} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 18.2\ K\Omega$$

$$R_3 = \frac{1}{0.309} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 103\ K\Omega$$

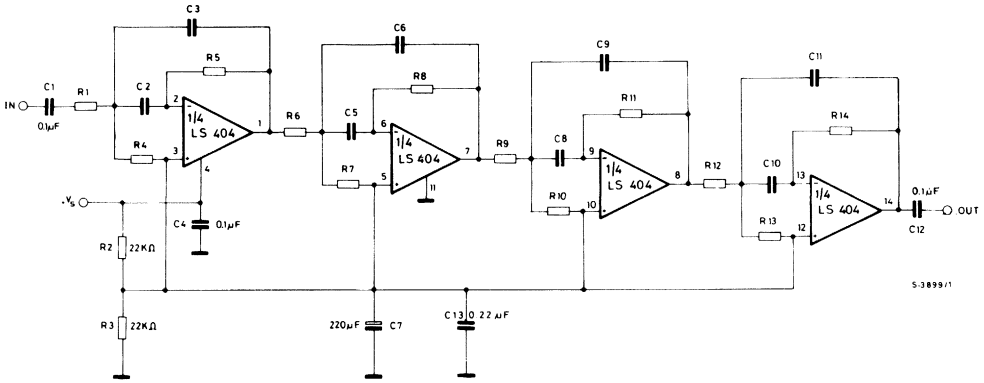
$$R_4 = \frac{1}{3.325} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 9.6\ K\Omega$$

Fig. 16 - 5th order high-pass filter (Butterworth) with unity gain configuration.



APPLICATION INFORMATION (continued)

Fig. 17 - Multiple feedback 8-pole bandpass filter.



f_c = 1.180Hz; A = 1; $C_2 = C_3 = C_5 = C_6 = C_8 = C_9 = C_{10} = C_{11}$ = 3.300 pF;
$R_1 = R_6 = R_9 = R_{12}$ = 160 KΩ; $R_5 = R_8 = R_{11} = R_{14}$ = 330KΩ; $R_4 = R_7 = R_{10} = R_{13}$ = 5.3KΩ

Fig. 18 - Frequency response of band-pass filter

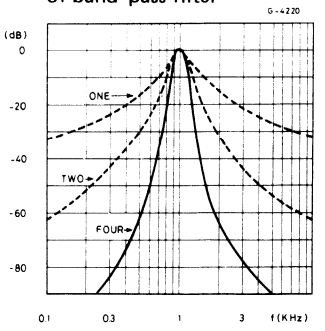
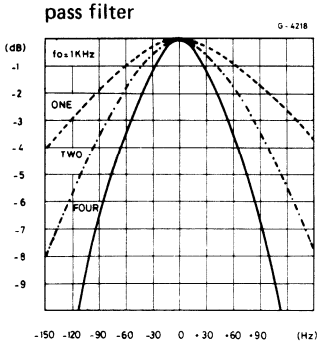
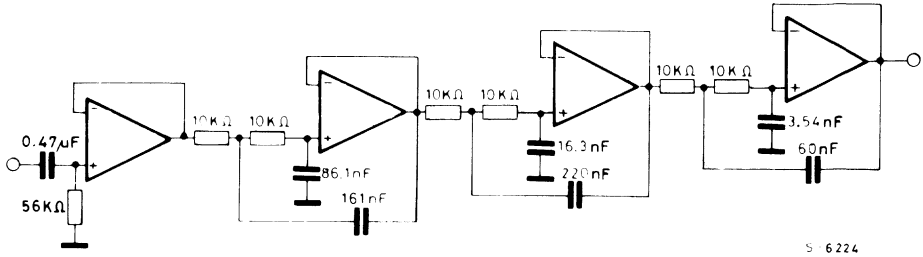


Fig. 19 - Bandwidth of band-pass filter



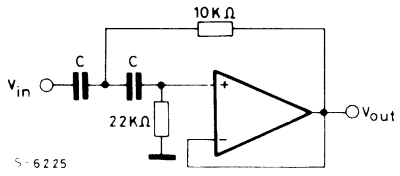
APPLICATION INFORMATION (continued)

Fig. 20 - Six-pole 355 Hz low-pass filter (Chebychev type)



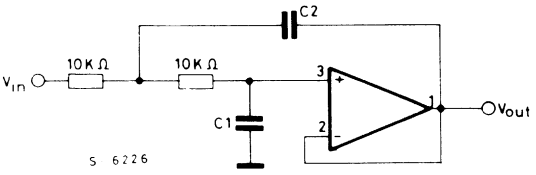
This is a 6- pole Chebychev type with ± 0.25 dB ripple in the passband. A decoupling stage is used to avoid the influence of the input impedance on the filter's characteristics. The attenuation is about 55 dB at 710 Hz and reaches 80 dB at 1065 Hz. The in band attenuation is limited in practice to the ± 0.25 dB ripple and does not exceed 0.5 dB at 0.9 fc.

Fig. 21 - Subsonic filter (G_v = 0 dB)



f_c (Hz)	C (µF)
15	0.68
22	0.47
30	0.33
55	0.22
100	0.1

Fig. 22 - High cut filter (G_v = 0 dB)



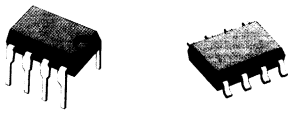
f_c (KHz)	C1 (nF)	C2 (nF)
3	3.9	6.8
5	2.2	4.7
10	1.2	2.2
15	0.68	1.5

LS4558N

DUAL HIGH PERFORMANCE OPERATIONAL AMPLIFIER

- SINGLE OR SPLIT SUPPLY OPERATION
- LOW POWER CONSUMPTION
- HIGH UNITY GAIN BANDWIDTH
- NO CROSSOVER DISTORTION
- NO POP NOISE
- SHORT CIRCUIT PROTECTION
- HIGH CHANNEL SEPARATION

The LS4558N is a high performace dual operational amplifier with frequency and phase compensation built into the chip. The internal phase compensation allows stable operation as voltage follower in spite of its high gain-bandwidth products. The circuit presents very stable electrical characteristics over the entire supply voltage range and the specially designed input stage allow the LS4558N to be used in **low noise audio signal processing application**. The optimized class AB output stage completely eliminates crossover, distortion, under any load conditions, has large source and sink capacity and is short circuit protected.



Minidip **SO-8**

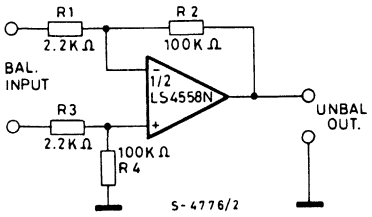
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage		± 18	V
V_I	Input voltage		± V_s	
V_i	Differential input voltage		± (V_s - 1)	V
P_{tot}	Power dissipation at T_{amb} = 70°C	Minidip	665	mW
		Micropackage	400	mW
T_{op}	Operating temperature		0 to 70	°C
T_j	Junction temperature		150	°C
T_{stg}	Storage temperature		-55 to 150	°C

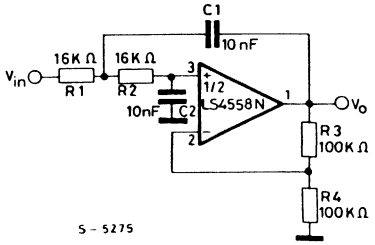
ORDERING NUMBER: LS 4558 NB (Minidip)
LS 4558 NM (Micropackage)

TYPICAL APPLICATIONS:

Balanced input audio preamplifier

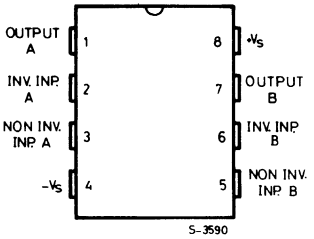


DC coupled low-pass active filter
(f = 1KHz, G_v = 6dB

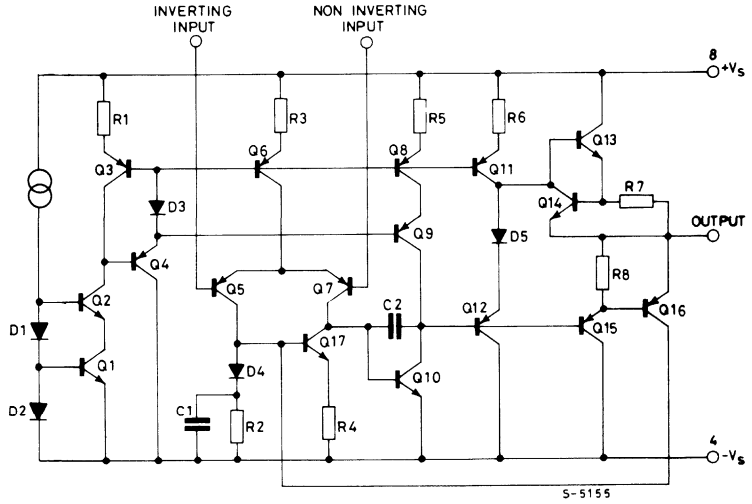


LS4558N

CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one section)



THERMAL DATA

		Minidip	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	120 °C/W	200°C/W

ELECTRICAL CHARACTERISTICS ($V_s = \pm 15V$, $T_{amb} = 25°C$, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_s	Supply current (*)			1	2	mA
I_b	Input bias current			50	500	nA
		$T_{min} < T_{op} < T_{max}$			800	nA
R_i	Input resistance	f = 1 KHz	0.3	1		MΩ
V_{os}	Input offset voltage	$R_g \leq 10$ KΩ		0.5	5	mV
		$R_g \leq 10$ KΩ $T_{min} < T_{op} < T_{max}$			7.5	mV
I_{os}	Input offset current			20	200	nA
		$T_{min} < T_{op} < T_{max}$			500	nA
I_{sc}	Output short circuit current			23		mA
G_v	Large signal open loop voltage gain	$R_L = 2$ KΩ	86	100		dB
B	Gain-bandwidth product	f = 20 KHz	2	3		MHz
e_N	Total input noise voltage	f = 1 KHz $R_g = 50Ω$ $R_g = 1$ KΩ $R_g = 10$ KΩ		8 10 18	15	$\frac{nV}{\sqrt{Hz}}$
e_N	Popcorn noise	B = 1 Hz to 1 KHz $R_g = 10$ KΩ t = 10 sec			10	μV peak
d	Distortion	$G_v = 20$ dB $R_L = 2$ KΩ $V_o = 2$ Vpp f = 1 KHz		0.03		%
V_o	Output voltage swing	$R_L = 2$ KΩ		± 13		V
V_o	Large signal voltage swing	$R_L = 10$ KΩ f = 10 KHz		28		Vpp
Transient response	Rise time	$V_i = 20$ mV $R_L = 2$ KΩ $C_L = 100$ pF		0.13		μS
	Overshoot			5		%
SR	Slew rate	unity gain $R_L = 2$ KΩ	0.8	1.5		V/μs
CMR	Common mode rejection	$V_i = 10V$ $T_{min} < T_{op} < T_{max}$	70	90		dB
SVR	Supply voltage rejection	$V_i = 1V$ f = 100 Hz $T_{min} < T_{op} < T_{max}$	80	100		dB
CS	Channel separation	f = 10 KHz $R_g = 1$ KΩ		105		dB

(*) Both amplifiers.

Fig. 1 - Open loop frequency and phase response

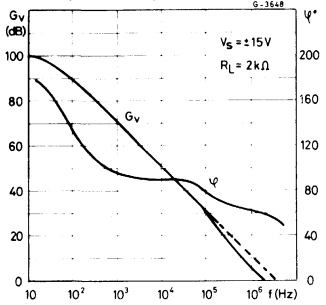


Fig. 2 - Open loop gain vs. ambient temperature

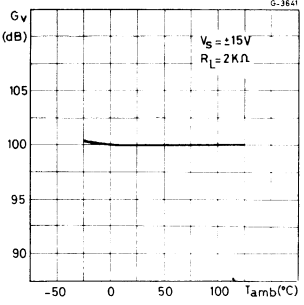


Fig. 3 - Supply voltage rejection vs. frequency

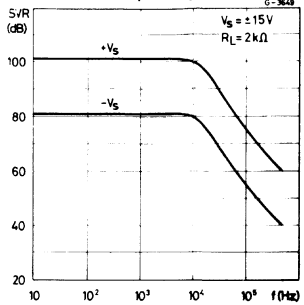


Fig. 4 - Large signal frequency response

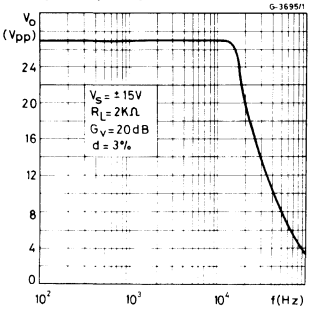


Fig. 5 - Output voltage swing vs. load resistance

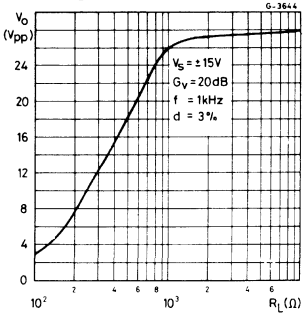


Fig. 6 - Total input noise vs. frequency

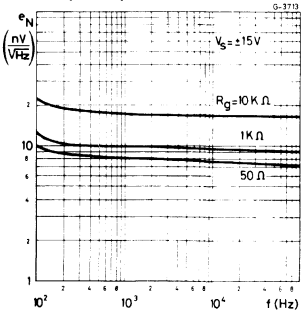


Fig. 7 - Channel separation

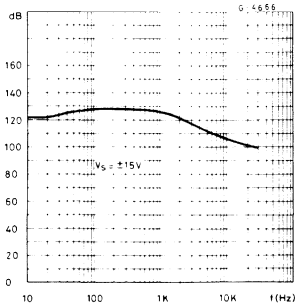


Fig. 8 - Transient response

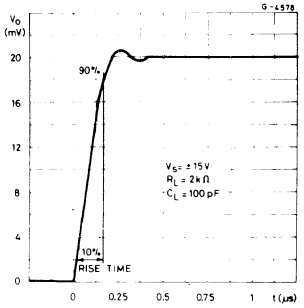
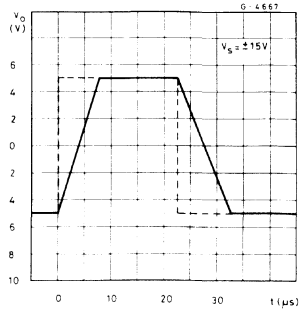
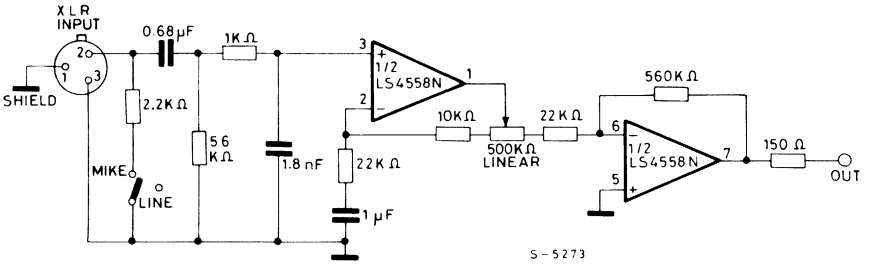


Fig. 9 - Voltage follower large-signal pulse response



APPLICATION INFORMATION

Fig. 10 - Mike/Line preamplifier for audio mixers (0 dB to 60 dB continuously variable gain)



Note – The particular characteristics of the circuit of fig. 10 is that using a linear potentiometer, the gain is continuously variable in a logarithmic mode from 0 dB to 60 dB in the audio band.

Fig. 11 - Microphones nomograph

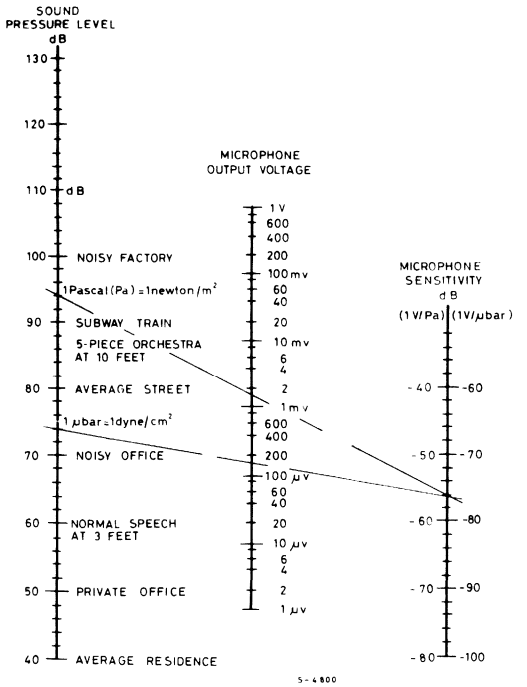


Fig. 12 - Very Low-Noise mike preamplifier (G_v= 40 dB)

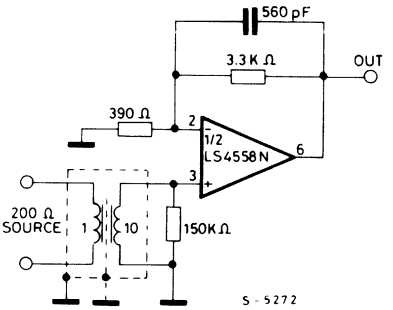
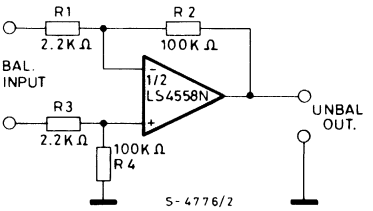


Fig. 13 - Balanced input audio preamplifier



APPLICATION INFORMATION (continued)

Fig. 14 - 20 Hz to 200 Hz variable High-pass filter (G_v = 3 dB)

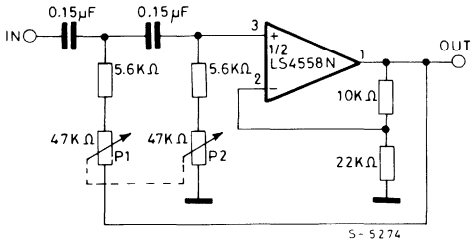


Fig. 15 - Frequency response of the High-pass filter of fig. 14

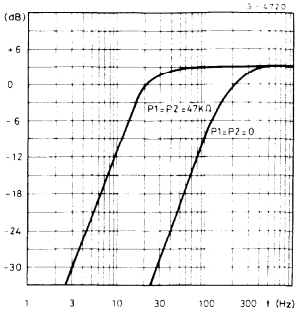


Fig. 16 - DC coupled low-pass active filter (f = 1KHz, G_v= 6 dB)

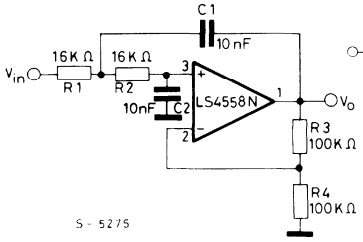


Fig. 17 - Switchable HP-LP audio filter

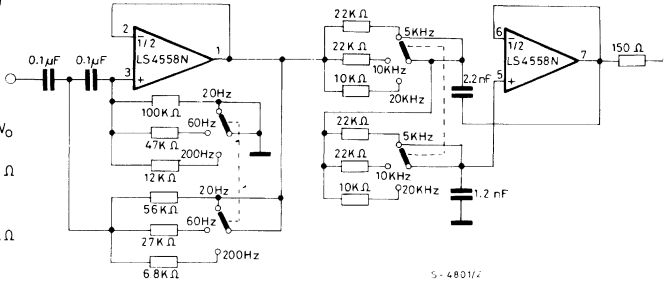
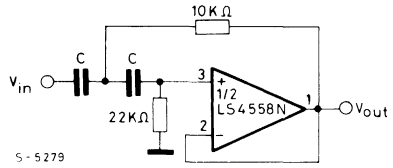
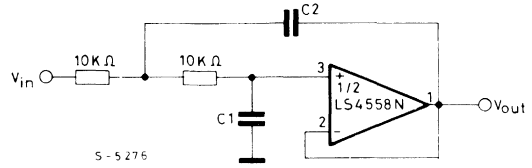


Fig. 18 - Subsonic or rumble filter (G_v= 0 dB)



f_c (Hz)	C (µF)
15	0.68
22	0.47
30	0.33
55	0.22
100	0.1

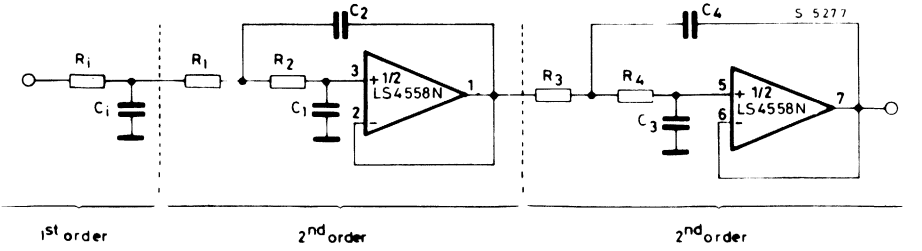
Fig. 19 - High-cut filter (G_v= 0 dB)



f_c (KHz)	C1 (nF)	C2 (nF)
3	3.9	6.8
5	2.2	4.7
10	1.2	2.2
15	0.68	1.5

APPLICATION INFORMATION (continued)

Fig. 20 - Fifth order 3.4 KHz low-pass Butterworth filter



For f_c = 3.4 KHz and R_i = R1 = R2 = R3 = R4 = 10 KΩ, we obtain:

$C1 = 1.354 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 6.33$ nF

$C1 = 0.421 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.97$ nF

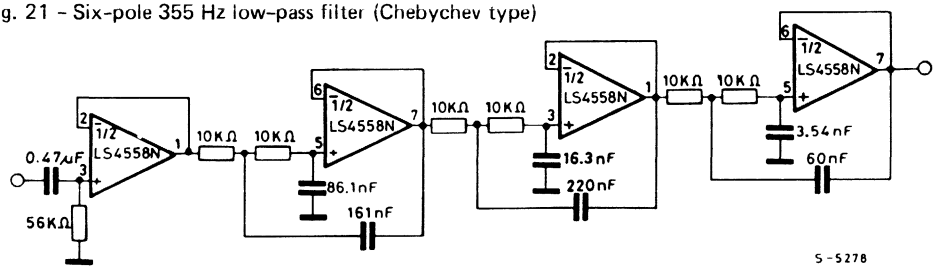
$C2 = 1.753 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 8.20$ nF

$C3 = 0.309 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.45$ nF

$C4 = 3.325 \cdot \frac{1}{R} \cdot \frac{1}{2,\pi f_c} = 15.14$ nF

The attenuation of the filter is 30 dB at 6.8 KHz and better than 60 dB at 15 KHz.

Fig. 21 - Six-pole 355 Hz low-pass filter (Chebychev type)



This is a 6- pole Chebychev type with ± 0.25 dB ripple in the passband. A decoupling stage is used to avoid the influence of the input impedance on the filter's characteristics. The attenuation is about 55 dB at 710 Hz and reaches 80 dB at 1065 Hz. The in band attenuation is limited in practice to the ± 0.25 dB ripple and does not exceed 0.5 dB at 0.9 fc.

M5450
M5451

LED DISPLAY DRIVERS

- M5450 34 OUTPUTS/15mA SINK
- M5451 35 OUTPUTS/15mA SINK
- CURRENT GENERATOR OUTPUTS (NO EXTERNAL RESISTORS REQUIRED)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- ENABLE (ON M5450)
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

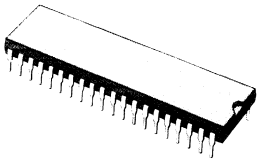
Application examples:

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATOR
- RELAY DRIVER
- INSTRUMENTATION READOUTS

The M5450 and M5451 are monolithic MOS integrated circuits produced with an N-channel silicon gate technology. They are available in 40-pin dual in-line plastic packages.

A single pin controls the LED display brightness by setting a reference current through a variable resistor connected to V_{DD} or to a separate supply of 13.2V maximum.

The M5450 and M5451 are pin-to-pin replacements of the NS MM 5450 and MM 5451.



DIP-40 Plastic

ORDERING NUMBERS: M5450 B7
M5451 B7

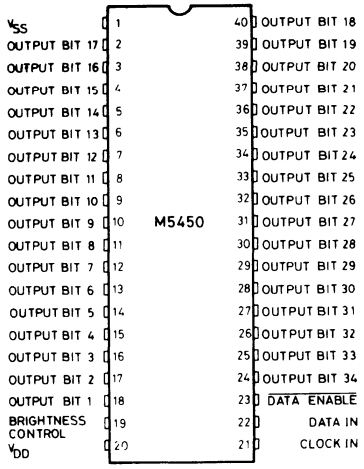
ABSOLUTE MAXIMUM RATINGS

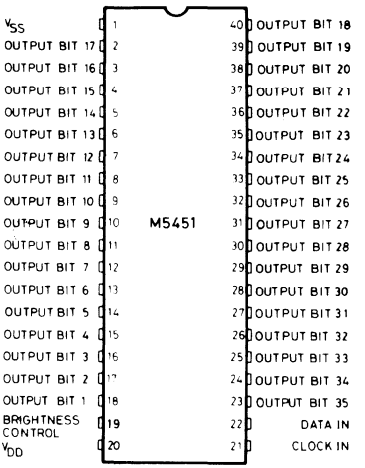
V_{DD}	Supply voltage	-0.3 to 15	V
V_I	Input voltage	-0.3 to 15	V
$V_{O(off)}$	Off state output voltage	15	V
I_O	Output sink current	40	mA
P_{tot}	Total package power dissipation	at 25°C	1W
		at 85°C	560 mW
T_j	Junction temperature	150	°C
T_{op}	Operating temperature range	-25 to 85	°C
T_{stg}	Storage temperature range	-65 to 150	°C

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

M5450
M5451

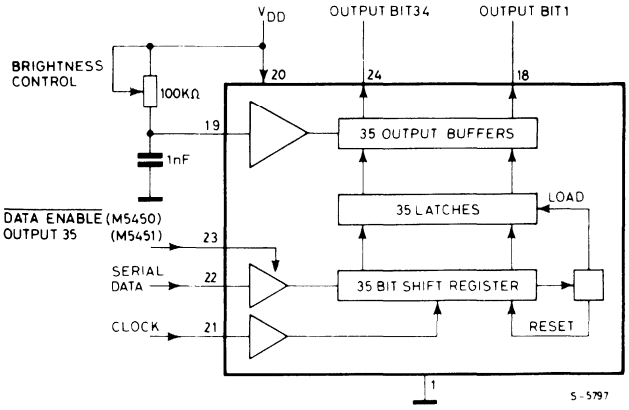
CONNECTION DIAGRAMS





BLOCK DIAGRAM

Fig. 1



STATIC ELECTRICAL CHARACTERISTICS (T_{amb} within operating range, V_{DD}= 4.75V to 13.2V, V_{SS}= 0V, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.75		13.2	V
I_{DD}	Supply Current	V_{DD}= 13.2V			7	mA
V_I	Input Voltage Logical "0" Level Logical "1" Level	± 10 μA input bias 4.75 ⩽ V_{DD} ⩽ 5.25 V_{DD} > 5.25	 -0.3 2.2 V_{DD}-2		 0.8 V_{DD} V_{DD}	 V V V
I_B	Brightness Input Current (note 2)		0		0.75	mA
V_B	Brightness Input Voltage (pin 19)	Input current = 750 μA	3		4.3	V
$V_{O(off)}$	Off State Out. Voltage				13.2	V
I_O	Out. Sink Current (note 3) Segment OFF Segment ON	 V_O = 3V V_O = 1V (note 4) Brightness In. = 0 μA Brightness In. = 100 μA Brightness In. = 750 μA	 0 2 12	 2.7 15	 10 10 4 25	 μA μA mA mA
f_{clock}	Input Clock Frequency		0		0.5	MHz
I_O	Output Matching (note 1)				± 20	%

Notes : 1. Output matching is calculated as the percent variation from $I_{MAX} + I_{MIN}/2$.

2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.

3. Absolute maximum for each output should be limited to 40 mA.

4. The V_O voltage should be regulated by the user. See figures 5 and 6 for allowable V_O versus I_O operation.

FUNCTIONAL DESCRIPTION

Both the M5450 and the M5451 are specifically designed to operate 4 or 5-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display.
Outputs change only if the serial data bits differ from the previous time.
Display brightness is determined by control of the output current LED displays.
A 1nF capacitor should be connected to brightness control, pin 19, to prevent possible oscillations.
A block diagram is shown in figure 1. For the M5450 a $\overline{\text{DATA ENABLE}}$ is used instead of the 35th output. The $\overline{\text{DATA ENABLE}}$ input is a metal option for the M5450.

FUNCTIONAL DESCRIPTION (continued)

The output current is typically 20 times greater than the current into pin 19, which is set by an external variable resistor. There is an internal limiting resistor of 400Ω nominal value.

Figure 2 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.
At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configurations. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Bit 1 is the first bit following the start bit and it will appear on pin 18. A logical "1" at the input will turn on the appropriate LED.
Figure 3 shows the timing relationship between Data, Clock and $\overline{\text{DATA ENABLE}}$.
A max clock frequency of 0.5 MHz is assumed.

For applications where a lesser number of outputs are used, it is possible to either increase the current per output or operate the part at higher than 1V V_{OUT}.
The following equation can be used for calculations.

$$T_j = [\,(V_{OUT})\ (I_{LED})\ (\text{No. of segments}) + (V_{DD} \cdot 7\ \text{mA})\,]\ (124\ °C/W) + T_{amb}$$

where:

T_j = junction temperature (150°C max)
V_{OUT} = the voltage at the LED driver outputs
I_{LED} = the LED current
124°C/W = thermal coefficient of the package
T_{amb} = ambient temperature

The above equation was used to plot figure 4, 5 and 6.

Fig. 2 - Input Data Format

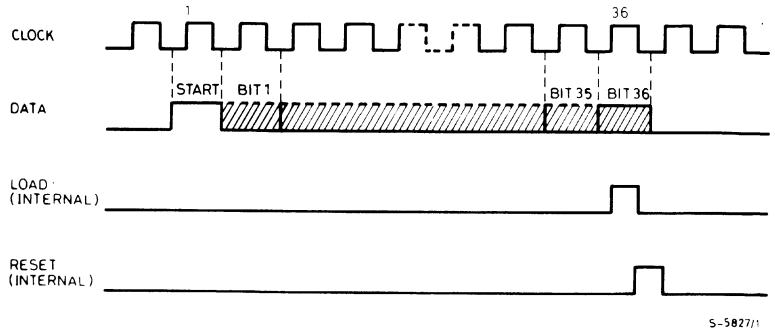


Fig. 3

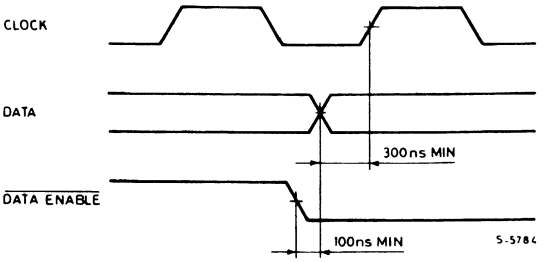


Fig. 4

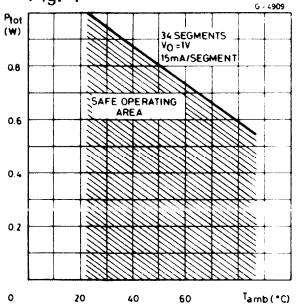


Fig. 5

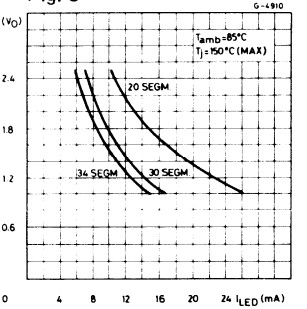
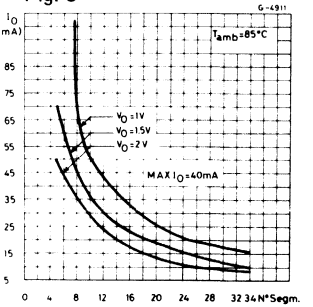
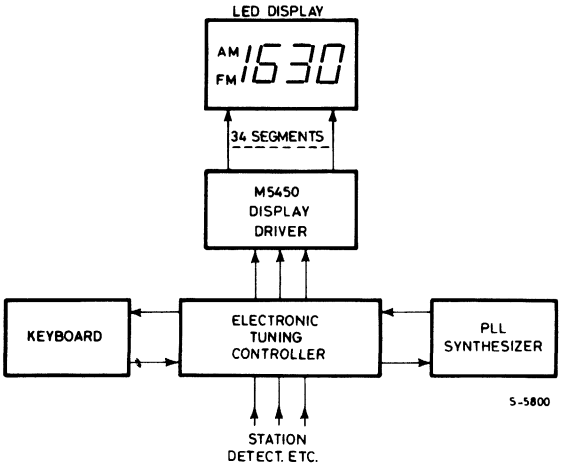


Fig. 6



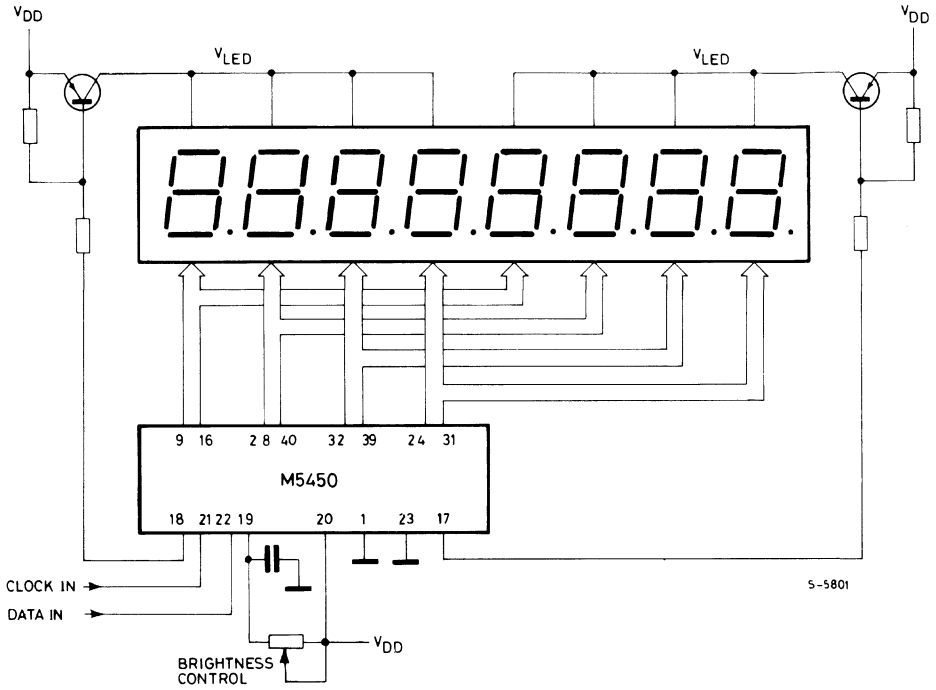
TYPICAL APPLICATIONS

Basic electronically tuned Radio or TV system



TYPICAL APPLICATIONS (continued)

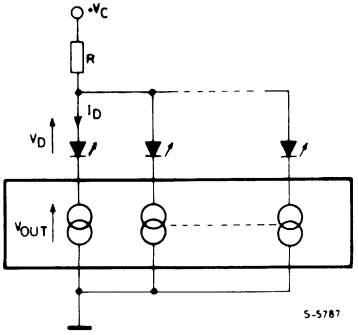
Duplexing 8 Digits with One M5450



POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

a)

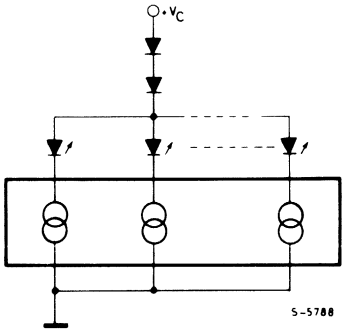


In this application R must be chosen taking into account the worst operating conditions.
R is determined by the maximum number of segments activated

$$R = \frac{V_C - V_{D\,MAX} - V_{O\,MIN}}{N_{MAX} \cdot I_D}$$

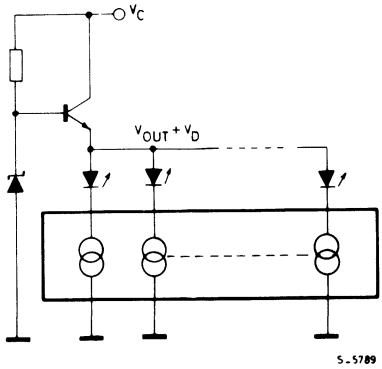
The worst case condition for the device is when roughly half of the maximum number of segments are activated.
It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.
In critical cases more resistors can be used in conjunction with groups of segments.
In this case the current variation in the single resistor is reduced and P_{tot} limited.

b)



In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.
The total power dissipation of the IC depends, in a first approximation, only on the number of segments activated.

c)



In this configuration $V_{OUT} + V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.

M5480

LED DISPLAY DRIVER

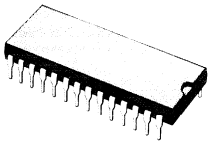
- 3½ DIGIT LED DRIVER (23 SEGMENTS)
- CURRENT GENERATOR OUTPUTS (NO RESISTORS REQUIRED)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- NO LOAD SIGNAL REQUIRED
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

Applications examples:

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATION
- RELAY DRIVER
- INSTRUMENTATION READOUTS

The M5480 is a monolithic MOS integrated circuit produced with a N-channel silicon gate technology. It utilizes the M5451 die packaged in a 28-pin plastic package making it ideal for a 3½ digit dispaly. A single pin controls the LED dispaly brightness by setting a reference current through a variable resistor connected either to V_{DD} or to a separate supply of 13.2V maximum.

The M5480 is a pin-to-pin replacement of the NS MM 5480.



DIP-28 Plastic

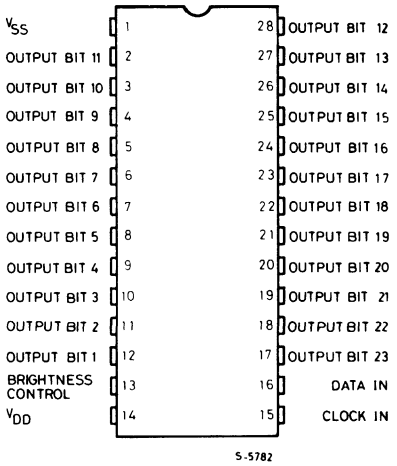
ORDERING NUMBER: M5480 B7

ABSOLUTE MAXIMUM RATINGS

V_{DD}	Supply voltage	-0.3 to 15	V
V_I	Input voltage	-0.3 to 15	V
$V_{O(off)}$	Off state output voltage	15	V
I_O	Output sink current	40	mA
P_{tot}	Total package power dissipation	at 25°C	940 mW
		at 85°C	490 mW
T_j	Junction temperature	150	°C
T_{op}	Operating temperature range	-25 to 85	°C
T_{stg}	Storage temperature range	-65 to 150	°C

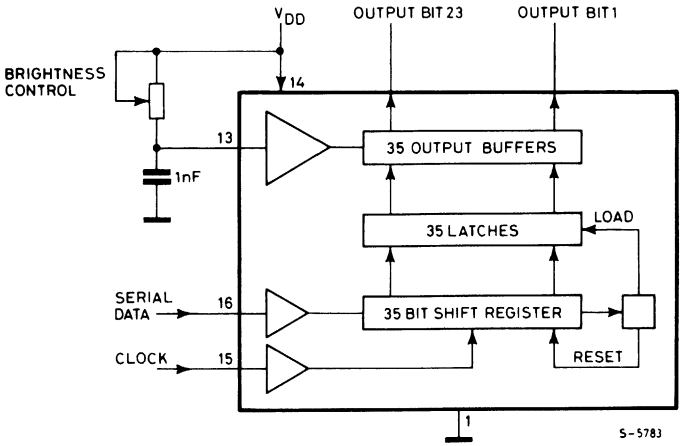
Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CONNECTION DIAGRAM



BLOCK DIAGRAM

Fig. 1



STATIC ELECTRICAL CHARACTERISTICS (T_{amb} within operating range, V_{DD}= 4.75V to 13.2V, V_{SS}= 0V, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.75		13.2	V
I_{DD}	Supply Current	V_{DD}= 13.2V			7	mA
V_I	Input Voltages Logical "0" Level Logical "1" Level	 ± 10 μA Input Bias 4.75 ⩽ V_{DD} ⩽ 5.25 V_{DD} > 5.25	 -0.3 2.2 V_{DD}-2		 0.8 V_{DD} V_{DD}	 V V V
I_B	Brightness Input Current (note 2)		0		0.75	mA
V_B	Brightness Input Voltage (pin 13)	Input Current = 750 μA	3		4.3	V
$V_{O(off)}$	Off State Output Voltage				13.2	V
I_O	Output Sink Current (note 3) Segment OFF Segment ON	 V_O = 3V V_O = 1V (note 4) Brightness In. = 0 μA Brightness In. = 100 μA Brightness In. = 750 μA	 0 2 12	 2.7 15	 10 10 4 25	 μA μA mA mA
f_{clock}	Input Clock Frequency		0		0.5	MHz
I_O	Output Matching (note 1)				+ 20	%

Notes: 1. Output matching is calculated as the percent variation from $I_{MAX} + I_{MIN}/2$.
2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.
3. Absolute maximum for each output should be limited to 40 mA.
4. The V_O voltage should be regulated by the user.

FUNCTIONAL DESCRIPTION

The M5480 is specifically designed to operate $3^1/_2$ digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display.
Outputs change only if the serial data bits differ from the previous time.
Display brightness is determined by control of the output current for LED displays. A 1nF capacitor should be connected to brightness control, pin 13, to prevent possible oscillations.

A block diagram is shown in figure 1. The output current is typically 20 times greater than the current into pin 13, which is set by an external variable resistor.
There is an internal limiting resistor of 400Ω nominal value.

FUNCTIONAL DESCRIPTION (continued)

Figure 2 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.
At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configurations. There is no clear for the master portion of the first register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 3 shows the timing relationships between Data, and Clock. A maximum clock frequency of 0.5 MHz is assumed.

Figure 4 shows the Output Data Format for the 5480.Because it uses only 23 of the possible 35 outputs, 12 of the bits are "Don't Care".

For applications where a lesser number of outputs are used, it is possible to either increase the current per output, or operate the part at higher than 1V V_{OUT}.
The following equation can be used for calculations.

$$T_j = [\ (V_{OUT})\ (I_{LED})\ (\text{No. of segments}) + V_{DD} \cdot 7\ \text{mA}\ ]\ (132\ °C/W) + T_{amb}$$

where:

T_j = junction temperature (150°C max)

V_{OUT}= the voltage at the LED driver outputs

I_{LED} = the LED current

132°C/W = thermal coefficient of the package

T_{amb}= ambient temperature

Fig. 2 - Input Data Format

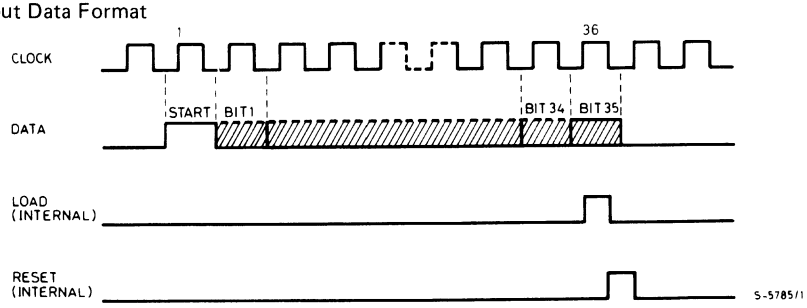


Fig. 3

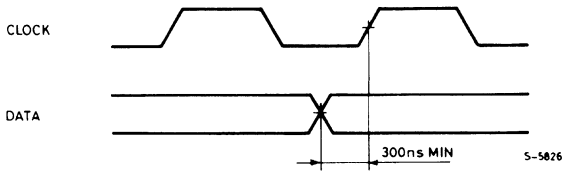
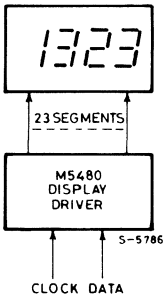


Fig. 4 - Serial Data Bus/Outputs Correspondence

5451	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	START
5480	X	23	22	21	20	19	X	X	18	X	17	16	15	14	13	12	X	X	X	X	11	10	9	8	X	X	X	7	6	5	4	3	2	1	X	START

TYPICAL APPLICATION

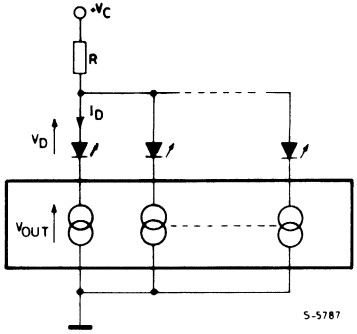
BASIC $3^1/_2$ Digit interface.



POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

a)

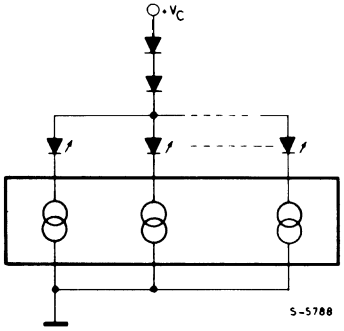


In this application R must be chosen taking into account the worst operating conditions.
R is determined by the maximum number of segments activated.

$$R = \frac{V_C - V_{D\ MAX} - V_{OUT\ MIN}}{N_{MAX} \cdot I_D}$$

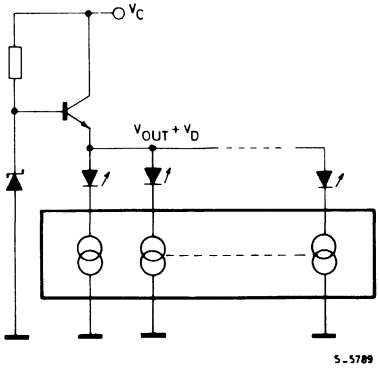
The worst case condition for the device is when roughly half of the maximum number of segments are activated.
It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.
In critical cases more resistors can be used in conjunction with groups of segments.
In this case the current variation in the single resistor is reduced and P_{tot} limited.

b)



In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.
The total power dissipation of the IC depends, in a first approximation, only on the number of segments activated.

c)



In this configuration $V_{OUT}+V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.

M5481

LED DISPLAY DRIVER

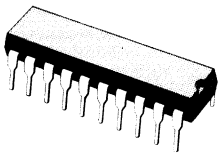
- 2 DIGIT LED DRIVER (14 SEGMENTS)
- CURRENT GENERATOR OUTPUTS (NO RESISTOR REQUIRED)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- DATA ENABLE
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

Application examples:

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATOR
- RELAY DRIVER
- INSTRUMENTATION READOUTS

The M5481 is a monolithic MOS integrated circuit produced with a N-channel silicon gate technology. It utilizes the M5450 die packaged in a 20-pin plastic package copper frame, making it ideal for a 2-digit display. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected either to V_{DD} or to a separate supply of 13.2V maximum.

The M5481 is a pin-to-pin replacement of the NS MM 5481.



DIP-20 Plastic
(0.25)

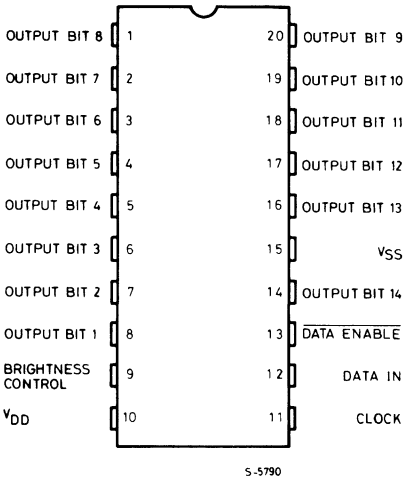
ORDERING NUMBER: M5481 B7

ABSOLUTE MAXIMUM RATINGS

V_{DD}	Supply voltage	-0.3 to 15	V
V_I	Input voltage	-0.3 to 15	V
$V_{O\,(off)}$	Off state output voltage	15	V
I_O	Output sink current	40	mA
P_{tot}	Total package power dissipation	at 25°C	1.5W
		at 85°C	800 mW
T_j	Junction temperature	150	°C
T_{op}	Operating temperature range	-25 to 85	°C
T_{stg}	Storage temperature range	-65 to 150	°C

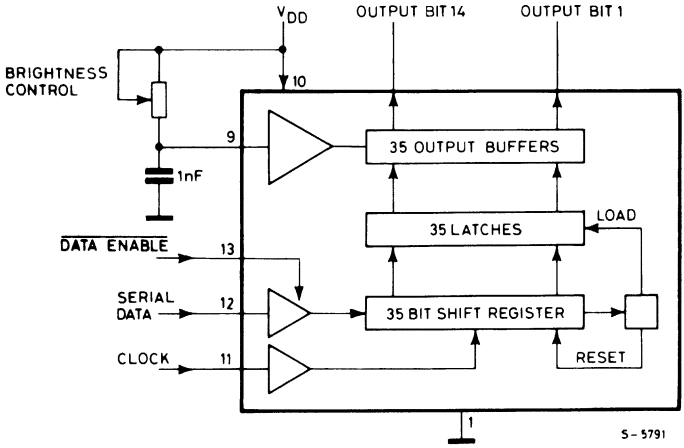
Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CONNECTION DIAGRAM



BLOCK DIAGRAM

Fig. 1



STATIC ELECTRICAL CHARACTERISTICS (T_{amb} within operating range, V_{DD}= 4.75V to 13.2V, V_{SS}= 0V, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.75		13.2	V
I_{DD}	Supply Current	V_{DD}= 13.2V			7	mA
V_I	Input Voltages Logical "0" Level Logical "1" Level	± 10 μA Input Bias 4.75 ⩽ V_{DD} ⩽ 5.25 V_{DD} > 5.25	 -0.3 2.2 V_{DD}-2		 0.8 V_{DD} V_{DD}	 V V V
I_B	Brightness Input Current (note 2)		0		0.75	mA
V_B	Brightness Input Voltage (pin 9)	Input Current = 750 μA	3		4.3	V
$V_{O(off)}$	Off State Output Voltage				13.2	V
I_O	Output Sink Current (note 3) Segment OFF Segment ON	 V_O = 3V V_O = 1V (note 4) Brightness In. = 0 μA Brightness In. = 100 μA Brightness In. = 750 μA	 0 2 12	 2.7 15	 10 10 4 25	 μA μA mA mA
f_{clock}	Input Clock Frequency		0		0.5	MHz
I_O	Output Matching (note 1)				± 20	%

Notes: 1. Output matching is calculates as the percent variation from I_{MAX} + I_{MIN}/2.
2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.
3. Absolute maximum for each output should be limited to 40 mA.
4. The V_O voltage should be regulated by the user.

FUNCTIONAL DESCRIPTION

The M5481 uses the M5450 die which is packaged to operate 2-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal.
The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 1nF capacitor should be connected to brightness control, pin 9, to prevent possible oscillations.

A block diagram is shown in figure 1. The output current is typically 20 times greater than the current into pin 9, which is set by an external variable resistor.
These is an internal limiting resistor of 400Ω nominal value.

FUNCTIONAL DESCRIPTION (continued)

Figure 2 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.
At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master slave configurations. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 3 shows the timing relationships between Data, Clock and $\overline{\text{DATA ENABLE}}$.
A maximum clock frequency of 0.5 MHz is assumed.

Figure 4 shows the Output Data Format for the M5481. Because it uses only 14 of the possible 35 outputs, 21 of the bits are "Don't Cares".

For applications where a lesser number of outputs are used it is possible to either increase the current per output or operate the part at higher than 1V V_{OUT}.
The following equation can be used for calculations.

$$T_j \equiv [\ (V_{OUT})\ (I_{LED})\ (\text{No. of segments}) + V_{DD} \cdot 7\ \text{mA}\ ]\ (80\ ^\circ\text{C/W}) + T_{amb}$$

where:
T_j = junction temperature (150°C max)
V_{OUT} = the voltage at the LED driver outputs
I_{LED} = the LED current
80°C/W = thermal coefficient of the package
T_{amb} = ambient temperature

Fig. 2 - Input Data Format

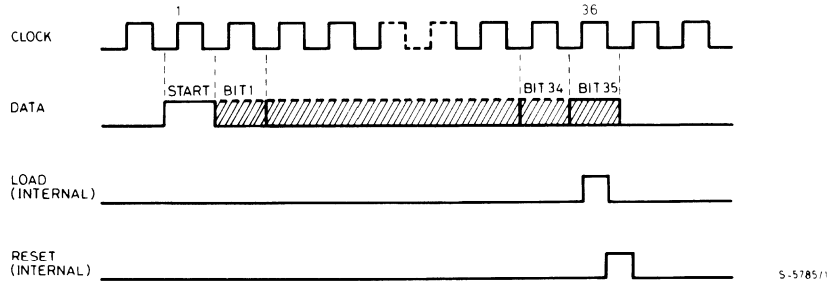


Fig. 3

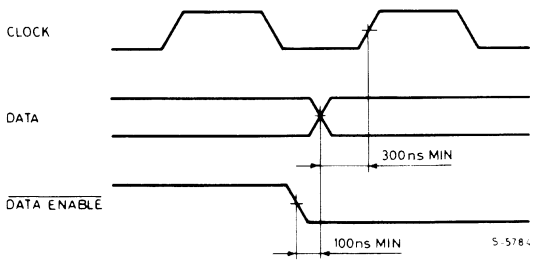
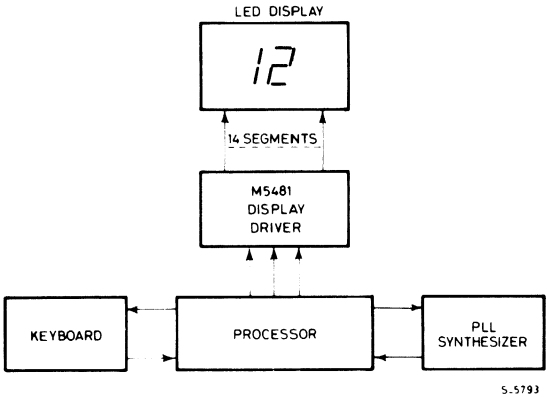


Fig. 4 - Serial Data Bus/Outputs Correspondence

5450	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	START
5481	X	X	X	X	14	13	X	X	X	X	12	11	10	9	X	X	X	X	8	7	6	5	X	X	X	X	4	3	2	1	X	X	X	X	START

TYPICAL APPLICATION

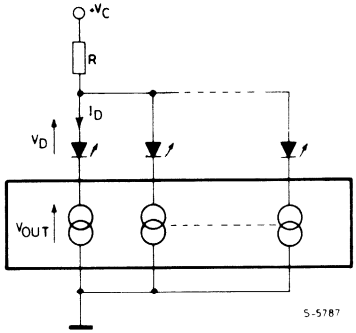
BASIC electronically tuned TV system



POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

a)

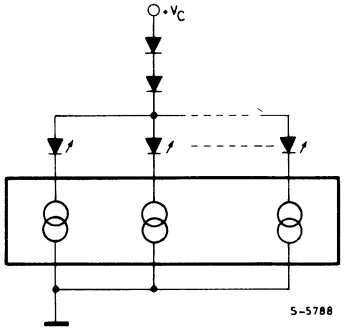


In this application R must be chosen taking into account the worst operating conditions.
R is determined by the maximum number of segments activated.

$$R = \frac{V_C - V_{D\,MAX} - V_{O\,MIN}}{N_{MAX} \cdot I_D}$$

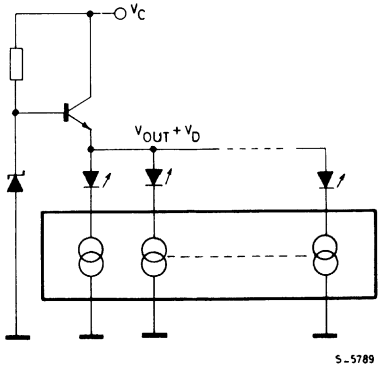
The worst case condition for the device is when roughly half of the maximum number of segments are activated.
It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.
In critical cases more resistors can be used in conjunction with groups of segments. In this case the current variation in the single resistor is reduced and P_{tot} limited.

b)



In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.
The total power dissipation of the IC is, in first approximation, depending only on the number of segments activated.

c)



In this configuration $V_{OUT} + V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.

M5482

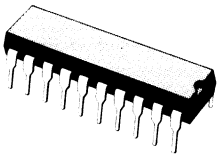
LED DISPLAY DRIVER

- 2 DIGIT LED DRIVER (15 SEGMENTS)
- CURRENT GENERATOR OUTPUTS (NO RESISTOR REQUIRED)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

Application examples:

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATOR
- RELAY DRIVER
- INSTRUMENTATION READOUTS

The M5482 is a monolithic MOS integrated circuit produced with an N-channel silicon gate technology. It utilizes the M5450 die packaged in a 20-pin plastic package copper frame, making it ideal for a 2-digit display. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected either to V_{DD} or to a separate supply of 13.2V maximum.



DIP-20 Plastic
(0.25)

ORDERING NUMBER: M5482 B7

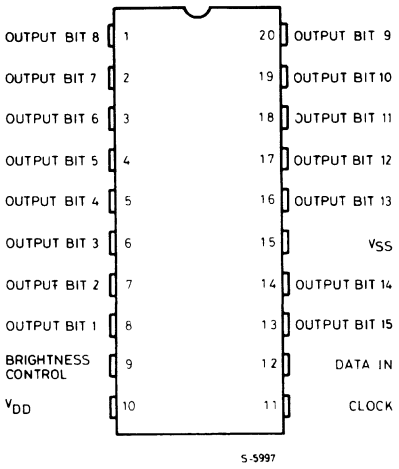
ABSOLUTE MAXIMUM RATINGS

V_{DD}	Supply voltage	-0.3 to 15	V
V_I	Input voltage	-0.3 to 15	V
$V_{O(off)}$	Off state output voltage	15	V
I_O	Output sink current	40	mA
P_{tot}	Total package power dissipation	at 25°C	1.5W
		at 85°C	800 mW
T_j	Junction temperature	150	°C
T_{op}	Operating temperature range	-25 to 85	°C
T_{stg}	Storage temperature range	-65 to 150	°C

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

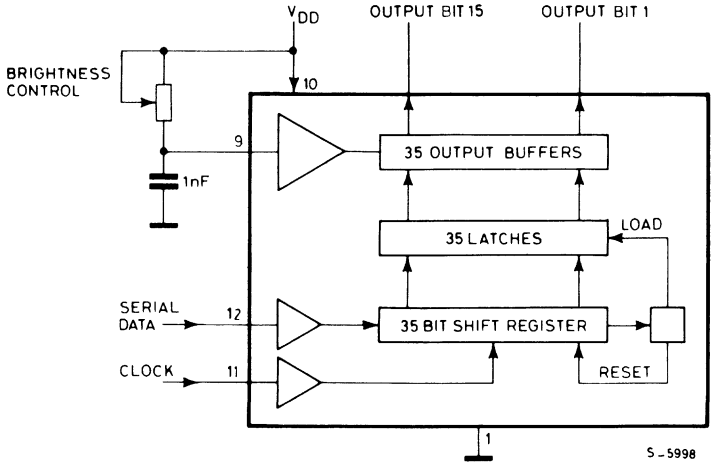
M5482

CONNECTION DIAGRAM



BLOCK DIAGRAM

Fig. 1



STATIC ELECTRICAL CHARACTERISTICS (T_{amb} within operating range, V_{DD}= 4.75V to 13.2V, V_{SS}= 0V, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.75		13.2	V
I_{DD}	Supply Current	V_{DD}= 13.2V			7	mA
V_I	Input Voltages Logical "0" Level Logical "1" Level	± 10 μA Input Bias 4.75 ≤ V_{DD} ≤ 5.25 V_{DD} > 5.25	 -0.3 2.2 V_{DD}-2		 0.8 V_{DD} V_{DD}	 V V V
I_B	Brightness Input Current (note 2)		0		0.75	mA
V_B	Brightness Input Voltage (pin 9)	Input Current = 750 μA	3		4.3	V
$V_{O(off)}$	Off State Output Voltage				13.2	V
I_O	Output Sink Current (note 3) Segment OFF Segment ON	 V_O = 3V V_O = 1V (note 4) Brightness In. = 0 μA Brightness In. = 100 μA Brightness In. = 750 μA	 0 2 12	 2.7 15	 10 10 4 25	 μA μA mA mA
f_{clock}	Input Clock Frequency		0		0.5	MHz
I_O	Output Matching (note 1)				± 20	%

Notes: 1. Output matching is calculated as the percent variation from I_{MAX} + I_{MIN}/2.
2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.
3. Absolute maximum for each output should be limited to 40 mA.
4. The V_O voltage should be regulated by the user.

FUNCTIONAL DESCRIPTION

The M5482 uses the M5451 die which is packaged to operate 2-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal.
The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 1nF capacitor should be connected to brightness control, pin 9, to prevent possible oscillations.

A block diagram is shown in figure 1. The output current is typically 20 times greater than the current into pin 9, which is set by an external variable resistor.
There is an internal limiting resistor of 400Ω nominal value.

FUNCTIONAL DESCRIPTION (continued)

Figure 2 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.
At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master slave configurations. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 3 shows the timing relationships between Data and Clock.
A maximum clock frequency of 0.5 MHz is assumed.

Figure 4 shows the Output Data Format for the M5482. Because it uses only 15 of the possible 35 outputs, 20 of the bits are "Don't Cares".

For applications where a lesser number of outputs are used it is possible to either increase the current per output or operate the part at higher than 1V V_{OUT}.
The following equation can be used for calculations.

$$T_j \equiv [\ (V_{OUT})\ (I_{LED})\ (\text{No. of segments}) + V_{DD} \cdot 7\ \text{mA}\ ]\ (80\ ^\circ\text{C/W}) + T_{amb}$$

where:
T_j = junction temperature (150°C max)
V_{OUT} = the voltage at the LED driver outputs
I_{LED} = the LED current
80°C/W = thermal coefficient of the package
T_{amb} = ambient temperature

Fig. 2 - Input Data Format

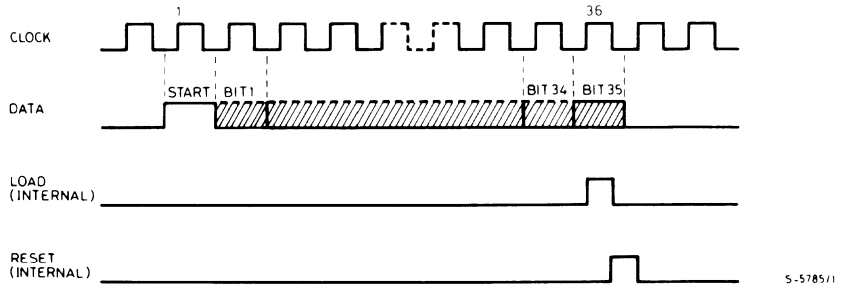


Fig. 3

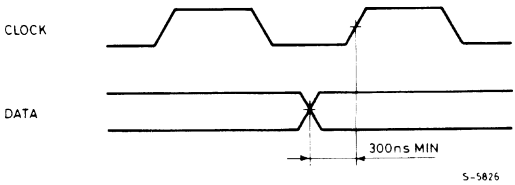
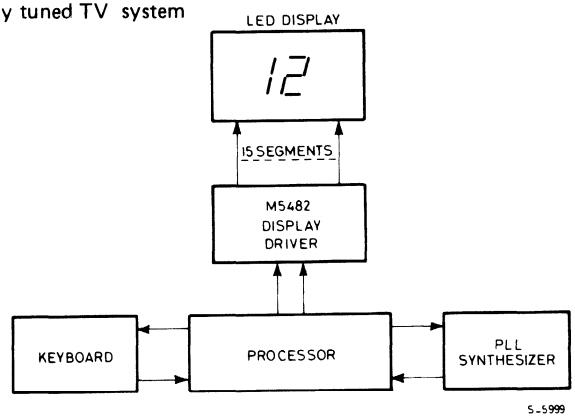


Fig. 4 - Serial Data Bus/Outputs Correspondence

5451	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	START
5482	15	X	X	X	X	14	13	X	X	X	X	12	11	10	9	X	X	X	X	8	7	6	5	X	X	X	X	4	3	2	1	X	X	X	X	START

TYPICAL APPLICATION

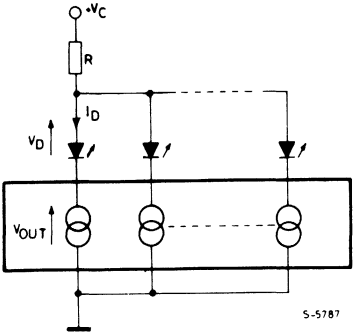
BASIC electronically tuned TV system



POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

a)

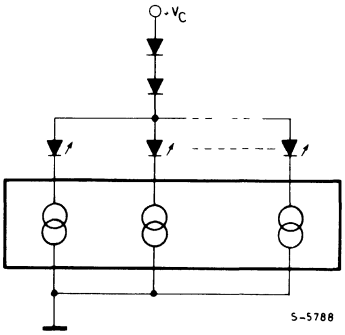


In this application R must be chosen taking into account the worst operating conditions.
R is determined by the maximum number of segments activated.

$$R = \frac{V_C - V_{D\ MAX} - V_{O\ MIN}}{N_{MAX} \cdot I_D}$$

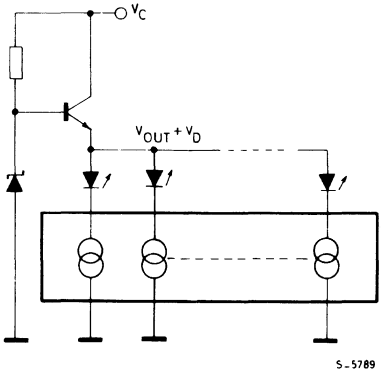
The worst case condition for the device is when roughly half of the maximum number of segments are activated.
It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.
In critical cases more resistors can be used in conjunction with groups of segments. In this case the current variation in the single resistor is reduced and P_{tot} limited.

b)



In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.
The total power dissipation of the IC is, in first approximation, depending only on the number of segments activated.

c)



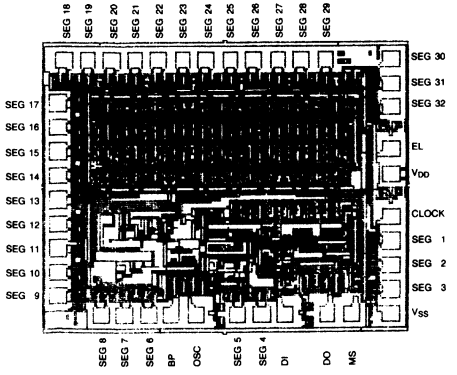
In this configuration $V_{OUT} + V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.

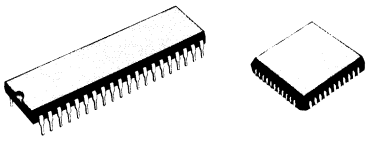
M8438A

SERIAL INPUT LCD DRIVER

- DATA TRANSFER: FIXED ENABLE MODE FOR DIP-40
- DRIVES UP TO 32 LCD SEGMENTS
- CMOS TECHNOLOGY FOR WIDE SUPPLY VOLTAGE RANGE
- CASCADABLE
- INPUTS ARE CMOS, NMOS AND TTL COMPATIBLE
- ON CHIP OSCILLATOR
- REQUIRES ONLY 3 CONTROL LINES
- −40 TO 85°C TEMPERATURE RANGE

The M8438A is a CMOS integrated circuit that drives an LCD display, usually under microprocessor control. The part acts as a smart peripheral that drives up to 32 LCD segments. It needs only three control lines due to its serial input construction. It latches the data to be displayed and relieves the microprocessor from the task of generating the required waveforms.
The M8438A can drive any standard or custom parallel drive LCD whether it be field effect or dynamic scattering. Several drivers can be cascaded, if more than 32 segments are to be driven. The AC frequency of the LCD waveforms can be supplied by the user or can be generated by attaching a capacitor to the OSC input which determines the frequency of an internal oscillator.
The M8438A is available in DIE form, assembled in 40 pin dual-in line plastic or 44 PLCC packages.





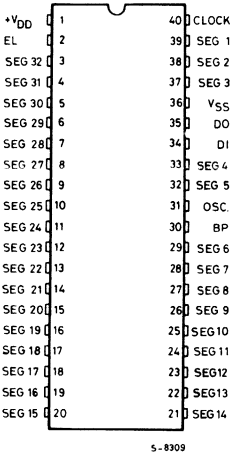
B DIP-40 Plastic

C 44 PLCC Plastic Chip Carrier

ORDERING NUMBERS: M8438A DIE1
M8436A B6
M8436A C6

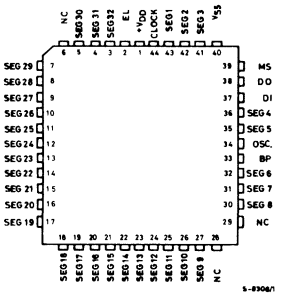
PIN CONFIGURATION

DUAL IN LINE



5-8309

CHIP CARRIER



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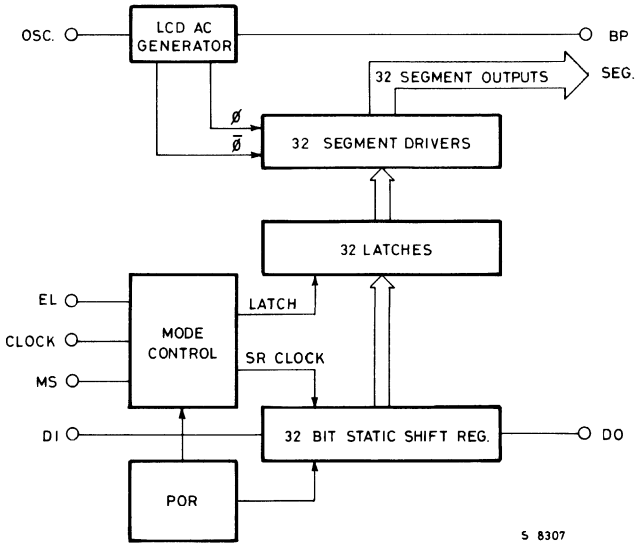
BLOCK DIAGRAM



OSC :Oscillator (capacitor or drive signal)
EL :Enable/Latch control input
MS :Mode select input (not available in 40 Pin DIL)
DI :Serial data input
DO :Serial data output
BP :Backplane output
SEG :Segment output signal

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
(VDD-VSS)	Supply voltage	−0.3 to +12	V
V_I	Input voltage	VSS−0.3 to VDD+0.3	V
V_O	Output voltage	VSS−0.3 to VDD+0.3	V
P_D	Power dissipation	250	mW
T_{stg}	Storage temperature	−55 to +125	°C
T_A	Operating temperature	−40 to +85	°C

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C and V_{DD} = 5V unless otherwise noted)

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Test Condition	Min.	Max.	Unit
V_{DD}	Supply Voltage			3	10	V
I_{DD}	Supply Current		Oscillator f < 15kHz		60	μA
I_Q	Quiescent Current		V_{DD} = 10V		10	μA
V_{IH}	Input High Level	CLOCK DI EL		.5V_{DD}	V_{DD}	V
V_{IL}	Input Low Level	CLOCK DI EL		0	.2V_{DD}	V
I_{IN}	Input Current	CLOCK DI EL			±5	μA
C_I	Input Capacitance	CLOCK DI EL			5	pF
V_{IH}	Input High Level	OSC	Driven mode	.9V_{DD}		V
V_{IL}	Input Low Level	OSC	Driven mode		.1V_{DD}	V
I_{IN}	Input Current	OSC	Driven mode		±10	μA
R_{ON}	Segment Output Impedance		I_{IL} = 10μA		40	kΩ
R_{ON}	Backplane Output Impedance		I_L = 100μA		3	kΩ
V_{OFF}	Output Offset Voltage		C_L = 250pF between each SEG output and BP		±50	mV
R_{ON}	Data Output Impedance		I_L = 100μA		3	kΩ

DYNAMIC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Max.	Unit
t_{TR}	Transition Time OSC	Driven mode		500	ns
t_{SD}	Data Set-up Time	Fig. 1 and 2	150		ns
t_{HD}	Data Hold Time	Fig. 1 and 2	50		ns
t_{SE}	EL Set-up Time	Fig. 1	100		ns
t_{HE}	EL Hold Time	Fig. 1	100		ns
t_{WE}	EL Pulse Width	Fig. 2	175		ns
t_{CE}	Clock to EL Time	Fig. 2	250		ns
t_{pd}	DO Propagation Delay	Fig. 1, 2; C_L = 55pF		500	ns
f	Clock Rate	V_{DD} = 10 50% duty cycle;	DC	1.5	MHz

FUNCTIONAL DESCRIPTION

LCD-AC-GENERATOR

This block generates a 50% duty cycle signal for the backplane output. The circuit can be used in two different modes: oscillator or driven.

OSCILLATOR MODE:

In this mode the backplane frequency is determined by the internal RC oscillator together with an 8-stage frequency divider. For generating the backplane output signal of 50% duty cycle the oscillator frequency is divided by 256. The RC oscillator requires an external capacitor to be connected between input OSC and VSS. A value of 18pF gives a backplane frequency of 80Hz ± 30% at VDD = 5V. The variation of the backplane frequency over the entire temperature and supply voltage range is ± 50%.

DRIVEN MODE:

In this mode the signal at the backplane output BP is in phase with an external driving signal applied to input OSC. This mode is used to synchronize the LCD drive of two or more cascaded driver circuits.

FUNCTIONAL DESCRIPTION (continued)

DETECTION LOGIC

The circuit is able to distinguish between the conditions for oscillator or driven mode. If the circuit is to be in the oscillator mode, the OSC pin has a capacitor connected to it. The oscillator will start as soon as the supply voltage exceeds a certain minimim value. The signal at pin OSC swings within a range from $0.3V_{DD}$ to $0.7V_{DD}$. If the circuit is to be in the driven mode, the OSC pin has to be forced to logic levels by an external source. The transition time between the logic levels must be short, so that the circuit does not react on the voltage level in between. In the driven mode the 8-stage frequency divider is by-passed.

SEGMENT OUTPUTS

A logic 0 at the data input DI causes a segment output signal to be in phase with the backplane signal and turns the segment off. A logic 1 causes a segment output to be in opposite phase to the backplane signal and turns the segment on.

MICROPROCESSOR INTERFACE

The circuit can operate in two different data transfer modes: Enable mode and latch mode. One of either mode can be chosen with the mode select input MS. An internal pull up device is provided between this input and VDD. Enable mode is selected if MS is left open or connected to VDD.
Latch mode is selected if MS is connected to VSS.
The input MS is not available, if the device is assembled in the 40 pin package, and is internally fixed to operate in ENABLE MODE.

ENABLE MODE

Fig. 3 shows a timing diagram of the enable mode. Data is serially shifted in and out of the shift register on the negative transition of the clock.
Serial entry into the shift register is permitted when the enable/latch control EL is high. When EL is low it causes the shift register clock to be inhibited and the content of the shift register to be loaded into the latches that control the segment drivers.

LATCH MODE

Fig. 4 shows a timing diagram of the latch mode. Data is serially shifted in and out of the shift register on the negative transition of the clock.
Serial entry into the shift register is permitted independently of the enable/latch control EL. When EL is high it causes a parallel load of the content in the shift register into the latches. It is acceptable to tie the EL line high. Then the latches are transparent and only two lines, clock and data input, would then be needed for data transfer.

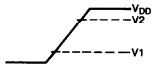
POWER-ON LOGIC

A power on reset pulse is generated internally when the supply voltage is being turned on. The generation of the reset pulse is level dependent and will occur even on a slowly rising supply voltage.
The power on reset pulse resets all shift register stages and the latches that control the segment drivers. Therefore all segment outputs are initially in phase with the backplane output. This causes the display to be blanked and no arbitrary data to show up. This condition is maintained until data is shifted into the register and loaded into the latches.

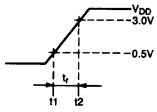
CONDITIONS FOR POWER-ON RESET FUNCTION

The POR circuit triggers on the rising slope of the positive supply voltage V_{DD}. A reset pulse will be generated, if conditions a) through d) are given:

a) Level
Rising slope from V1 to V2
V1 max = 0.5V
V2 min = 3.0V



b) Rise time
t_r min = 10 μs
t_r max = 1 s



c) Rise function
The function of V_{DD} between t1 und t2 may be nonlinear, but should not show a maximum and should not exceed 0.25 V/μs.

d) Recovery time
The minimum time between turn-off and turn-on of V_{DD} is 1s.

CASCADE CONFIGURATION

Several LCD drivers can be cascaded if a liquid crystal display with more than 32 segments is to be connected.
The phase correlation between all segment outputs is achieved by using the second (and any other) device in the driven mode.
Two different cascade configurations can be chosen depending whether the LCD frequency is to be determined by the internal RC oscillator or by an external signal.
Figure 5 shows the connection scheme for a self oscillating configuration, figure 6 shows the connection of an externally controlled one.

Fig. 1 - Timing diagram of enable mode: set-up and hold time

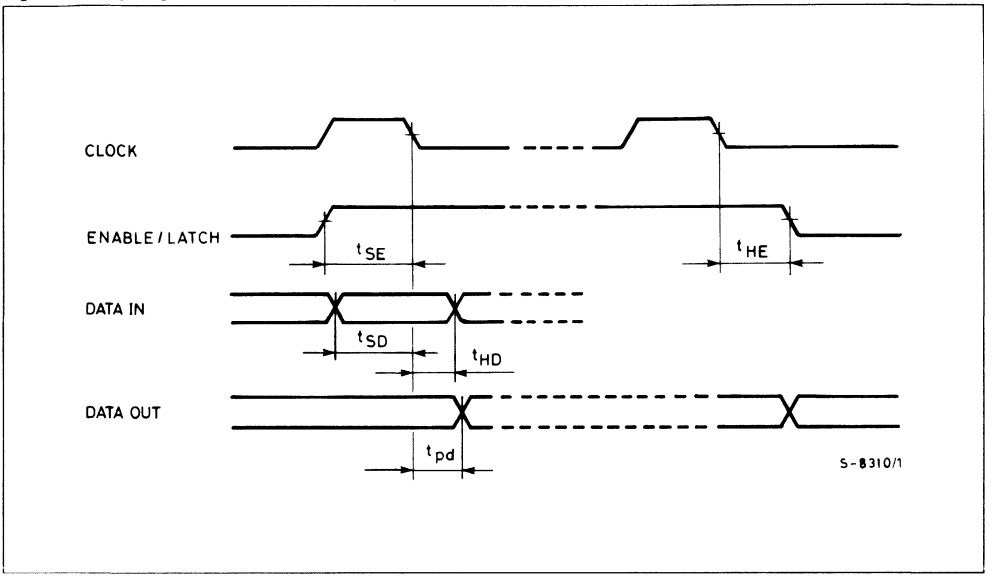


Fig. 2 - Timing diagram of latch mode: set-up and hold time

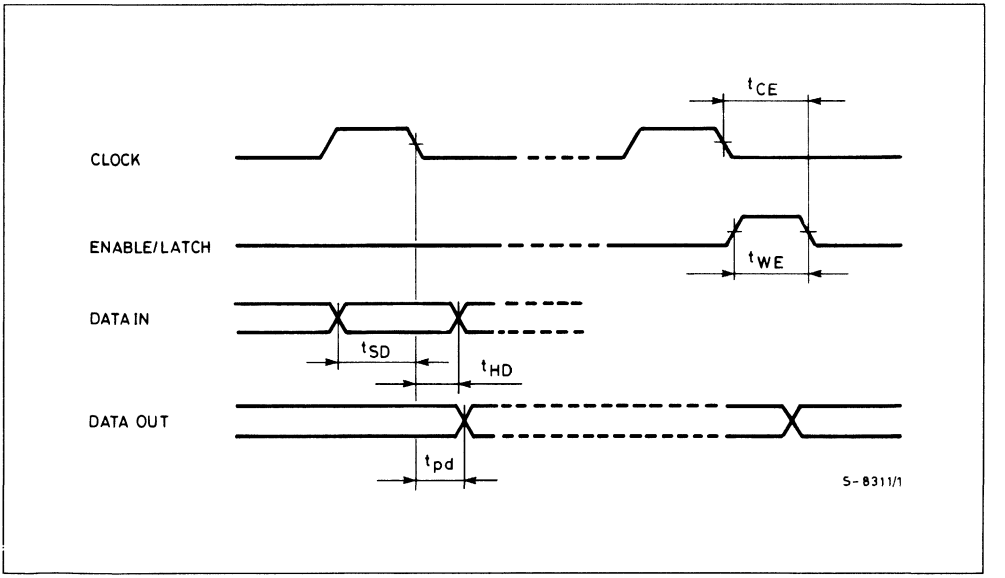


Fig. 3 - Timing diagram of enable mode: Serial load into SR and parallel transfer to LCD

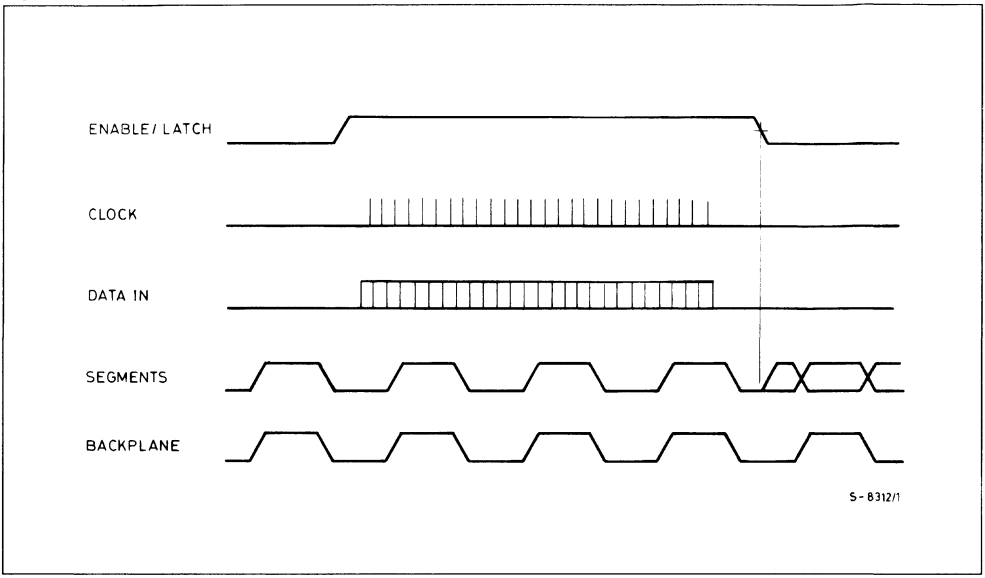


Fig. 4 - Timing diagram of latch mode: Serial load into SR and parallel transfer to LCD

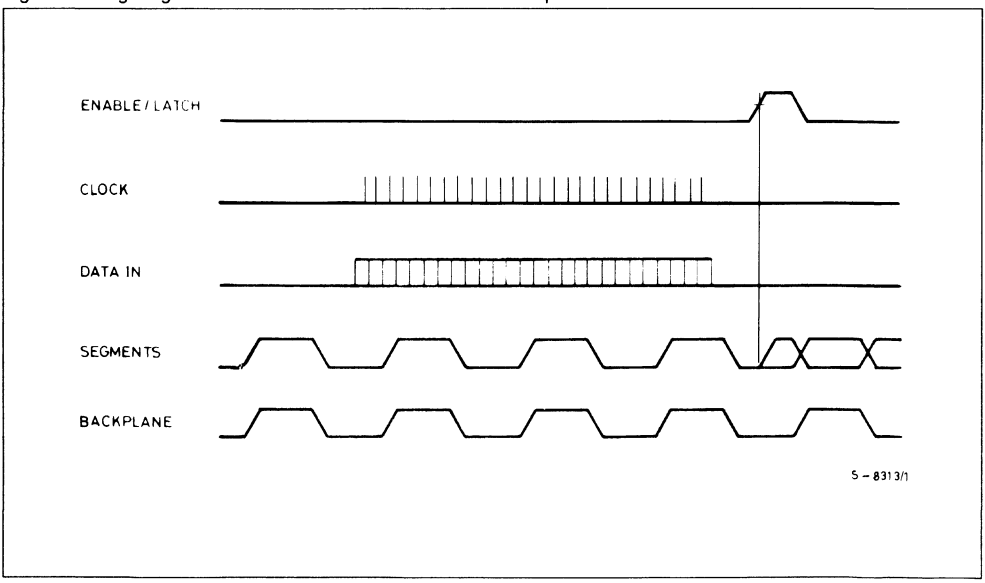


Fig. 5 - Cascade configuration, self oscillating

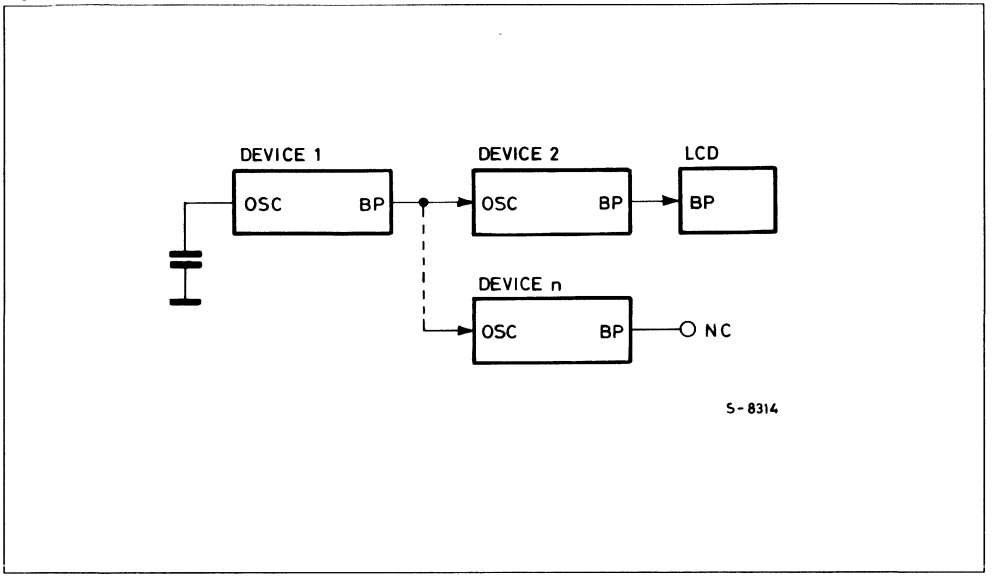
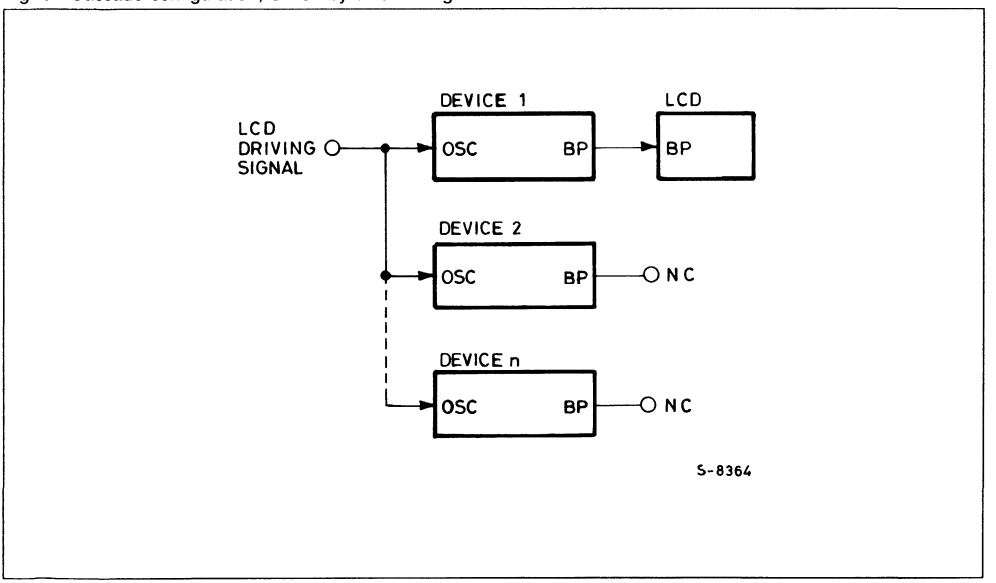


Fig. 6 - Cascade configuration, driven by external signal

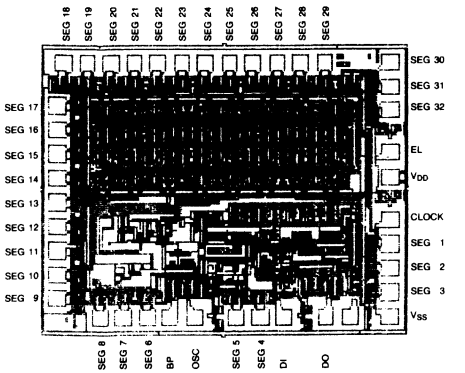


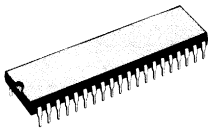
M8439

SERIAL INPUT LCD DRIVER

- **DATA TRANSFER: LATCH MODE**
- DRIVES UP TO 32 LCD SEGMENTS
- CMOS TECHNOLOGY FOR WIDE SUPPLY VOLTAGE RANGE
- CASCADABLE
- INPUTS ARE CMOS, NMOS AND TTL COMPATIBLE
- ON CHIP OSCILLATOR
- REQUIRES ONLY 3 CONTROL LINES
- −40 TO 85°C TEMPERATURE RANGE

The M8439 is a CMOS integrated circuit that drives an LCD display, usually under microprocessor control. The part acts as a smart peripheral that drives up to 32 LCD segments. It needs only three control lines due to its serial input construction. It latches the data to be displayed and relieves the microprocessor from the task of generating the required waveforms.
The M8439 can drive any standard or custom parallel drive LCD whether it be field effect or dynamic scattering. Several drivers can be cascaded, if more than 32 segments are to be driven. The AC frequency of the LCD waveforms can be supplied by the user or can be generated by attaching a capacitor to the OSC input which determines the frequency of an internal oscillator.
The M8439 is available in DIE form and assembled in 40 pin dual-in line plastic.

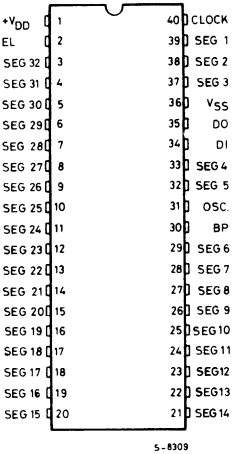




Plastic DIP-40

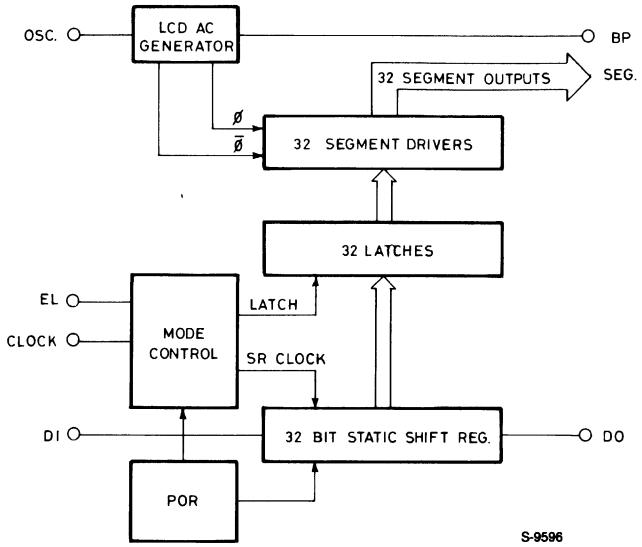
ORDERING NUMBERS: M8439 B6
M8439 DIE1

PIN CONNECTIONS



5-8309

BLOCK DIAGRAM



OSC :Oscillator (capacitor or drive signal)
EL :Enable/Latch control input
DI :Serial data input
DO :Serial data output
BP :Backplane output
SEG :Segment output signal

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
(VDD-VSS)	Supply voltage	−0.3 to +12	V
V_I	Input voltage	VSS−0.3 to VDD+0.3	V
V_O	Output voltage	VSS−0.3 to VDD+0.3	V
P_D	Power dissipation	250	mW
T_{stg}	Storage temperature	−55 to +125	°C
T_A	Operating temperature	−40 to +85	°C

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C and V_{DD} = 5V unless otherwise noted)

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Test Condition	Min.	Max.	Unit
V_{DD}	Supply Voltage			3	10	V
I_{DD}	Supply Current		Oscillator f < 15kHz		60	μA
I_Q	Quiescent Current		V_{DD} = 10V		10	μA
V_{IH}	Input High Level	CLOCK DI EL		.5V_{DD}	V_{DD}	V
V_{IL}	Input Low Level	CLOCK DI EL		0	.2V_{DD}	V
I_{IN}	Input Current	CLOCK DI EL			±5	μA
C_I	Input Capacitance	CLOCK DI EL			5	pF
V_{IH}	Input High Level	OSC	Driven mode	.9V_{DD}		V
V_{IL}	Input Low Level	OSC	Driven mode		.1V_{DD}	V
I_{IN}	Input Current	OSC	Driven mode		±10	μA
R_{ON}	Segment Output Impedance		I_{IL} = 10μA		40	kΩ
R_{ON}	Backplane Output Impedance		I_L = 100μA		3	kΩ
V_{OFF}	Output Offset Voltage		C_L = 250pF between each SEG output and BP		±50	mV
R_{ON}	Data Output Impedance		I_L = 100μA		3	kΩ

DYNAMIC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Max.	Unit
t_{TR}	Transition Time OSC	Driven mode		500	ns
t_{SD}	Data Set-up Time	Fig. 1 and 2	150		ns
t_{HD}	Data Hold Time	Fig. 1 and 2	50		ns
t_{SE}	EL Set-up Time	Fig. 1	100		ns
t_{HE}	EL Hold Time	Fig. 1	100		ns
t_{WE}	EL Pulse Width	Fig. 2	175		ns
t_{CE}	Clock to EL Time	Fig. 2	250		ns
t_{pd}	DO Propagation Delay	Fig. 1, 2; C_L = 55pF		500	ns
f	Clock Rate	V_{DD} = 10 50% duty cycle;	DC	1.5	MHz

FUNCTIONAL DESCRIPTION

LCD-AC-GENERATOR

This block generates a 50% duty cycle signal for the backplane output. The circuit can be used in two different modes: oscillator or driven.

OSCILLATOR MODE:

In this mode the backplane frequency is determined by the internal RC oscillator together with an 8-stage frequency divider. For generating the backplane output signal of 50% duty cycle the oscillator frequency is divided by 256. The RC oscillator requires an external capacitor to be connected between input OSC and VSS. A value of 18pF gives a backplane frequency of 80Hz ± 30% at VDD = 5V. The variation of the backplane frequency over the entire temperature and supply voltage range is ± 50%.

DRIVEN MODE:

In this mode the signal at the backplane output BP is in phase with an external driving signal applied to input OSC. This mode is used to synchronize the LCD drive of two or more cascaded driver circuits.

FUNCTIONAL DESCRIPTION (continued)

DETECTION LOGIC

The circuit is able to distinguish between the conditions for oscillator or driven mode. If the circuit is to be in the oscillator mode, the OSC pin has a capacitor connected to it. The oscillator will start as soon as the supply voltage exceeds a certain minimim value. The signal at pin OSC swings within a range from $0.3V_{DD}$ to $0.7V_{DD}$. If the circuit is to be in the driven mode, the OSC pin has to be forced to logic levels by an external source. The transition time between the logic levels must be short, so that the circuit does not react on the voltage level in between. In the driven mode the 8-stage frequency divider is by-passed.

SEGMENT OUTPUTS

A logic 0 at the data input DI causes a segment output signal to be in phase with the backplane signal and turns the segment off. A logic 1 causes a segment output to be in opposite phase to the backplane signal and turns the segment on.

MICROPROCESSOR INTERFACE

Fig. 2 shows a timing diagram.
Data is serially shifted in and out of the shift register on the negative transition of the clock.
Serial entry into the shift register is permitted independently of the enable/latch control EL. When EL is high it causes a parallel load of the content in the shift register into the latches. It is acceptable to tie the EL line high. Then the latches are transparent and only two lines, clock and data input, would then be needed for data transfer.

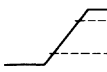
POWER-ON LOGIC

A power on reset pulse is generated internally when the supply voltage is being turned on. The generation of the reset pulse is level dependent and will occur even on a slowly rising supply voltage.
The power on reset pulse resets all shift register stages and the latches that control the segment drivers. Therefore all segment outputs are initially in phase with the backplane output. This causes the display to be blanked and no arbitrary data to show up. This condition is maintained until data is shifted into the register and loaded into the latches.

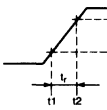
CONDITIONS FOR POWER-ON RESET FUNCTION

The POR circuit triggers on the rising slope of the positive supply voltage V_{DD}. A reset pulse will be generated, if conditions a) through d) are given:

a) Level
Rising slope from V1 to V2
V1 max = 0.5V
V2 min = 3.0V



b) Rise time
t_r min = 10 μs
t_r max = 1 s



c) Rise function
The function of V_{DD} between t1 und t2 may be nonlinear, but should not show a maximum and should not exceed 0.25 V/μs.

d) Recovery time
The minimum time between turn-off and turn-on of V_{DD} is 1s.

CASCADE CONFIGURATION

Several LCD drivers can be cascaded if a liquid crystal display with more than 32 segments is to be connected.
The phase correlation between all segment outputs is achieved by using the second (and any other) device in the driven mode.
Two different cascade configurations can be chosen depending whether the LCD frequency is to be determined by the internal RC oscillator or by an external signal.
Figure 3 shows the connection scheme for a self oscillating configuration, figure 4 shows the connection of an externally controlled one.

Fig. 1 - Timing diagram of latch mode: set-up and hold time

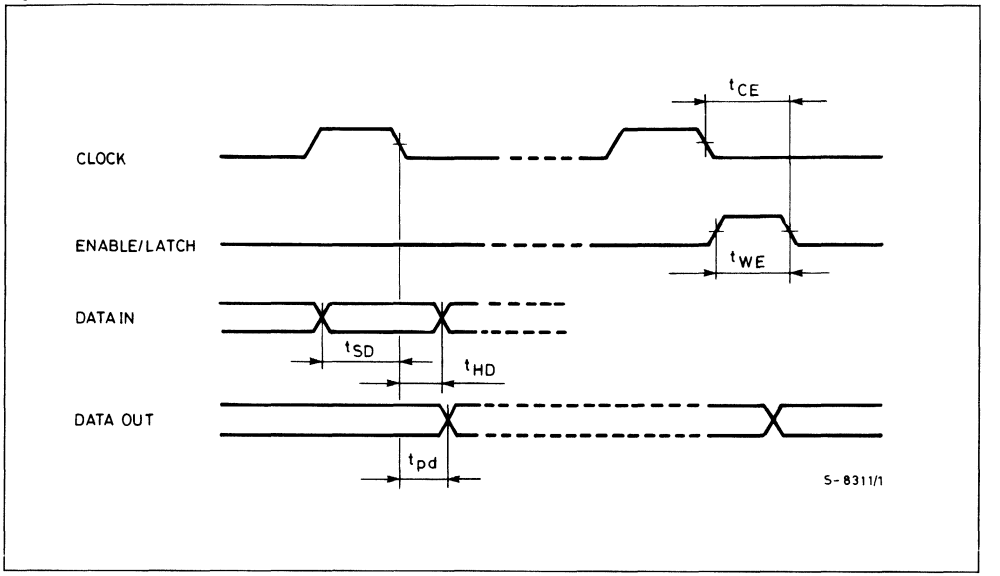


Fig. 2 - Timing diagram of latch mode: Serial load into SR and parallel transfer to LCD

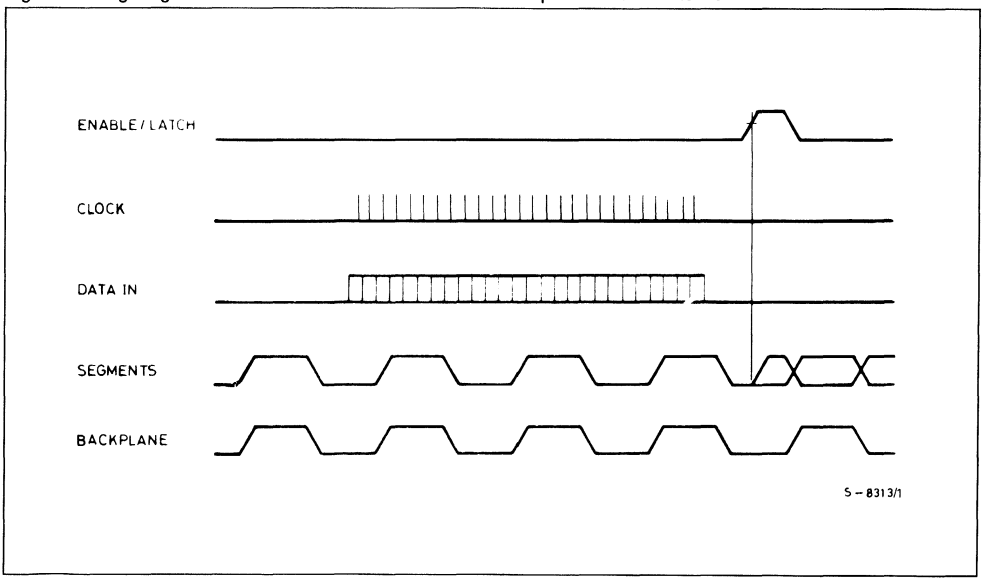


Fig. 3 - Cascade configuration, self oscillating

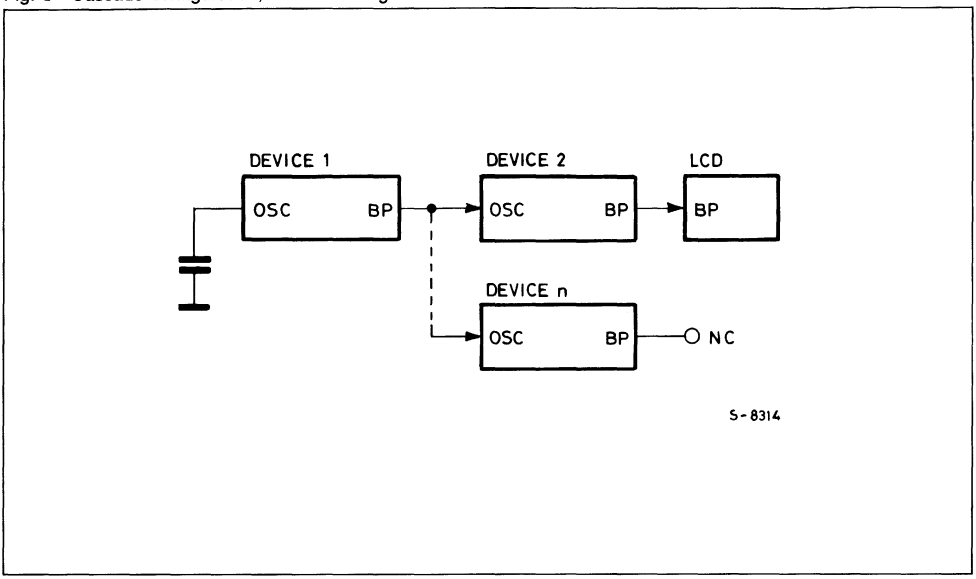
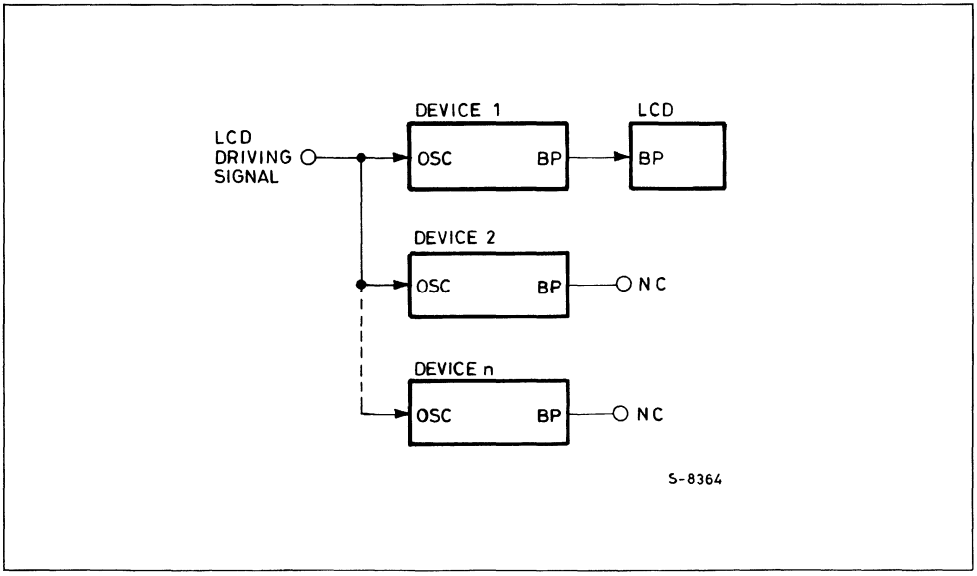


Fig. 4 - Cascade configuration, driven by external signal

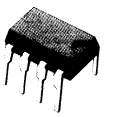


MC1458
MC1558

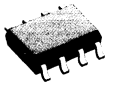
DUAL OPERATIONAL AMPLIFIERS

- INTERNALLY COMPENSATED
- SHORT-CIRCUIT PROTECTED
- LOW POWER CONSUMPTION
- WIDE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- NO LATCH-UP

The MC1458 and MC1558 are dual operational amplifiers with frequency and phase compensation built into the chip, available in 8-lead minidip plastic or ceramic package and in 8-lead micropackage. They are intended for a wide range of applications where space and cost saving are the main goals. In spite of that, the MC1458/1558 offers good performance and absence of latch-up makes the device ideal for use as voltage follower integrator, summing amplifier and general feedback applications.

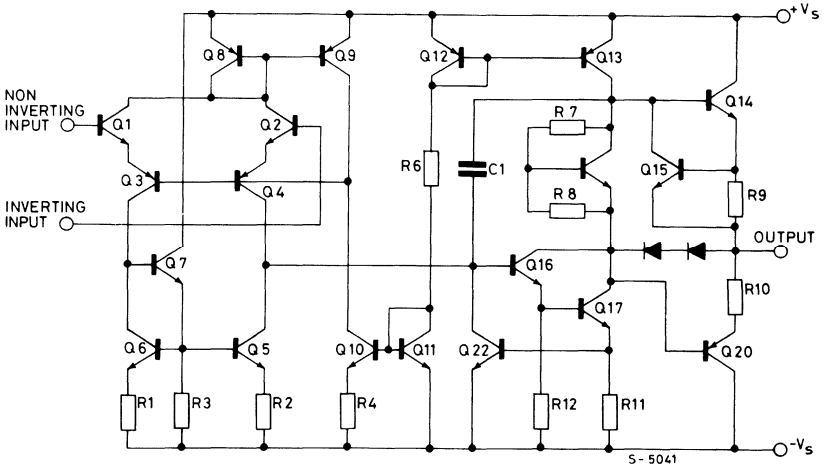


Minidip
(Plastic and Ceramic)



SO-8

SCHEMATIC DIAGRAM (one section)

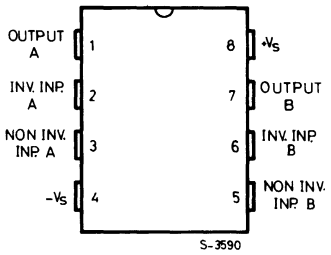


MC1458
MC1558

ABSOLUTE MAXIMUM RATINGS		MC1458/C	MC1458I	MC1558
V_s	Supply voltage	± 18V	± 18V	± 22V
V_{ID}	Input differential voltage		± 30V	
V_{ICM} *	Input common mode voltage		± 15V	
I_s **	Output short circuit duration		continuous	
T_{amb}	Operating temperature	0 to 70°C	-25 to 85°C	-55 to 125°C
T_j	Junction temperature		150°C	
T_{stg}	Storage temperature		-65 to 150°C	

* For supply voltages less than 15V, the absolute maximum input voltage is equal to the supply voltage
** Supply voltage equal to or less than 15V

CONNECTION DIAGRAM AND ORDERING NUMBERS
(top view)



Temperature range	Ceramic minidip	Plastic minidip	SO-8
Commercial 0 to 70°C	MC1458U MC1458CU	MC1458P1 MC1458CP1	MC1458D MC1458CD
Military -55 to 125°C	MC1558U	—	—
Industrial -25 to 85°C	—	—	MC1458ID

THERMAL DATA

			Plastic Minidip	Ceramic Minidip	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	120°C/W	150°C/W	200°C/W

ELECTRICAL CHARACTERISTICS (V_s= ± 15V, T_{amb}= 25°C, unless otherwise specified)

Parameter		Test conditions		MC1458/I			MC1458C			MC1558			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_s	Supply current (both amplifiers)				2.3	5.6		2.3	8		2.3	5	mA
		T_{amb} = High										4.5	
		T_{amb} = Low										6	
I_b	Input bias current				80	500		80	700		80	500	nA
		T_{amb} = High									30	500	
		T_{amb} = Low									300	1500	
		T_{amb}= 0 to 70°C				800			1000				
V_{os}	Input offset voltage	$R_g \leqslant 10K\Omega$			2	6		2	10		1	5	mV
		$R_g \leqslant 10K\Omega$ T_{amb}= full range				7.5			12		1	6	
I_{os}	Input offset current				20	200		20	300		20	200	nA
		T_{amb} = High				300			400		7	200	
		T_{amb} = Low									85	500	
		T_{amb}= 0 to 70°C				300			400				
I_{sc}	Output short circuit current				20			20			20		mA
G_v	Large signal open loop voltage gain	R_L= 2KΩ	T_{amb}= full range	83						88			dB
				86	106					94	106		
		R_L= 10KΩ	T_{amb}= full range				83						dB
							86	106					
B	Unity gain bandwidth				0.8			0.8			0.8		MHz
e_N	Input noise voltage	B= 10Hz to 10KHz	R_g= 1KΩ		3			3			3		μV
			R_g= 500KΩ		25			25			25		
V_O	Output voltage swing	R_L= 2KΩ		± 10	± 13		± 9	± 13		± 10	± 13		V
		R_L= 10KΩ		± 12	± 14		± 11	± 14		± 12	± 14		
SR	Slew Rate				0.8			0.8			0.8		V/μs
CMR	Common mode reiction			70	90		60	90		70	90		dB
SVR	Supply voltage rejection			76	90			90		76	90		dB
V_{ICR}	Common mode input voltage range			± 12	±13		± 11	± 13		± 12	± 13		V

T_{HIGH} = 125°C for MC1558U, 85°C for MC1458I, 70°C for MC1458/C

T_{LOW} = 55°C for MC1558U, -25°C for MC1458I, 0°C for MC1458/C

Fig. 1 - Input bias current as a function of ambient temperature

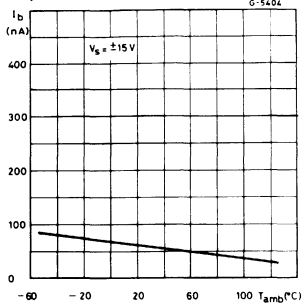


Fig. 2 - Input common mode voltage range as a function of supply voltage

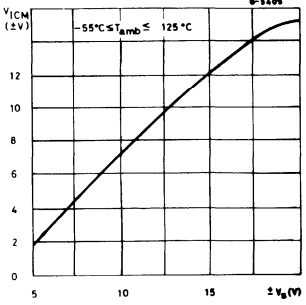


Fig. 3 - Output short-circuit current as a function of ambient temperature

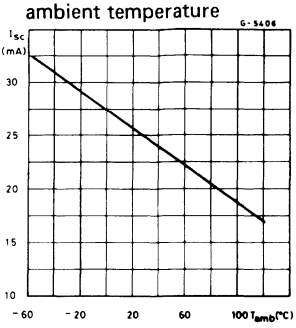


Fig. 4 - Open loop voltage gain as a function of frequency

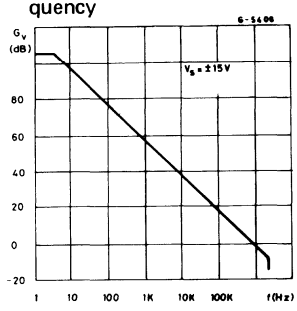


Fig. 5 - Open loop phase response as a function of frequency.

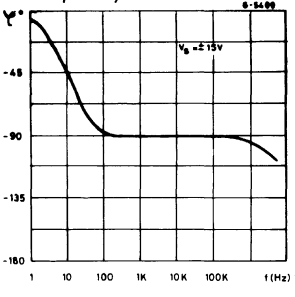


Fig. 6 - Broadband noise for various bandwidths

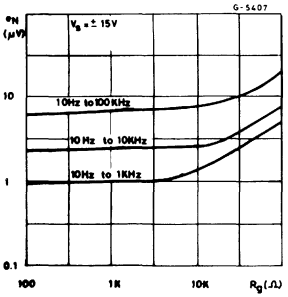


Fig. 7 - Power bandwidth (large signal swing vs. frequency)

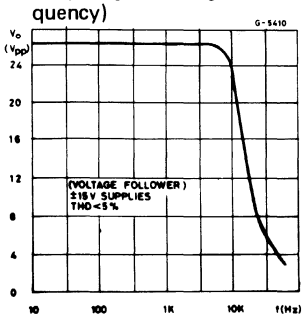


Fig. 8 - Output voltage swing as a function of load resistance

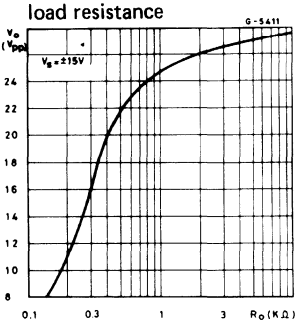
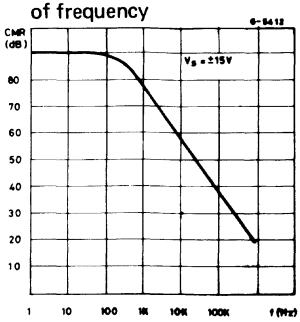


Fig. 9 - Common mode rejection ratio as a function of frequency



APPLICATION INFORMATION

Fig. 10 - Full wave rectifier

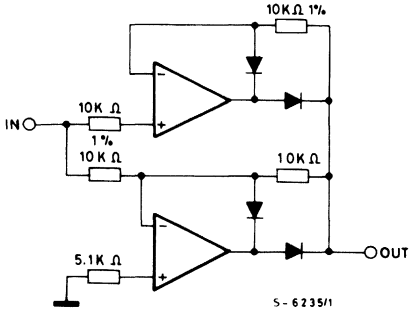


Fig. 11 - Half wave rectifier

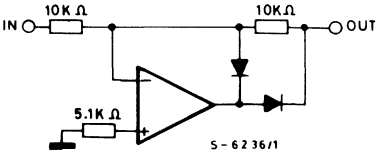
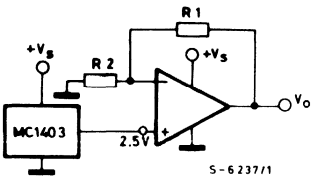
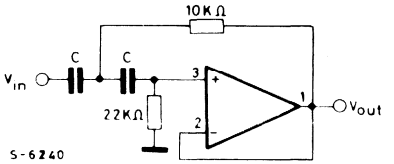


Fig. 12 - Voltage reference



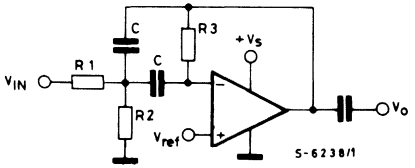
$$V_o = 2.5\ V\ (1 + \frac{R1}{R2})$$

Fig. 14 - High-pass filter



f_c = 100 Hz with C = 0.1 μF

Fig. 13 - Multiple feedback bandpass filter



Given f_o = Center Frequency
$A(f_o)$ = Gain at Center Frequency
Choose Value f_o, C
Then:

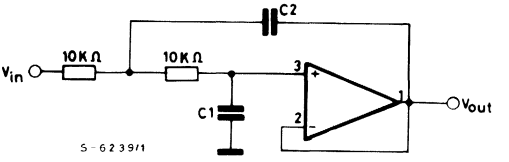
$$R3 = \frac{Q}{\pi f_o C}\ ;\ R1 = \frac{R3}{2\,A(f_o)}\ ;\ R2 = \frac{R1\,R3}{4Q^2\,R1 - R3}$$

For less than 10% error from operational amplifier

$\frac{Q_o\ f_o}{BW} < 0.1$ Where f_o and BW are expressed in Hz.

If source impedance varies, filter may be preceeded with voltage follower buffer to stabilize filter parameters.

Fig. 15 - Low-pass filter



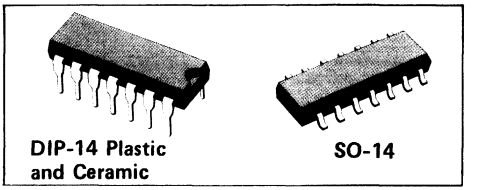
f_c = 3KHz with C1 = 3.9 nF
and C2 = 6.8 nF.

MC1488

RS232C QUAD LINE DRIVER

- CURRENT LIMITED OUTPUT ± 10mA TYP.
- POWER-OFF SOURCE IMPEDANCE 300Ω MIN.
- SIMPLE SLEW RATE CONTROL WITH EXTERNAL CAPACITOR
- FLEXIBLE OPERATING SUPPLY RANGE
- INPUTS ARE TTL AND μP COMPATIBLE

The MC1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS232C.



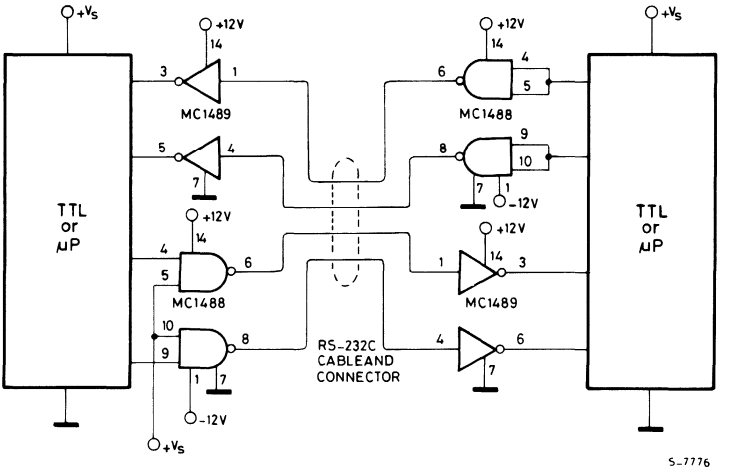
DIP-14 Plastic and Ceramic — SO-14

ORDERING NUMBER: MC1488P (Plastic DIP)
MC1488L (Ceramic DIP)
MC1488D (SO-14)

ABSOLUTE MAXIMUM RATINGS

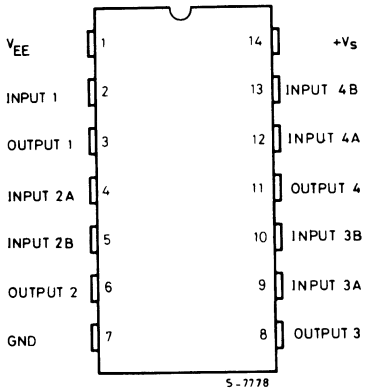
V_S	Power supply voltage	15	V
V_{EE}	Power supply voltage	-15	V
V_{IR}	Input voltage range	$-15 \leqslant V_{IR} \leqslant 7$	V
V_O	Output signal voltage	± 15	V
T_{amb}	Operating ambient temperature	0 to 75	°C
T_{stg}	Storage temperature range	-65 to 150	°C

Typical Application: RS232C data transmission

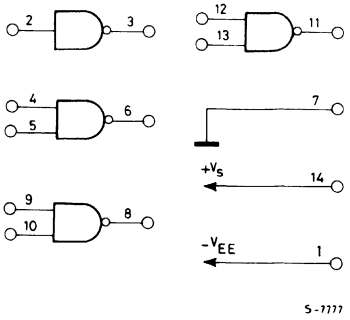


MC1488

CONNECTION DIAGRAM
(top view)



LOGIC DIAGRAM



THERMAL DATA

			Plastic DIP-14	Ceramic DIP-14	SO-14
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	200°C/W	165°C/W	165°C/W

ELECTRICAL CHARACTERISTICS (V_S = 9 ± 10% V, V_{EE} = -9 ± 10% V, T_{amb} = 0 to 75°C unless otherwise specified)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{IL}	Input current	Low logic state (V_{IL} = 0)		1	1.6	mA	1
I_{IH}	Input current	High logic state (V_{IH} = 5V)			10	μA	1
V_{OH}	Output voltage	High logic state R_L = 3KΩ V_{IL} = 0.8V, V_S = 9V, V_{EE} = -9V V_{IL} = 0.8V, V_S = 13.2V, V_{EE} = -13.2V	6 9	7 10.5		V V	2 2
V_{OL}	Output voltage	Low logic state R_L = 3KΩ V_{IH} = 1.9V, V_{EE} = -9V, V_S = 9V V_{IH} = 1.9V, V_{EE} = -13.2V, V_S = 13.2V	-6 -9	-7 -10.5		V V	2 2
I_{OS+} *	Positive output short-circuit current		6	10	12	mA	3
I_{OS-} *	Negative output short-circuit current		-6	-10	-12	mA	3
R_o	Output resistance	$V_S = V_{EE} = 0$ $\lvert V_o \rvert = \pm 2V$	300			Ω	4

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit	Fig.
I_S	Positive supply current ($R_l = \infty$)	V_{IH} = 1.9V V_{IL} = 0.8V V_{IH} = 1.9V V_{IL} = 0.8V V_{IH} = 1.9V V_{IL} = 0.8V	V_S = 9V V_S = 9V V_S = 12V V_S = 12V V_S = 15V V_S = 15V		15 4.5 19 5.5	20 6 25 7 34 12	mA	5
I_{EE}	Negative supply current ($R_L = \infty$)	V_{IH} = 1.9V V_{IL} = 0.8V V_{IH} = 1.9V V_{IL} = 0.8V V_{IH} = 1.9V V_{IL} = 0.8V	V_{EE} = -9V V_{EE} = -9V V_{EE} = -12V V_{EE} = -12V V_{EE} = -15V V_{EE} = -15V		-13 -18	-17 -15 -23 -15 -34 -2.5	mA µA mA µA mA mA	5
P_C	Power consumption	V_S = 9V V_S = 12V	V_{EE} = -9V V_{EE} = -12V			333 576	mW	

SWITCHING CHARACTERISTICS ($V_S = \pm 9 \pm 1\%$ V, $V_{EE} = -9 \pm 1\%$ V, $T_{amb} = 25°C$)

t_{PLH}	Propagation delay time	Z_l = 3KΩ and 15pF		275	350	ns	6
t_{THL}	Fall time	Z_l = 3KΩ and 15pF		45	75	ns	6
t_{PHL}	Propagation delay time	Z_l = 3KΩ and 15pF		110	175	ns	6
t_{TLH}	Rise time	Z_l = 3KΩ and 15pF		55	100	ns	6

* Maximum package power dissipation may be exceeded if all outputs are shorted simultaneously

TEST CIRCUITS

Fig. 1 - Input current

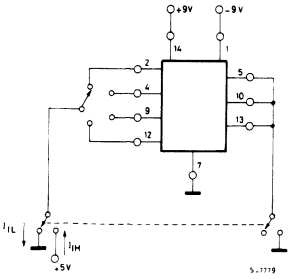


Fig. 2 - Output voltage

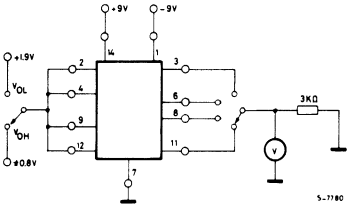
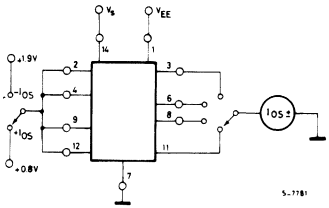


Fig. 3 - Output short-circuit current



TEST CIRCUITS

Fig. 4 - Output resistance (power off)

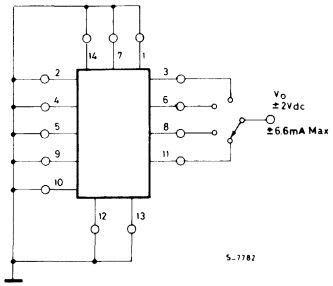


Fig. 5 - Power supply currents

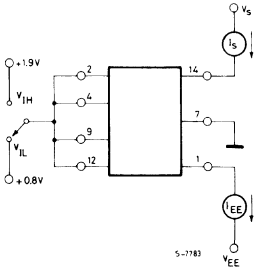


Fig. 6 - Switching response

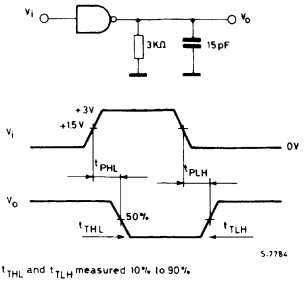


Fig. 7 - Transfer characteristics vs. power supply voltage

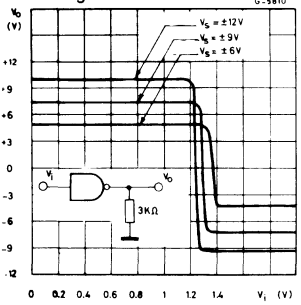


Fig. 8 - Short-circuit output current vs. temperature

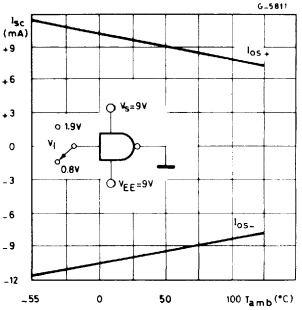


Fig. 9 - Output slew-rate load capacitance

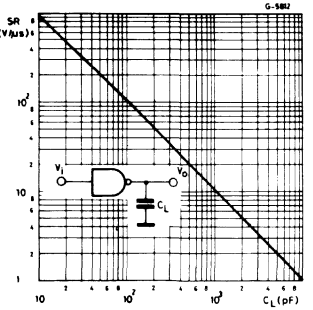


Fig. 10 - Output voltage and current-limiting characteristics

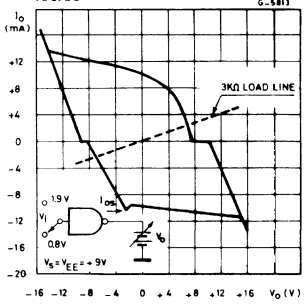
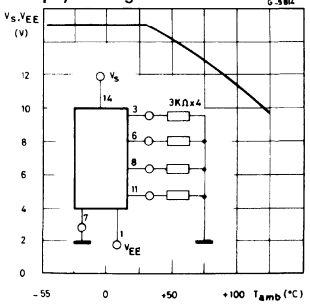


Fig. 11 - Maximum operating temperature vs. power-supply voltage



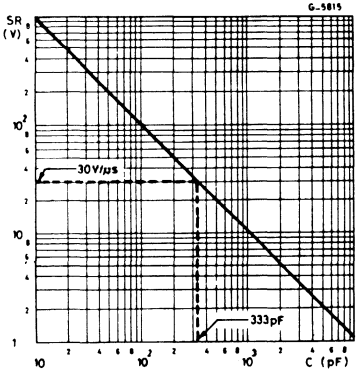
APPLICATIONS INFORMATION

The Electronic Industries Association (EIA) has released the RS232C specification detailing the requirements for the interface between data processing equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS232C defined levels. The RS232C requirements as applied to drivers are discussed herein.

The required driver voltages are defined as between 5 and 15V in magnitude and are positive for a logic "0" and negative for a logic "1". These voltages are so defined when the drivers are terminated with a 3000 to 7000Ω resistor. The MC1488 meets this voltage requirement by converting a DTL/TTL logic level into RS232C levels with one stage of inversion.

The RS232C specification further requires that during transitions, the driver output slew rate must not exceed 30V per μs. The inherent slew rate of the MC1488 is much too fast for this requirement. The current limited output of the device can be used to control this slew rate by connecting a capacitor to each driver output. The required capacitor can be easily determined by using the relationship $C = I_{OS} \times \Delta T/\Delta V$ from which Figure 12 is derived. Accordingly, a 330pF capacitor on each output will guarantee a worst case slew rate of 30V per μs.

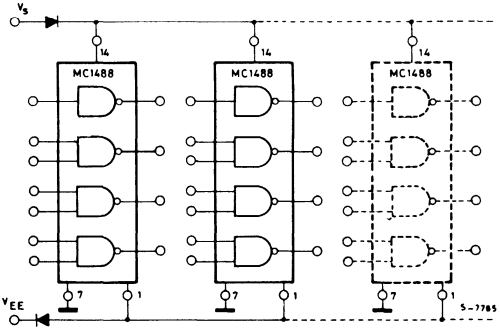
Fig. 12 - Slew rate vs. capacitance for I_{SC} = 10mA



The interface driver is also required to withstand an accidental short to any other conductor in an interconnecting cable. The worst possible signal on any conductor would be another driver using a plus or minus 15V, 500mA source. The MC1488 is designed to indefinitely withstand such a short to all four outputs in a package as long as the power-supply voltages are greater than 9.0V (i.e., $V_S \geq 9.0V$; $V_{EE} \leq -9.0V$). In some power-supply designs, a loss of system power causes a low impedance on the power-supply outputs. When this occurs, a low impedance to ground would exist at the power inputs to the MC1488 effectively shorting the 300Ω output resistor to ground. If **all four outputs** were then shorted to plus or minus 15V, the power dissipation in these resistors would be excessive. Therefore, if the system is designed to permit low impedances to ground at the power-supplies of the drivers, a diode should be placed in each power-supply lead to prevent over-heating in this fault condition. These two diodes, as shown in Figure 13, could be used to decouple all the driver packages in a system. (These same diodes will allow the MC1488 to withstand momentary shorts to the ± 15V limits specified in the earlier Standard RS232B). The addition of the diodes also permits the MC1488 to withstand faults with power-supplies of less than the 9.0V stated above.

The maximum short-circuit current allowable under fault conditions is more than guaranteed by the previously mentioned 10mA output current limiting.

Fig. 13 - Power supply protection to meet power-off fault conditions



Other Applications

The MC1488 is an extremely versatile line driver with a miriad of possible applications. Several features of the drivers enhance this versatility:

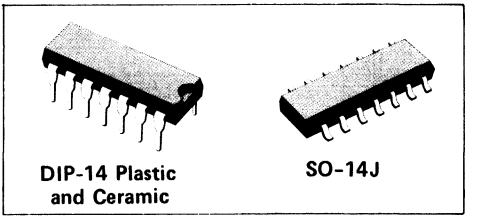
1. Output Current Limiting – this enables the circuit designer to define the output voltage levels independent of power-supplies and can be accomplished by diode clamping of the output pins.
2. Power-Supply Range – as can be seen from the schematic drawing of the drivers, the positive and negative driving elements of the device are essentially independent and do not require matching power-supplies. In fact, the positive supply can very from a minimum seven volts (required for driving the negative pulldown section) to the maximum specified 15V. The negative supply can vary from approximately -2.5V to the minimum specified -15V. The MC1488 will drive the output to within 2V of the positive or negative supplies as long as the current output limits are not exceeded. The combination of the current-limiting and supply-voltage features allow a wide combination of possible outputs within the same quad package.

MC1489
MC1489A

QUAD LINE RECEIVERS

- INPUT RESISTANCE – 3.0K to 7.0KΩ
- INPUT SIGNAL RANGE – ± 30V
- INPUT THRESHOLD HYSTERESIS BUILT-IN
- RESPONSE CONTROL:
  a) LOGIC THRESHOLD SHIFTING
  b) INPUT NOISE FILTERING

The MC1489 monolithic quad line receivers are designed to interface data therminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.



DIP-14 Plastic and Ceramic

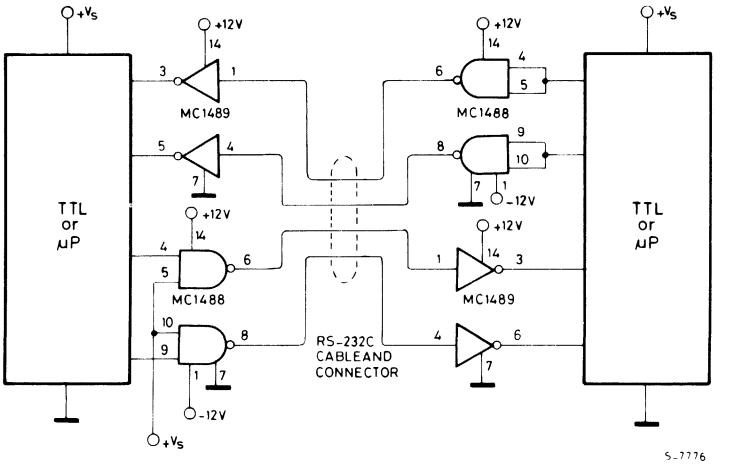
SO-14J

ABSOLUTE MAXIMUM RATINGS

V_S	Power supply voltage	10	V
V_i	Input voltage range	± 30	V
I_{OL}	Output load current	20	mA
P_{tot}	Power dissipation	1	W
T_{amb}	Operating ambient temperature	0 to 75	°C
T_{stg}	Storage temperature range	-65 to 150	°C

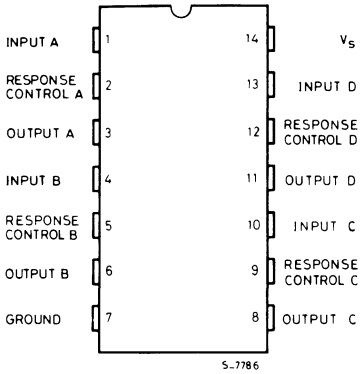
ORDERING NUMBER: MC1489L, MC1489AL (DIP-14 Ceramic)
MC1489P, MC1489AP (DIP-14 Plastic)
MC1489D, MC1489AD (SO-14)

Typical Application: RS232C data transmission

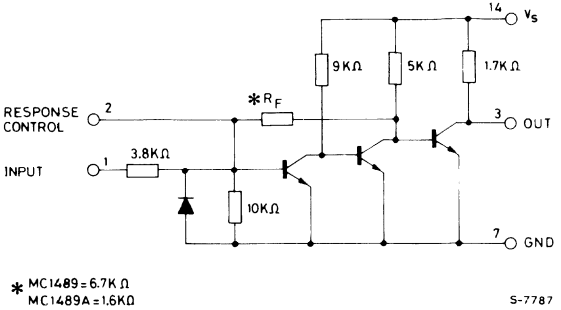


MC1489
MC1489A

CONNECTION DIAGRAM
(Top view)



SCHEMATIC DIAGRAM (1/4 of circuit shown)



ELECTRICAL CHARACTERISTICS (Response control pin is open; V_S = 5V, T_{amb} = 0 to 75°C unless otherwise specified)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{IH}	Positive input current	V_{IH} = 25V V_{IH} = 3V	3.6 0.43		8.3	mA
I_{IL}	Negative input current	V_{IL} = -25V V_{IL} = -3V	-3.6 -0.43		-8.3	mA
V_{IH}	Input Turn-on threshold voltage	T_{amb} = 25°C $V_{OL} \leqslant$ 0.45V for **MC1489** for **MC1489A**	1 1.75	1.95	1.5 2.25	V
V_{IL}	Input Turn-off threshold voltage	T_{amb} = 25°C $V_{OH} \geqslant$ 2.5V I_L = -0.5mA	0.75		1.25	V
V_{OH}	Output voltage high	V_{IH} = 0.75V I_L = -0.5mA	2.5	4	5	V
		I_L = -0.5mA input open circuit	2.5	4	5	V
V_{OL}	Output voltage low	V_{IL} = 3V I_L = 10mA		0.2	0.45	V
I_{OS}	Output short circuit current			-3	-4	mA
I_S	Power supply current	All gates "on" I_O = 0mA V_{IH} = 5V		16	26	mA
P_C	Power consumption	V_{IH} = 5V		80	130	mW

SWITCHING CHARACTERISTICS (V_S = 5V, T_{amb} = 25°C, see Fig. 1)

t_{PLH}	Propagation Delay time	R_L = 3.9KΩ		25	85	ns
t_{TLH}	Rise time	R_L = 3.9KΩ		120	175	ns
t_{PHL}	Propagation Delay time	R_L = 390Ω		25	50	ns
t_{THL}	Fall time	R_L = 390Ω		10	20	ns

TEST CIRCUITS

Fig. 1 - Switching response

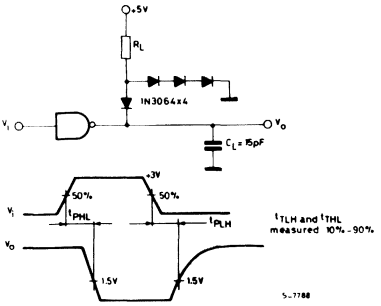
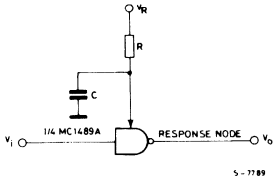


Fig. 2 - Response control node



C, capacitor is for noise filtering
R, resistor is for threshold shifting

Fig. 3 - Input current

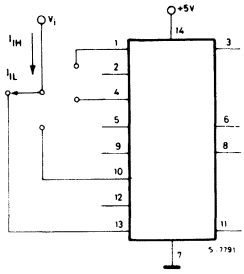


Fig. 4 - Output short-circuit current

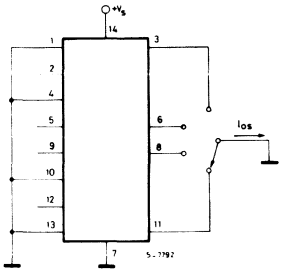


Fig. 5 - Output voltage and input threshold voltage

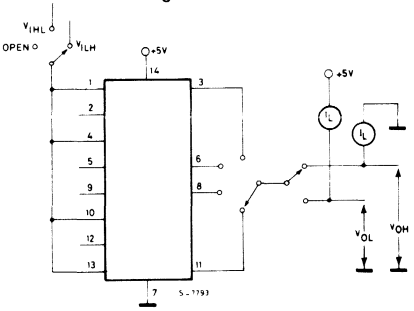
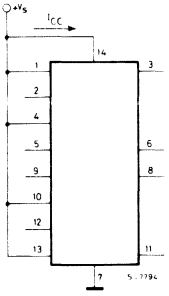


Fig. 6 - Power supply current



TYPICAL CHARACTERISTICS (V_S = 5V, T_{amb} = 25°C unless otherwise specified)

Fig. 7 - Input current

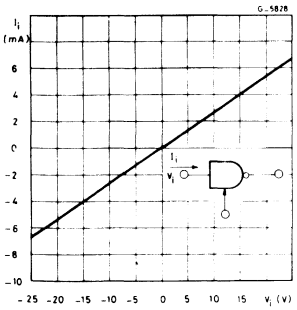


Fig. 8 - MC1489 input threshold voltage adjustament

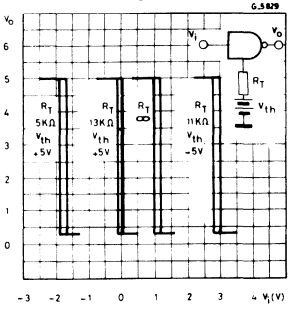


Fig. 9 - MC1489A input threshold voltage adjustment

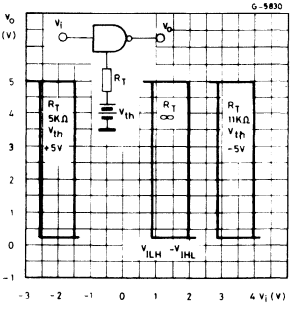


Fig. 10 - Input threshold voltage vs. temperature

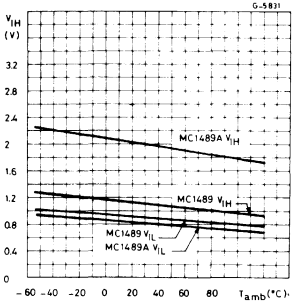
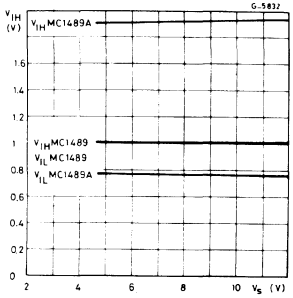


Fig. 11 - Input threshold vs. power-supply voltage



APPLICATION INFORMATION

General Information

The Electronic Industries Association (EIA) has released the RS-232C specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS-232C defined levels. The RS-232C requirements as applied to receivers are discussed herein.

The required input impedance is defined as between 3000Ω and 7000Ω for input voltages between 3.0 and 25V in magnitude; and any voltage on the receiver input in an open circuit condition must be less than 2.0V in magnitude. The MC1489 circuits meet these requirements with a maximum open circuit voltage of one V_{BE}.

The receiver shall detect a voltage between -3.0 and -25V as a Logic "1" and inputs between + 3.0 and + 2.5V as a Logic "0". On some interchange leads, an open circuit of power "OFF" condition (300Ω or more to ground) shall be decoded as an "OFF" condition or Logic "1". For this reason, the input hysteresis thresholds of the MC1489 circuits are all above ground. Thus an open or grounded input will cause the same output as a negative or Logic "1" input.

Device Characteristics

The MC1489 interface receivers have internal feedback from the second stage to the input stage providing input hysteresis for noise rejection. The MC1489 input has typical turn-on voltage of 1.25V and turn-off of 1.0V for a typical hysteresis of 250mV. The MC1489A has typical turn-on of 1.95V and turn-off of 0.8V for typically 1.15V of hysteresis.

Each receiver section has an external response control node in addition to the input and output pins, thereby allowing the designer to vary the input threshold voltage levels. A resistor can be connected between this node and an external power supply. Figure 2, 4 and 5 illustrate the input threshold voltage shift possible through this technique.

This response node can also be used for the filtering of high-frequency, high-energy noise pulses. Figures 8 and 9 show typical noise-pulse rejection for external capacitors of various sizes.

These two operations on the response node can be combined or used individually for may combinations of interfacing applications. The MC1489 circuits are particularly useful for interfacing between MOS circuits and MDTL/MTTL logic systems. In this application, the input threshold voltages are adjusted. (with the appropiate supply and resistor values) to fall in the center of the MOS voltage logic levels. (See Figure 10).

APPLICATION INFORMATION (continued)

The response node may also be used as the receiver input as long as the designer realizes that he may not drive this node with a low impedance source to a voltage greater than one diode above gorund or less than one diode below ground. This feature is demonstrated in Figure 11 where two receivers are slaved to the same line that must still meet the RS-232C impedance requirement.

Fig. 12 - Typical Turn-on threshold vs. capacitance from response control pin to GND

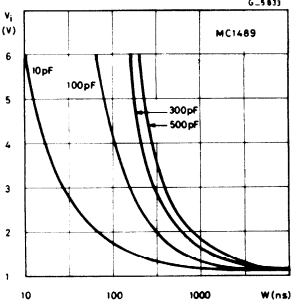


Fig. 13 - Typical Turn-on threshold vs. capacitance from response control pin to GND

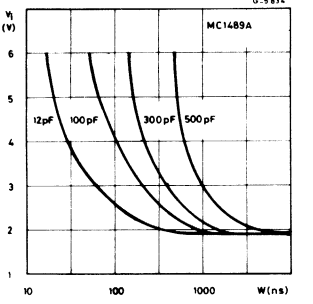
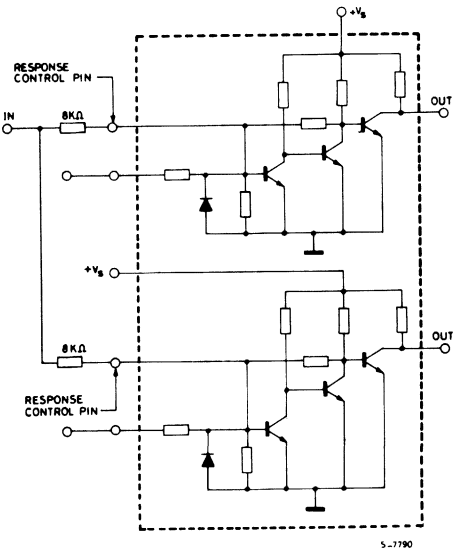


Fig. 14 - Typical paralleling of two MC1489/A receivers to meet RS-232C



MC1776

PROGRAMMABLE OPERATIONAL AMPLIFIERS

- MICROPOWER CONSUMPTION
- INTERNALLY FREQUENCY COMPENSATION
- OFFSET NULL CAPABILITY
- SHORT CIRCUIT PROTECTION
- LOW INPUT BIAS CURRENTS
- LOW NOISE

The MC1776 is a programmable operational amplifier available in four different packages (plastic and ceramic Minidip, TO-99 and SO-8 micropackage). High input impedance, low supply currents and low input noise over a wide range of operating supply voltages coupled with programmable electrical characteristics, make it an extremely versatile amplifier for use in high accuracy, low power consumption analog applications.

Input noise voltage and current, power consumption and input current can be optimized by a single resistor of current source that sets the quiescent current for nanowatt power consumption or for characteristics similar to the LM741. Internal frequency compensation absence of "latch-up" high slew rate and short circuit current protection assure ease of use in long interval integrators, active filters and sample and hold circuits.

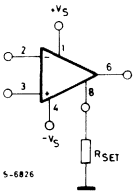
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 18	V
$V_{I(1)}$	Input voltage	± 15	V
ΔV_I	Differential input voltage	± 30	V
V_{SET}	Maximum voltage to ground at I_{SET}	V_s -2V to V_s	V
I_{SET}	Minimum current at I_{SET}	500	μA
T_{op}	Operating temperature for **MC1776**	-55 to 125	°C
	for **MC1776I**	-25 to 85	°C
	for **MC1776C**	0 to 70	°C
	Output short circuit duration (2)	indefinite	
T_{stg}	Storage temperature	-65 to 150	°C
T_j	Junction temperature	150	°C

1) For supply voltage less than ± 1.5V, input voltage is equal to the supply voltage
2) The short circuit duration is limited by thermal dissipation

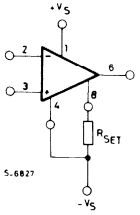
PROGRAMMING

R_{set} to GROUND



Typical R_{SET} values		
V_s	I_{SET} = 1.5μA	I_{SET} = 15μA
± 6V	3.6 MΩ	360 kΩ
± 10V	6.2 MΩ	620 kΩ
± 12V	7.5 MΩ	750 kΩ
± 15V	10 MΩ	1 MΩ

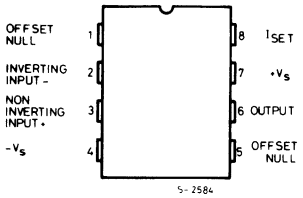
R_{set} to NEGATIVE SUPPLY (Recommended for supply voltage less than ± 6V)



Typical R_{SET} values		
V_s	I_{SET} = 1.5μA	I_{SET} = 15μA
± 1.5V	1.6 MΩ	160 kΩ
± 3V	3.6 MΩ	360 kΩ
± 6V	7.5 MΩ	750 kΩ
± 15V	20 MΩ	2 MΩ

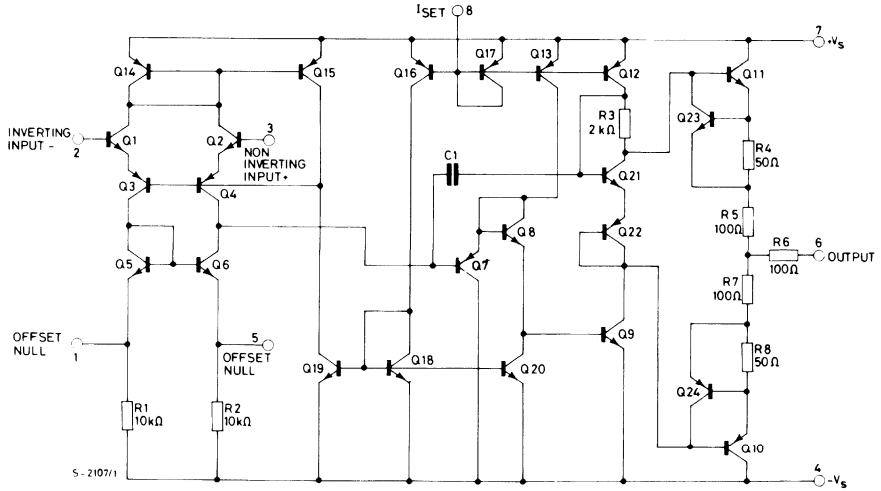
MC1776

CONNECTION DIAGRAM AND ORDERING NUMBERS
(top views)



Temperature range	Ceramic Minidip	Plastic Minidip	SO-8 Micropackage	TO-99
Commercial 0 to 70°C	MC1776CU	MC1776CP1	MC1776CD	MC1776CG
Industrial -25 to 85°C	–	–	MC1776ID	–
Military -55 to 125°C	MC1776U	–	–	MC1776G

SCHEMATIC DIAGRAM



THERMAL DATA

		Plastic Minidip	Ceramic Minidip	TO-99	SO-8
$R_{th\ j\text{-}amb}$ Thermal resistance junction-ambient	max	120°C/W	150°C/W	155°C/W	200°C/W

ELECTRICAL CHARACTERISTICS for MC1776/I

(V_s= ± 15V, T_{amb}= 25°C unless otherwise specified)

Parameter		Test conditions	I_{SET}= 1.5 μA			I_{SET}= 15 μA			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OS}	Input offset voltage	$R_g \leq 10\ k\Omega$		2	5		2	5	mV
I_{OS}	Input offset current	$R_g \leq 10\ k\Omega$		0.7	3		2	15	nA
I_b	Input bias current			2	7.5		15	50	nA
R_i	Input resistance			50			5		MΩ
C_i	Input capacitance			2			2		pF
ΔV_{OS}	Input offset voltage adjustment range			9			18		mV
G_v	Large signal voltage gain	$R_L \geq 75\ k\Omega$ V_o= ± 10 V	106	112					dB
		$R_L \geq 5\ k\Omega$ V_o= ± 10 V				100	112		dB
R_o	Output resistance			5			1		kΩ
I_{sc}	Output short-circuit current			3			12		mA
I_s	Supply current			20	25		160	180	μA
P_S	Power consumption				0.75			5.4	mW
	Transient response (unity gain)	V_i = 20 m V $R_L \geq 5\ k\Omega$ C_L= 100 pF							
	Rise time t_r			1.6			0.35		μs.
	Overshoot Δ V_o			0			10		%
SR	Slew rate	$R_L \geq 5\ k\Omega$		0.1			0.8		V/μs
V_o	Output voltage swing	$R_L \geq 75\ k\Omega$	± 12	± 14					V
		$R_L \geq 5\ k\Omega$				± 10	± 13		V
The following specifications apply for T_{amb} = -55 to 125°C (MC1776), -25 to + 85°C (MC1776I)									
V_{OS}	Input offset voltage	$R_g \leq 10\ k\Omega$			6			6	mV
I_{OS}	Input offset current	T_{amb} = Max			5			15	nA
		T_{amb} = Min			10			40	nA
I_b	Input bias current	T_{amb} = Max			7.5			50	nA
		T_{amb} = Min			20			120	nA
V_i	Input voltage range		± 10			± 10			V
CMR	Common mode rejection	$R_g \leq 10\ k\Omega$	70	90		70	90		dB
SVR	Supply voltage rejection	$R_g \leq 10\ k\Omega$	76	92		76	92		dB
G_v	Large signal voltage gain	$R_L \geq 75\ k\Omega$ V_o= ± 10V	100			98			dB
V_o	Output voltage swing	$R_L \geq 75\ k\Omega$	± 10			± 10			V
I_s	Supply current				30			200	μA
P_S	Power consumption				0.9			6	mW

ELECTRICAL CHARACTERISTICS for MC1776/I

(V_s= ± 3V, T_{amb}= 25°C unless otherwise specified)

Parameter		Test conditions	I_{SET}= 1.5 μA			I_{SET}= 15 μA			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OS}	Input offset voltage	$R_g \leq$ 10 kΩ		2	5		2	5	mV
I_{OS}	Input offset current			0.7	3		2	15	nA
I_b	Input bias current			2	7.5		15	50	nA
R_i	Input resistance			50			5		MΩ
C_i	Input capacitance			2			2		pF
ΔV_{OS}	Input offset voltage adjustment range			9			18		mV
G_v	Large signal voltage gain	$R_L \geq$ 75 kΩ V_o= ± 1V	94	106					dB
		$R_L \geq$ 5 kΩ V_o= ± 1V				94	106		dB
R_o	Output resistance			5			1		kΩ
I_{sc}	Output short-circuit current			3			5		mA
I_s	Supply current			13	20		130	160	μA
P_S	Power consumption			78	120		780	960	μW
	Transient response (unity gain)	V_i = 20 m V $R_L \geq$ 5 kΩ $C_L \leq$ 100 pF							
	Rise time t_r			3			0.6		μs
	Overshoot ΔV_o			0			5		%
SR	Slew rate	$R_L \geq$ 5 kΩ		0.03			0.35		V/μs
The following specifications apply for T_{amb} = -55 to 125°C (MC1776), -25 to + 85°C (MC1776I)									
V_{OS}	Input offset voltage	$R_g \leq$ 10 kΩ			6			6	mV
I_{OS}	Input offset current	T_{amb} = Max			5			15	nA
		T_{amb} = Min			10			40	nA
I_b	Input bias current	T_{amb} = Max			7.5			50	nA
		T_{amb} = Min			20			120	nA
V_i	Input voltage range		± 1			± 1			V
CMR	Common mode rejection	$R_g \leq$ 10 kΩ	70	86		70	86		dB
SVR	Supply voltage rejection	$R_g \leq$ 10 kΩ	76	92		76	92		dB
G_v	Large signal voltage gain	$R_L \geq$ 75 kΩ V_o= ± 1V	88						dB
		$R_L \geq$ 5 kΩ V_o= ± 1V				88			dB
V_o	Output voltage swing	$R_L \geq$ 75 kΩ	± 2	± 2.4					V
		$R_L \geq$ 5 kΩ				± 1.9	± 2.1		V
I_s	Supply current				25			180	μA
P_S	Power consumption				150			1080	μW

ELECTRICAL CHARACTERISTICS for MC1776C

(V_s= ± 15V, T_{amb}= 25°C unless otherwise specified)

Parameter		Test conditions	I_{SET}= 1.5 μA			I_{SET}= 15 μA			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OS}	Input offset voltage	$R_g \leq$ 10 kΩ		2	6		2	6	mV
I_{OS}	Input offset current			0.7	6		2	25	nA
I_b	Input bias current			2	10		15	50	nA
R_i	Input resistance			50			5		MΩ
C_i	Input capacitance			2			2		pF
ΔV_{OS}	Input offset voltage adjustment range			9			18		mV
G_v	Large signal voltage gain	$R_L \geq$ 75 kΩ V_o= ± 10V	94	112					dB
		$R_L \geq$ 5 kΩ V_o= ± 10V				94	112		dB
R_o	Output resistance			5			1		kΩ
I_{sc}	Output short-circuit current			3			12		mA
I_s	Supply current			20	30		160	190	μA
P_S	Power consumption				0.9			5.7	mW
	Transient response (unity gain)	V_i = 20 mV $R_L \geq$ 5 kΩ $C_L \leq$ 100 pF							
	Rise time t_r			1.6			0.35		μs
	Overshoot ΔV_o			0			10		%
SR	Slew rate	$R_L \geq$ 5 kΩ		0.1			0.8		V/μs
V_o	Output voltage swing	$R_L \geq$ 75 kΩ	± 12	± 14					V
		$R_L \geq$ 5 kΩ				± 10	± 13		V
The following specifications apply for T_{amb}= 0 to 70°C									
V_{OS}	Input offset voltage	$R_g \leq$ 10 kΩ			7.5			7.5	mV
I_{OS}	Input offset current	T_{amb}= 70°C			6			25	nA
		T_{amb}= 0°C			10			40	nA
I_b	Input bias current	T_{amb}= 70°C			10			50	nA
		T_{amb}= 0°C			20			100	nA
V_i	Input voltage range		± 10			± 10			V
CMR	Common mode rejection	$R_g \leq$ 10 kΩ	70	90		70	90		dB
SVR	Supply voltage rejection	$R_g \leq$ 10 kΩ	74	92		74	92		dB
G_v	Large signal voltage gain	$R_L \geq$ 75 kΩ V_o= ± 10V	94			94			dB
V_o	Output voltage swing	$R_L \geq$ 75 kΩ	± 10			± 10			V
I_s	Supply current				35			200	μA
P_S	Power consumption				1.05			6	mW

ELECTRICAL CHARACTERISTICS for MC1776C

(V_s= ± 3V, T_{amb}= 25°C unless otherwise specified)

Parameter		Test conditions	I_{SET}= 1.5 μA			I_{SET}= 15 μA			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OS}	Input offset voltage	$R_g \leq$ 10 kΩ		2	6		2	6	mV
I_{OS}	Input offset current			0.7	6		2	25	nA
I_b	Input bias current			2	10		15	50	nA
R_i	Input resistance			50			5		MΩ
C_i	Input capacitance			2			2		pF
ΔV_{OS}	Input offset voltage adjustment range			9			18		mV
G_v	Large signal voltage gain	$R_L \geq$ 75 kΩ V_o= ± 1V	88	106					dB
		$R_L \geq$ 5 kΩ V_o= ± 1V				88	106		dB
R_o	Output resistance			5			1		kΩ
I_{sc}	Output short-circuit current			3			5		mA
I_s	Supply current			13	20		130	170	μA
P_S	Power consumption			78	120		780	1020	μW
	Transient response (unity gain)	V_i = 20 m V $R_L \geq$ 5 kΩ $C_L \leq$ 100 pF							
	Rise time t_r			3			0.6		μs
	Overshoot ΔV_o			0			5		%
SR	Slew rate	$R_L \geq$ 5 kΩ		0.03			0.35		V/μs
The following specifications apply for T_{amb}= 0 to 70°C									
V_{OS}	Input offset voltage	$R_g \leq$ 10 kΩ			7.5			7.5	mV
I_{OS}	Input offset current	T_{amb}= 70°C			6			25	nA
		T_{amb}= 0°C			10			40	nA
I_b	Input bias current	T_{amb}= 70°C			10			50	nA
		T_{amb}= 0°C			20			100	nA
V_i	Input voltage range		± 1			± 1			V
CMR	Common mode rejection	$R_g \leq$ 10 kΩ	70	86		70	86		dB
SVR	Supply voltage rejection	$R_g \leq$ 10 kΩ	74	92		74	92		dB
G_v	Large signal voltage gain	$R_L \geq$ 75 kΩ V_o= ± 1V	88						dB
		$R_L \geq$ 5 kΩ V_o= ± 1V				88			dB
V_o	Output voltage swing	$R_L \geq$ 75 kΩ	± 2	± 2.4					V
		$R_L \geq$ 5 kΩ				± 2	± 2.1		V
I_s	Supply current				25			180	μA
P_S	Power consumption				150			1080	μW

Fig. 1 - Input bias current vs. set current

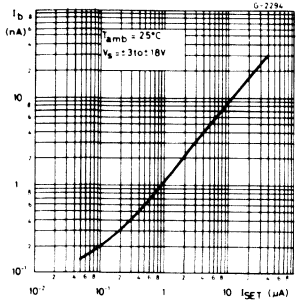


Fig. 2 - Input bias current vs. ambient temperature

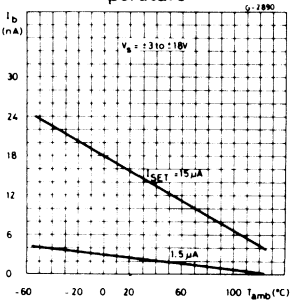


Fig. 3 - Input offset current vs. ambient temperature

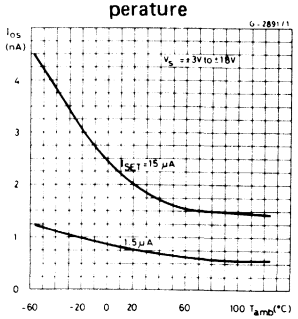


Fig. 4 - Change in input offset voltage vs. set current

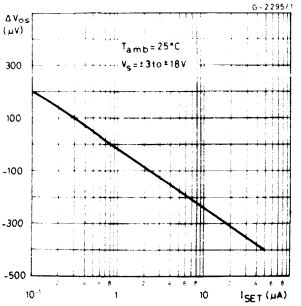


Fig. 5 - Change in input offset voltage vs. ambient temperature (unnulled)

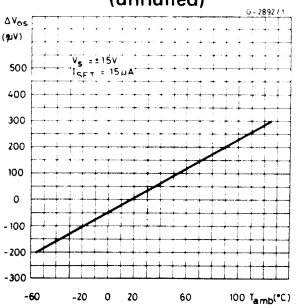


Fig. 6 - Input noise voltage vs. set current

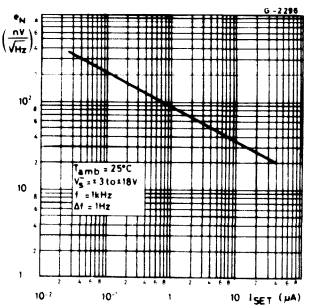


Fig. 7 - Input noise voltage and current vs. frequency

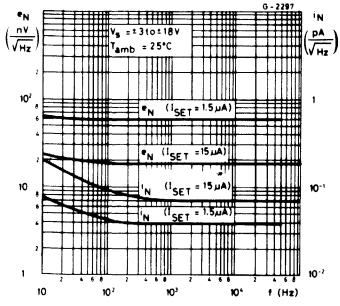


Fig. 8 - Input noise current vs. set current

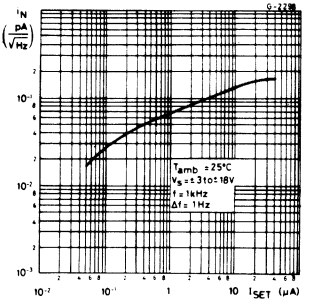


Fig. 9 - Optimum source resistance for minimum noise vs. set current.

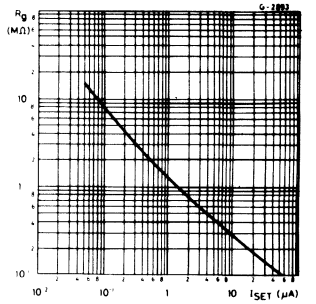


Fig. 10 - Output voltage swing vs. load resistance

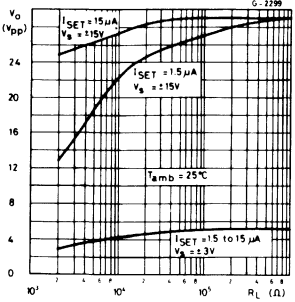


Fig. 11 - Output voltage swing vs. supply voltage

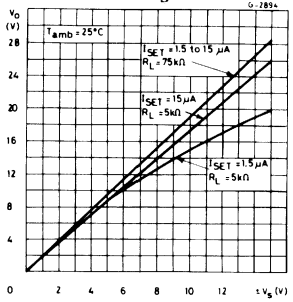


Fig. 12 - Gain bandwidth product vs. set current

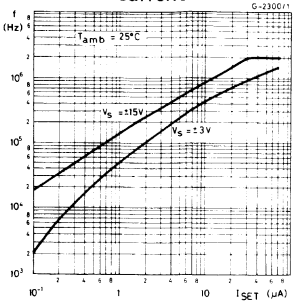


Fig. 13 - Open loop voltage gain vs. ambient temperature

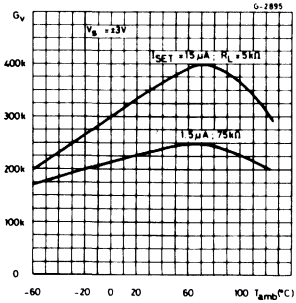


Fig. 14 - Open loop voltage gain vs. ambient temperature

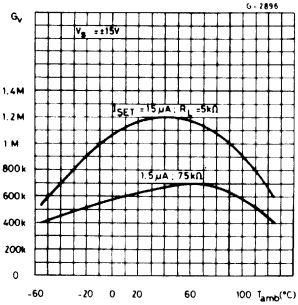


Fig. 15 - Open loop voltage gain vs. set current

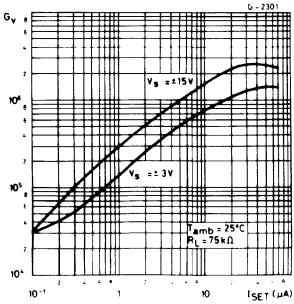


Fig. 16 - Common mode rejection vs. set current

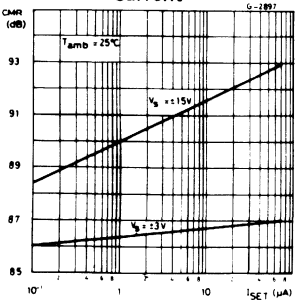


Fig. 17 - Supply voltage rejection vs. set current

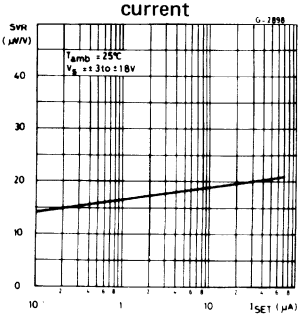


Fig. 18 - Supply current vs. ambient temperature

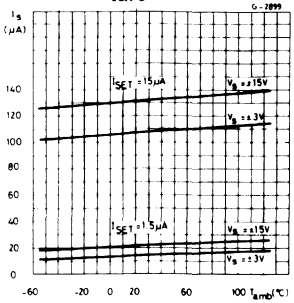


Fig. 19 - Standby supply current vs. set current

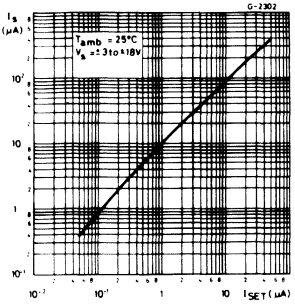


Fig. 20 - Slew rate vs. set current

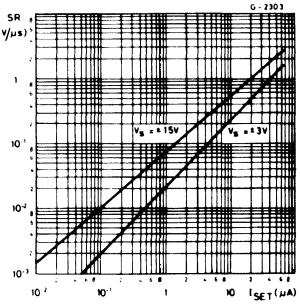
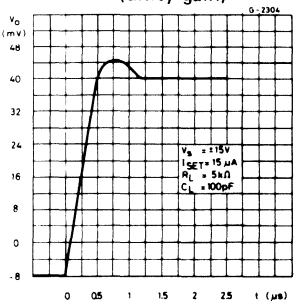


Fig. 21 - Voltage follower transient response (unity gain)



TYPICAL APPLICATIONS

Fig. 22 - High accuracy sample and hold

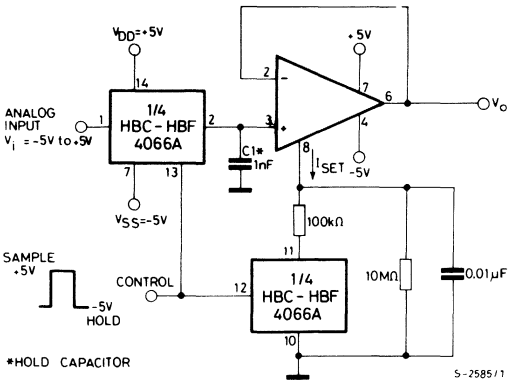


Fig. 23 - Nanowatt amplifier ($V_S = \pm 1.2V$)

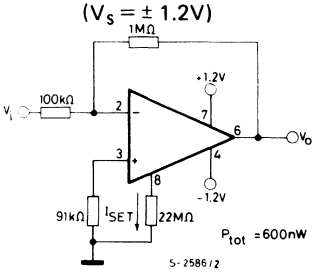
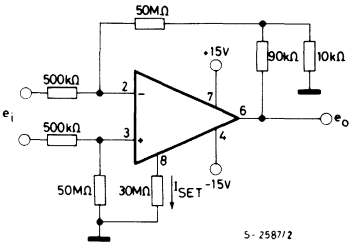


Fig. 24 - High input impedance amplifier



TYPICAL APPLICATIONS (continued)

Fig. 25 - Multiplexing and signal conditioning

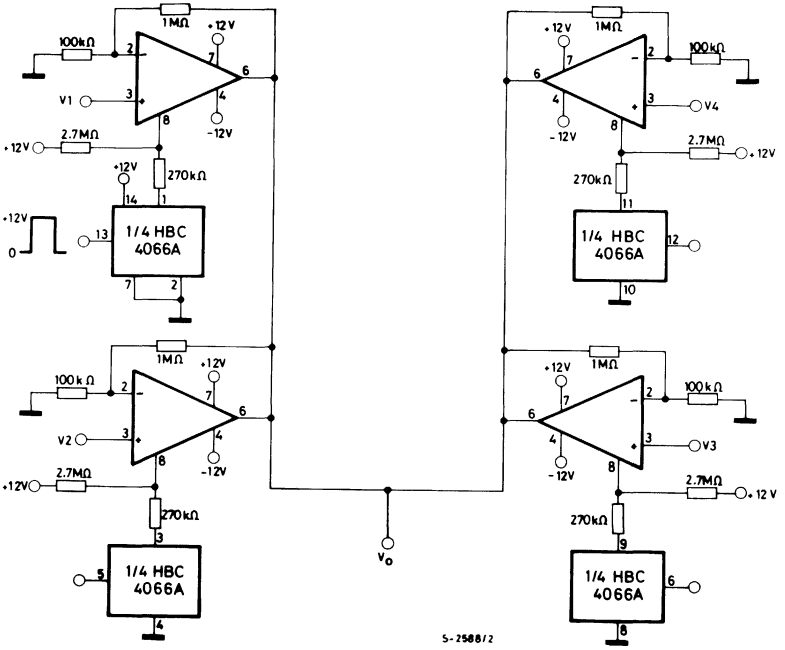


Fig. 26 - Multiple feedback bandpass filter

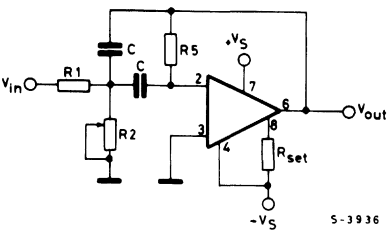
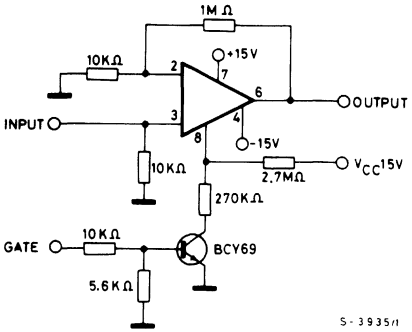


Fig. 27 - Gated amplifier



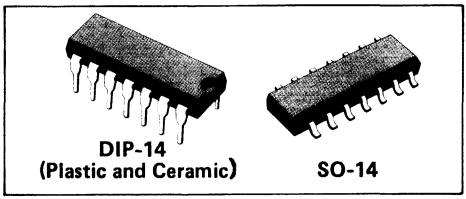
MC3302

QUAD SINGLE-SUPPLY COMPARATOR

- WIDE OPERATING TEMPERATURE RANGE: -40 to + 85°C
- SINGLE-SUPPLY OPERATION: + 2 to + 28V
- DIFFERENTIAL INPUT VOLTAGE = ± V_S
- COMPARE VOLTAGES AT GROUND POTENTIAL
- TTL/CMOS COMPATIBLE
- LOW CURRENT DRAIN (800μA TYP.)
- OUTPUTS CAN BE CONNECTED TO GIVE THE IMPLIED AND FUNCTION

The MC3302 Quad Comparator is designed specifically for single positive supply consumer, automotive and industrial electronic applications.

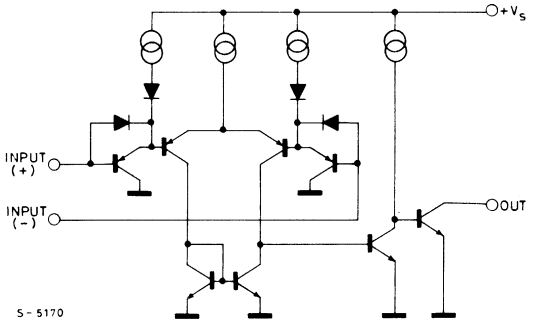
Each device contains four independent comparators, making it ideally suited to applications where high density and low cost are important. The MC3302 is available in a standard 14-lead dual in line plastic or ceramic package and in 14-lead micropackage.



DIP-14 (Plastic and Ceramic) **SO-14**

ORDERING NUMBERS: MC3302P (Plastic DIP)
MC3302L (Ceramic DIP)
MC3302D (SO-14)

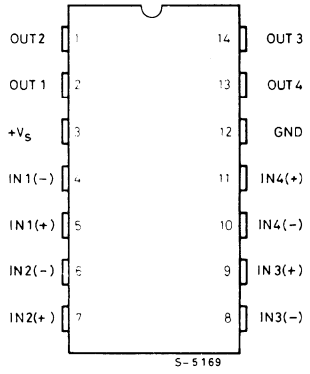
SCHEMATIC DIAGRAM
(each section)



ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	+2 to +28	V
V_l	Input voltage range	-0.3 to V_s	V
V_i	Differential input voltage	$\pm V_s$	
I_i	Input current ($V_i < -0.3$ V)	50	mA
T_{op}	Operating temperature	-40 to + 85	°C
T_j	Junction temperature	150	°C
T_{stg}	Storage and junction temperature	-65 to 150	°C

CONNECTION DIAGRAM
(top view)



THERMAL DATA (*)

			Ceramic DIP-14	SO-14	Plastic DIP-14
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	150°C/W	165°C/W	200°C/W

ELECTRICAL CHARACTERISTICS (V_s = +15V, T_{amb} = 25°C, unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_{os}	Input offset voltage	V_{REF} = 1.2 V			3	20	mV
			T_{amb} = -40 to +85°C			40	
I_b	Input bias current (1)	Output in linear range			30	500	nA
			T_{amb} = -40 to +85°C			1000	
V_{ICR}	Input Common-Mode voltage range (2)	V_s = 28V		0 to 26			V
I_s	Supply current	$R_L = \infty$	V_s = 5V		0.8	1.8	mA
G_v	Voltage gain	R_L = 15 KΩ		66	90		dB
g_m	Transconductance				2		mhos
I_o	Output sink current	(V_s = 5.0 V) (T_{amb} = +25°C, V_{OL} = 400 mV)			6		mA
		(T_{amb} = -40 to +85°C, V_{OL} = 800 mV)		2			
V_{sat}	Output saturation voltage	$V_{IN(-)} \geq 1V$, $V_{IN(+)} = 0V$, I_{sink} = 2 mA	V_s = 5 to 28V		150	400	mV
$I_{o\ leak}$	Output leakage current	$V_{IN(+)} \geq 1V$, $V_{IN(-)} = 0V$				1	μA
V_{IDR}	Differential input Voltage			±Vs			
CMR	Common Mode Rejection				60		dB
$t_{PHL/LH}$	Propagation delay time for positive and negative-going input pulse	R_L = 15KΩ			2		μs
t_{THL} t_{TLH}	Transition Time	R_L = 15KΩ			0.15		μs
					0.8		

Notes: (1) The direction of the current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading change exists on the reference or input lines.

(2) If either input of any comparators goes more negative than 0.3V below ground, a parasitic transistor turns on causing high input current and possible faulty outputs. This conditions is not destructive providing the input current is limited to less than 50 mA.

(3) The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained.

Fig. 1 - Supply current vs. voltage

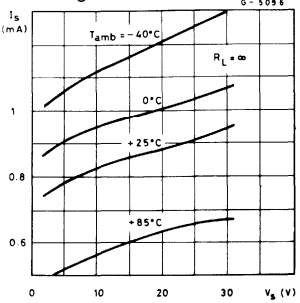


Fig. 2 - Input bias current vs. supply voltage

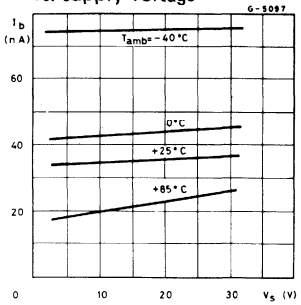


Fig. 3 - Normalized offset voltage vs. temperature

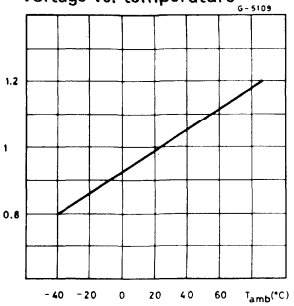


Fig. 4 - Output saturation voltage

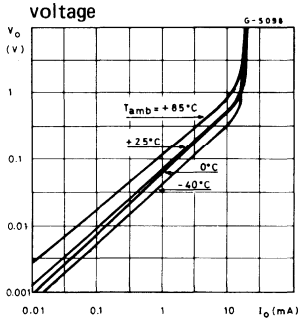


Fig. 5 - Response time

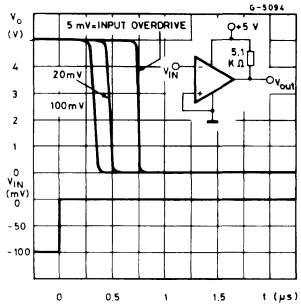
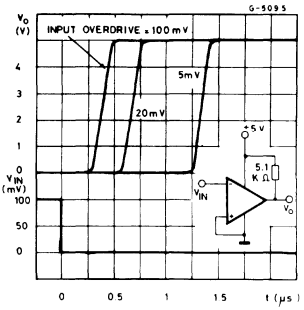


Fig. 6 - Reponse time



APPLICATION INFORMATION

The MC3302 includes four high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output is inadvertently allowed to capacitively couple to the inputs via stray capacitance.

That occurs during the output voltage transitions, when the comparator changes state.

To minimize this problem, PC board layout should be designed to reduce stray input-output coupling; reducing the input resistors to less than 10 KΩ reduces the feedback signal levels and finally, adding even a small amount (1 to 10mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible.

It is good design practice to ground all unused pins.

The differential input voltage may be larger than positive supply without damaging the device. Note that voltages more negative than -0.3V should not be used: an input clamping diode can be used as protection.

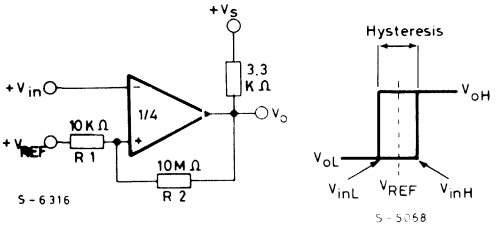
The output of the MC3302 is the uncommitted collector of NPN transistor with grounded emitter. This allows the device to be used like any open-collector gate providing the OR-wide facility.

The output sink current capability is approximately 16mA; if this limit is exceeded, the output transistor will come out of saturation and the output voltage will rise very rapidly.

Under this limit, the output saturarion voltage is limited by the approximately 60Ω r_{sat} of the output transistor.

APPLICATION INFORMATION (continued)

Fig. 7 - Comparator with Hysteresis



$$V_{in\,L} = \frac{R1}{R1 + R2}\,(V_{OL} - V_{REF}) + V_{REF}$$

$$V_{in\,H} = \frac{R1}{R1 + R2}\,(V_{OH} - V_{REF}) + V_{REF}$$

$$\text{Hysteresis} = \frac{R1}{R1 + R2}\,(V_{OH} - V_{OL})$$

Fig. 8 - Squarewave oscillator

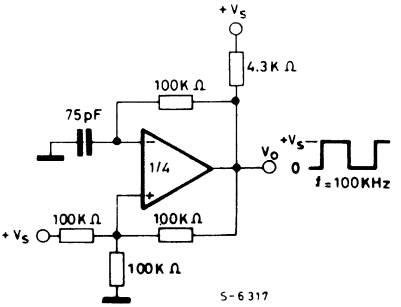


Fig. 9 - Time delay generator

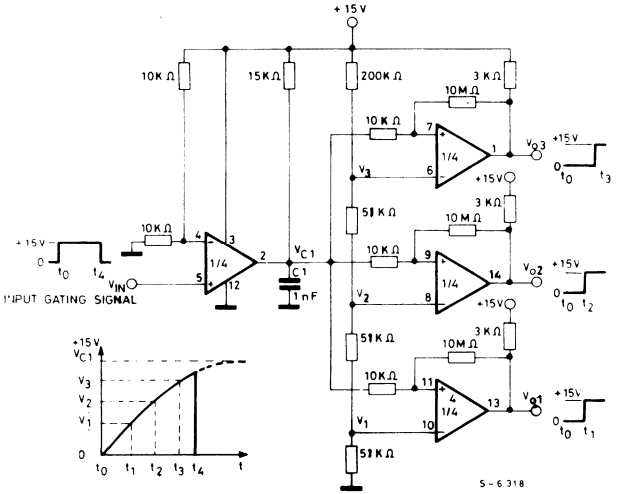
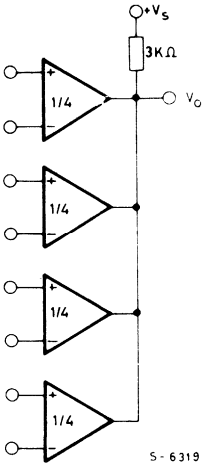


Fig. 10 - ORing the outputs



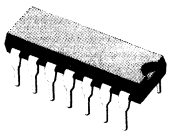
MC3303
MC3403
MC3503

QUAD OPERATIONAL AMPLIFIERS

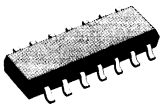
- TRUE DIFFERENTIAL INPUT STAGE
- CLASS AB OUTPUT STAGE FOR MINIMAL CROSSOVER DISTORTION
- SINGLE SUPPLY OPERATION: 3.0 to 36V
- SPLIT SUPPLY OPERATION: ± 1.5 to ± 18V
- LOW INPUT BIAS CURRENTS: 500nA max
- INTERNALLY COMPENSATED
- SHORT CIRCUIT PROTECTED OUTPUTS

The MC3403 is a quad operational amplifier with true differential inputs. The device has electrical characteristics similar to the popular LM741/μA741. However, the MC3403 has several distinct advantages over standard operational amplifier types in single supply applications.

The MC3403 can operate at supply voltages as low as 3.0V or has high as 36V. The common mode input range includes the negative supply, thereby eliminating the necessity for external blasing components in many applications. The output voltage range also includes the negative power supply voltage.

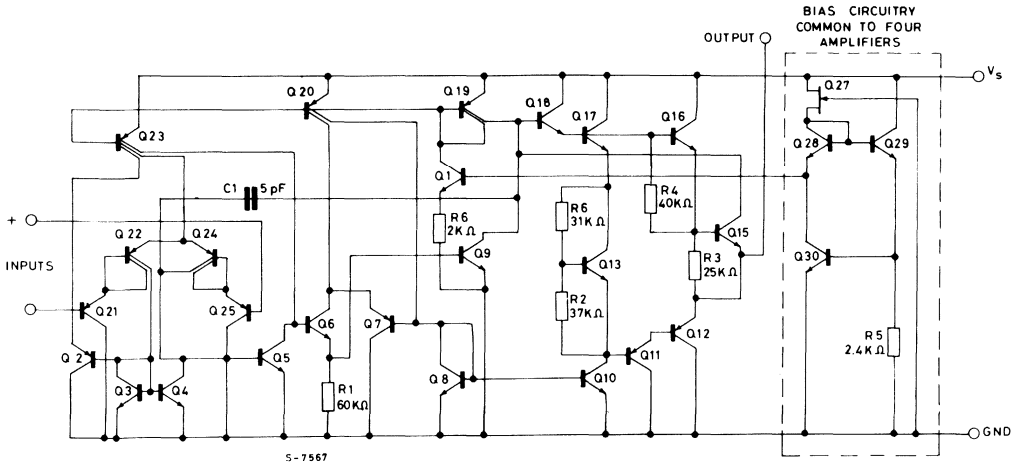


DIP-14
(Plastic and Ceramic)



SO-14

SCHEMATIC DIAGRAM (one section only)



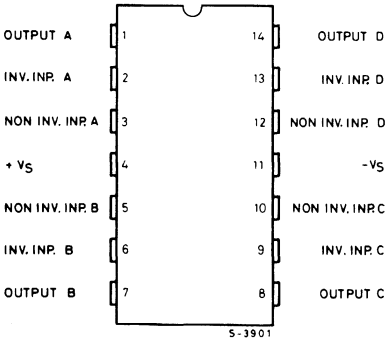
ABSOLUTE MAXIMUM RATINGS

V_S	Single supply voltage	36 V
V_S	Split supplies voltage	± 18 V
V_{IDR}	Input differential voltage range ([1])	± 36 V
V_{ICR}	Input common mode voltage range ([1,2])	± 18 V
T_{op}	Operating ambient temperature for MC3503	-55 to 125 °C
	MC3403	0 to 70 °C
	MC3303	-40 to 85 °C
T_j	Junction temperature	150 °C
T_{stg}	Storage temperature	-65 to 150 °C

Notes: 1 – Split power supplies
2 – For supply voltages less than ± 15V, the absolute maximum input voltage is equal to the supply voltage.

CONNECTION DIAGRAM AND ORDERING NUMBERS

(top view)



Temperature range	Plastic DIP-14	Ceramic DIP-14	Micropackage SO-14
0 to 70°C	MC3403P	MC3403L	MC3403D
-40 to 85°C	MC3303P	MC3303L	MC3303D
-55 to 125°C	–	MC3503L	–

THERMAL DATA

			Ceramic DIP-14	SO-14	Plastic DIP-14
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	150°C/W	165°C/W	200°C/W

ELECTRICAL CHARACTERISTICS (V_S = ± 15V for MC3503, MC3403; V_S = single + 14V for MC3303 T_{amb} = 25°C unless otherwise noted)

Parameter		Test conditions	MC3503			MC3403			MC3303			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IO}	Input offset voltage	T_{amb}= T_{HIGH} to T_{LOW}(1)	– –	2 –	5 6	– –	2 –	10 12	– –	2 –	8 10	mV
I_{IO}	Input offset current	T_{amb}= T_{HIGH} to T_{LOW}	– –	30 –	50 200	– –	30 –	50 200	– –	30 –	75 250	nA
A_{VOL}	Large signal openloop voltage gain	V_O = ± 10V R_L = 2.0KΩ T_{amb}= T_{HIGH} to T_{LOW}	50 25	200 300	– –	20 15	200 –	– –	20 15	200 –	– –	V/mV
I_b	Input bias current	T_{amb} = T_{HIGH} to T_{LOW}	– –	200 300	- 500 - 1200	– –	-200 –	- 500 - 800	– –	-200 –	- 500 - 1000	nA
Z_o	Output impedance	f = 20Hz	–	75	–	–	75	–	–	75	–	Ω
Z_I	Input impedance	f = 20Hz	0.3	1.0	–	0.3	1.0	–	0.3	1.0	–	MΩ
V_{OR}	Output voltage range	R_L = 10KΩ R_L = 2.0KΩ R_L = 2.0KΩ T_{amb}= T_{HIGH} to T_{LOW}	± 12 ± 10 ± 10	± 13.5 ± 13 –	– – –	± 12 ± 10 ± 10	± 13.5 ± 13 –	– – –	+ 12 + 10 + 10	+ 12.5 + 12 –	– – –	V
V_{ICR}	Input common mode voltage range		+ 13V - V_{EE}	+ 13.5V - V_{EE}	–	+ 13V - V_{EE}	+ 13.5V - V_{EE}	–	+ 12V - V_{EE}	+ 12.5V - V_{EE}		V
CMR	Common mode rejection	R_S ≤ 10KΩ	70	90	–	70	90	–	70	90	–	dB
I_S	Power supply current (V_O = 0)	R_L = ∞	–	2.8	4.0	–	2.8	7.0	–	2.6	7.0	mA
I_{os} ±	Individual output short circuit current (2)		± 10	± 30	± 45	± 10	± 20	± 45	± 10	± 30	± 45	mA
SVR	Positive supply rejection		–	30	150	–	30	150	–	30	150	μV/V
SVR	Negative supply rejection		–	30	150	–	30	150	–	–	–	μV/V
$\Delta I_{IO}/\Delta T$	Average temeprature coefficient of input offset current	T_{amb}= T_{HIGH} to T_{LOW}	–	50	–	–	50	–	–	50	–	pA/°C
$\Delta V_{IO}/\Delta T$	Average temperature coefficient of input offset voltage	T_{amb}= T_{HIGH} to T_{LOW}	–	10	–	–	10	–	–	10	–	μV/°C
BW_P	Power bandwidth	A_v = 1, R_L = 2.0KΩ V_O = 20V (p-p) THD = 5%	–	9	–	–	9	–	–	9	–	KHz
B	Small signal bandwidth	A_v = 1, R_L = 10KΩ V_O = 50mV	–	1	–	–	1	–	–	1	–	MHz
SR	Slew rate	A_v = 1, V_I = -10V to + 10V	–	0.6	–	–	0.6	–	–	0.6	–	V/μS
t_{TLH}	Rise time	A_v = 1, R_L = 10KΩ V_O = 50mV	–	0.35	–	–	0.35	–	–	0.35	–	μs
t_{THL}	Fall time	A_v = 1, R_L = 10KΩ V_O = 50mV	–	0.35	–	–	0.35	–	–	0.35	–	μs
OS	Overshoot	A_v = 1, R_L = 10KΩ V_O = 50mV	–	20	–	–	20	–	–	20	–	%
ϕ m	Phase margin	A_v = 1, R_L = 2.0KΩ C_L = 200pF	–	60	–	–	60	–	–	60	–	°
d	Crossover distortion	V_{IN} = 30mV (p-p) V_{OUT} = 2.0V (p-p) f = 10KHz	–	1	–	–	1	–	–	1	–	%

NOTES

1. T_{HIGH} = 125°C for MC3503, 70°C for MC3403, 85°C for MC3303. T_{LOW} = -55°C for MC3503, 0°C for MC3403, -40°C for MC3303.
2. Not to exceed maximum package power dissipation

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V, V_E = GND, T_{amb} = 25°C unless otherwise noted)

Parameter		Test conditions	MC3503			MC3403			MC3303			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IO}	Input offset voltage		–	2	5	–	2	10	–	–	10	mV
I_{IO}	Input offset current		–	30	50	–	30	50	–	–	75	nA
I_b	Input bias current		–	- 200	- 500	–	- 200	- 500	–	–	- 500	nA
A_{VOL}	Large signal open-loop voltage gain	R_L = 2.0KΩ	10	200	–	10	200	–	10	200	–	V/mV
SVR	Supply voltage rejection		–	–	150	–	–	150	–	–	150	μV/V
V_{OR}	Output voltage range range *	R_L = 10KΩ V_{CC} = 5.0V R_L = 10KΩ 5V ⩽ V_{CC} ⩽ 30V	3.3 V_{CC} - 1.7	3.5 V_{CC} - 1.5	– –	3.3 V_{CC} - 1.7	3.5 V_{CC} - 1.5	– –	3.3 V_{CC} - 1.7	3.5 V_{CC} - 1.5	– –	Vp-p
I_S	Power supply current		–	2.5	4	–	2.5	7	–	2.5	7	mA
C_S	Channel separation	f = 1KHz to 20KHz (input referenced)	–	- 120	–	–	- 120	–	–	- 120	–	dB

* Output will swing to ground

Fig. 1 – Sine wave response

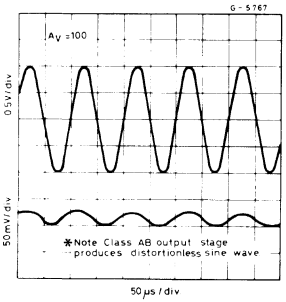


Fig. 2 – Open loop frequency response

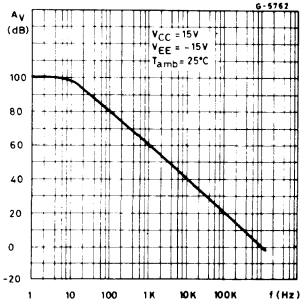


Fig. 3 – Power bandwidth

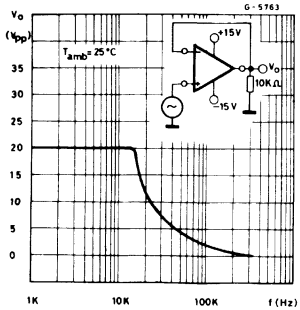


Fig. 4 – Output swing vs. supply voltage

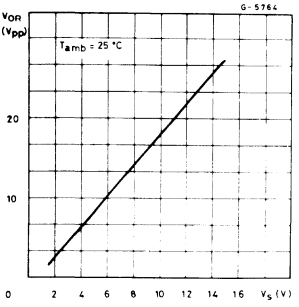


Fig. 5 – Input bias current vs. temperature

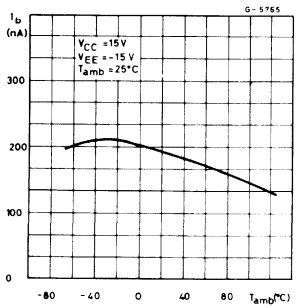
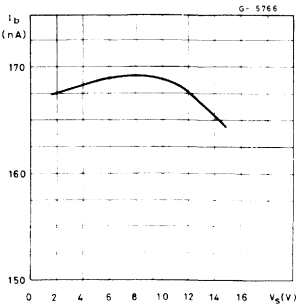
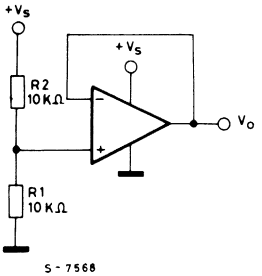


Fig. 6 – Input bias current vs. supply voltage



APPLICATION INFORMATION

Fig. 7 – Voltage reference



$$V_O = \frac{R1}{R1 + R2} \qquad V_O = \frac{1}{2} V_S$$

Fig. 8 – High impedance differential amplifier

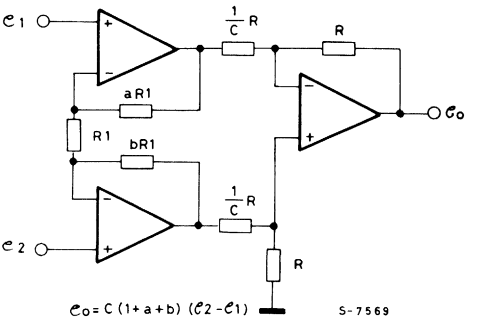
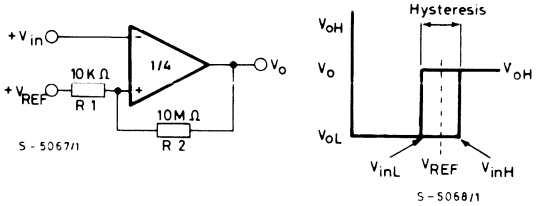


Fig. 9 – Comparator with hysteresis



$$V_{IN\,(L)} = \frac{R1}{R1 + R2} (V_{OL} - V_{REF}) + V_{REF}$$

$$V_{IN\,(H)} = \frac{R1}{R1 + R2} (V_{OH} - V_{REF}) + V_{REF}$$

$$H = \frac{R1}{R1 + R2} (V_{OH} - V_{OL})$$

Fig. 10 – Full wave rectifier

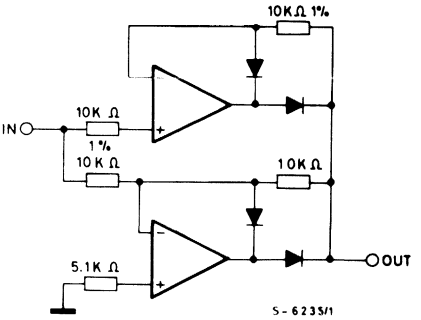
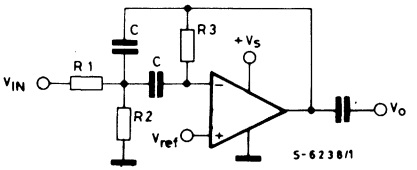


Fig. 11 – Multiple feed back bandpass filter



$$V_{REF} = \frac{1}{2} V_S$$

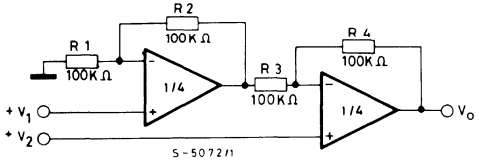
Given f_o = center frequency
$A(f_o)$ = gain at center frequency

then: $R3 = \frac{Q}{\pi f_o C}$, $R1 = \frac{R3}{2A(f_o)}$, $R2 = \frac{R1\,R5}{4Q^2\,R1 - R5}$

For less than 10% error from operational amplifier $\frac{Q_o f_o}{BW} < 0.1$ where f_o and BW are expressed in Hz. If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

APPLICATION INFORMATION (continued)

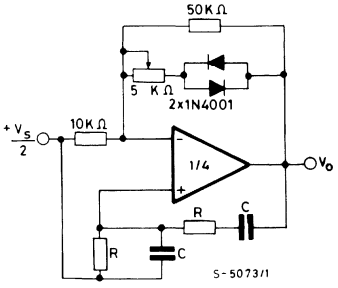
Fig. 12 – High input Z, DC differential amplifier



For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

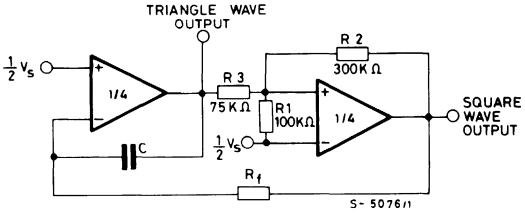
$V_O = 1 + \frac{R4}{R3}$ (V2 – V1)

Fig. 13 – Wien bridge oscillator



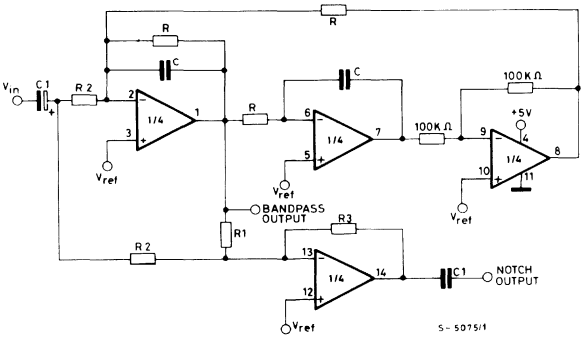
$f_o = \frac{1}{2\pi RC}$

Fig. 14 - Function generator



$f = \frac{R1 + R_C}{4 C R_f R1}$ $\quad R3 = \frac{R1\ R2}{R2 + R1}$

Fig. 15 – Bi-Quad filter



$f_o = \frac{1}{2\pi RC}$; $R1 = QR$; $R2 = \frac{R1}{G_{BP}}$

$V_{ref} = \frac{1}{2} V_s$; $R3 = G_N\ R2$; $C1 = 10C$

Example:

$f_o = 1KHz$	$R = 160K\Omega$
$Q = 10$	$C = 1nF$
$G_{BP} = 1$	$R1 = 1.6M\Omega$
$G_N = 1$	$R2 = 1.6M\Omega$
	$R3 = 1.6M\Omega$

Where: G_{BP} = Center Frequency Gain
G_N = Passband Notch Gain

MC34002

JFET-INPUT DUAL OPERATIONAL AMPLIFIERS

- HIGH SLEW-RATE ... 13V/μs TYP.
- LOW POWER CONSUMPTION
- WIDE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW INPUT BIAS AND OFFSET CURRENTS
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE ... JFET-INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH-UP-FREE OPERATION

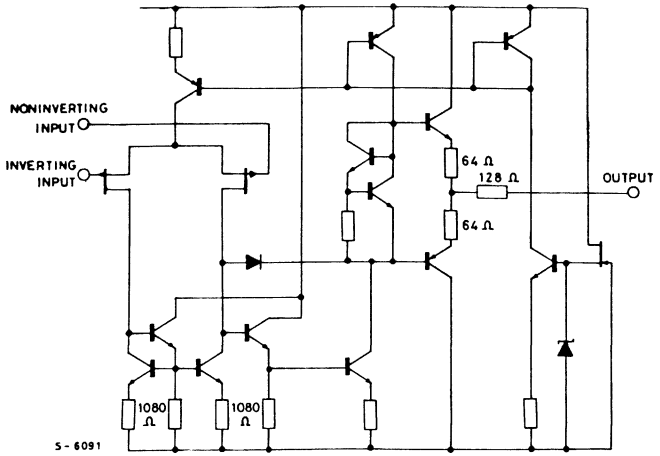
The MC34002 JFET-input operational amplifiers are designed to offer high slew-rate, low input bias and offset current, and low offset voltage temperature coefficient. Each JFET-input operational amplifier incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit.

Minidip
(Plastic and Ceramic)

ABSOLUTE MAXIMUM RATINGS

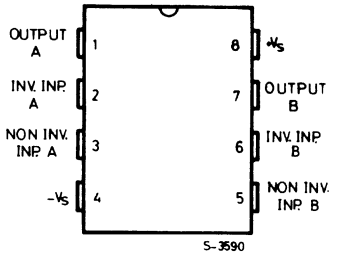
V_s	Supply voltage	+ 18	V
V_{is}	Differential input voltage	± 30	V
V_i	Input voltage	± 16	V
T_{op}	Operating ambient temperature	0 to 70	°C
T_j	Operating junction temperature	115	°C
T_{stg}	Storage temperature	-65 to 150	°C

SCHEMATIC DIAGRAM
(one section)



MC34002

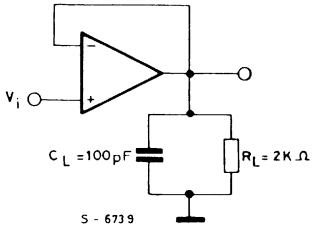
CONNECTION DIAGRAM
(Top view)



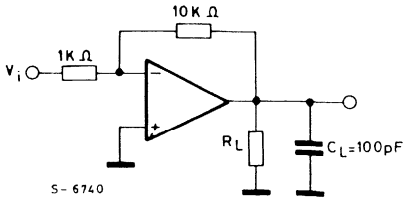
ORDERING NUMBERS

TYPE	PACKAGE	
	Plastic Minidip	Ceramic Minidip
MC34002	MC34002P	MC34002U
MC34002A	MC34002 AP	MC34002 AU
MC34002B	MC34002 BP	MC34002 BU

TEST CIRCUITS



Unity gain amplifier



Gain of 10 inverting amplifier

THERMAL DATA

			Plastic Minidip	Ceramic Minidip
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	120°C/W	150°C/W

ELECTRICAL CHARACTERISTICS ($V_s = \pm 15V$, $T_{amb} = 25°C$, otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_{OS}	Input offset voltage	$R_s < 10K\Omega$	MC34002A		1	2	mV
			MC34002B		3	5	
			MC34002		5	10	
		$R_s < 10K\Omega$ T_{amb} = full range	MC34002A			4	
			MC34002B			7	
			MC34002			13	
$\frac{\Delta V_{OS}}{\Delta T}$	Input offset voltage drift	$R_s < 10K\Omega$ T_{amb} = full range			10		$\mu V/°C$
I_{OS}	Input offset current		MC34002A		25	50	pA
			MC34002B		25	100	
			MC34002		25	100	
		T_{amb} = full range	MC34002A			2	nA
			MC34002B			4	
			MC34002			4	
I_b	Input bias current		MC34002A		50	100	pA
			MC34002B		50	200	
			MC34002		50	200	
		T_{amb} = full range	MC34002A			4	nA
			MC34002B			8	
			MC34002			8	
V_{CM}	Common mode input voltage range			+ 11	+ 15 + 12		V
		T_{amb} = full range		± 11			
V_{OPP}	Large signal voltage swing		$R_L > 10K\Omega$	± 12	± 14		V
			$R_L > 2K\Omega$	± 10	± 13		
		T_{amb} = full range	$R_L > 10K\Omega$	± 12			
			$R_L > 2K\Omega$	± 10			
G_V	Large signal voltage gain	$R_L \geq 2K\Omega$ $V_o = \pm 10V$	MC34002A	50	150		V/mV
			MC34002B	50	150		
			MC34002	25	100		
		$R_L \geq 2K\Omega$	MC34002A	25			
		$V_o = \pm 10V$	MC34002B	25			
		T_{amb} = full range	MC34002	25			
B	Unity gain bandwidth				4		MHz
R_I	Input resistance				10^{12}		Ω
CMR	Common mode rejection	$R_s < 10K\Omega$	MC34002A	80	100		dB
			MC34002B	80	100		
			MC34002	70	100		
		T_{amb} = full range	MC34002A	80			
			MC34002B	80			
			MC34002	70			

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit.
SVR	Suplly voltage rejection	$R_s < 10K\Omega$	MC34002A	80	100		dB
			MC34002B	80	100		
			MC34002	70	100		
		T_{amb} = full range	MC34002A	80			
			MC34002B	80			
			MC34002	70			
I_S	Supply current	$R_L = \infty$	MC34002A		2.8	5	mA
			MC34002B		2.8	5	
			MC34002		2.8	5.4	
		$R_L = \infty$ T_{amb} = full range	MC34002A			5.6	
			MC34002B			5.6	
			MC34002			6.0	
SR	Slew-rate at unity gain	V_I = 10V C_L = 100pF	$R_L = 2K\Omega$		13		V/μs
e_N	Total input noise voltage	f = 1KHz			25		$\frac{nV}{\sqrt{Hz}}$
i_N	Total input noise current				0.01		$\frac{pA}{\sqrt{Hz}}$

Fig. 1 - Maximum peak to peak output voltage vs. frequency

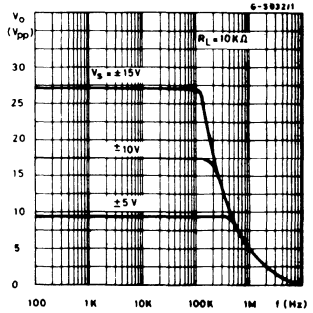


Fig. 2 - Maximum peak to peak output voltage vs. frequency

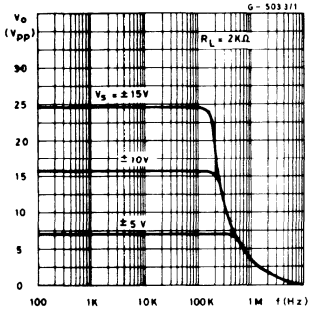


Fig. 3 - Maximum peak to peak output voltage vs. load resistance

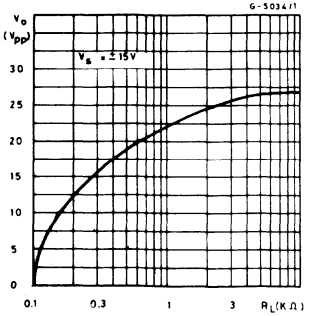


Fig. 4 - Large signal voltage gain and phase shift vs. frequency

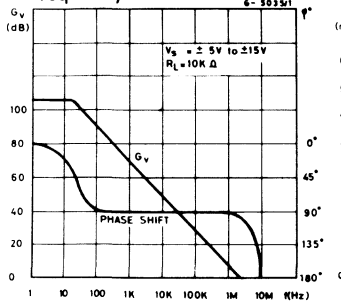


Fig. 5 - Supply current vs. temperature

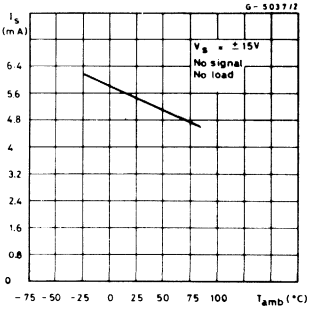


Fig. 6 - Supply current vs. supply voltage

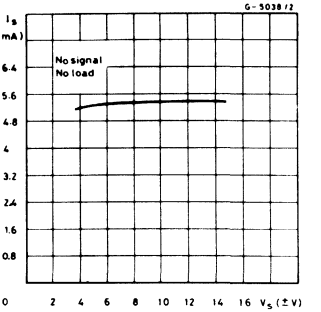


Fig. 7 - Input bias current vs. temperature

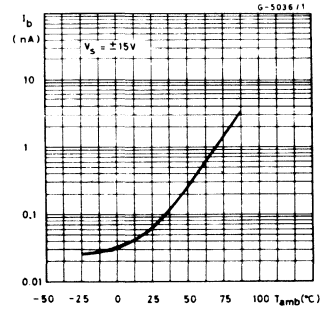


Fig. 8 - Equivalent input noise voltage vs. frequency

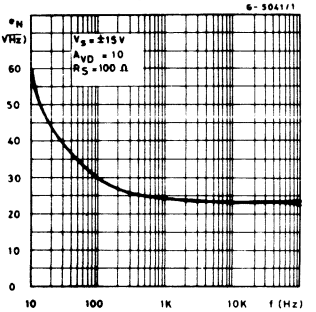
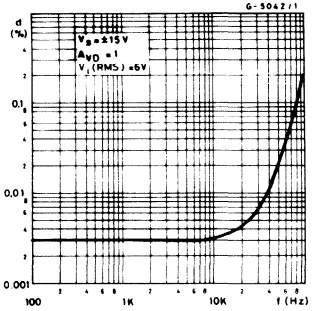
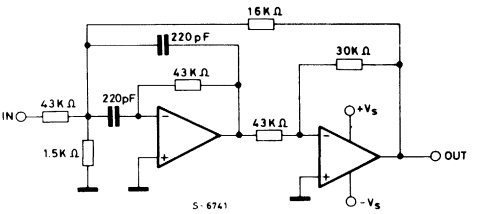


Fig. 9 - Total harmonic distortion vs. frequency



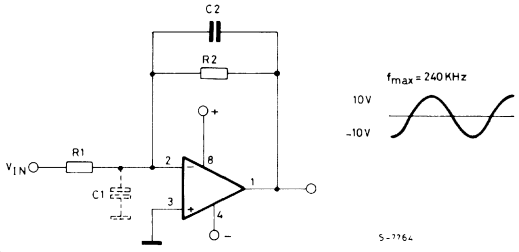
APPLICATION INFORMATION

Fig. 10 - Second order high Q band pass filter (f_o = 100KHz, Q = 30, gain = 4)



APPLICATION INFORMATION (continued)

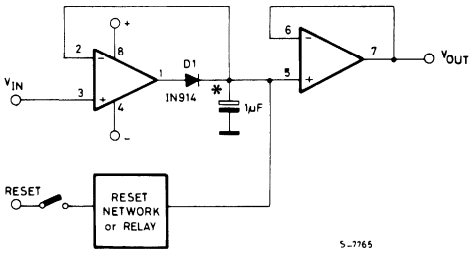
Fig. 11 Wide BW, low noise, low drift amplifier



- Power BW: $f_{max} = \frac{S_r}{2\pi V_p} \cong 240kHz$

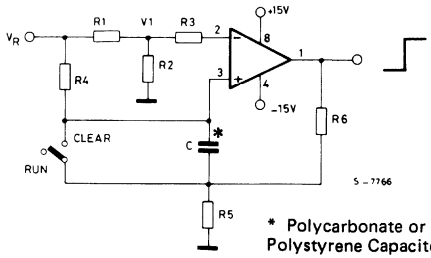
- Parasitic input capacitance (C1 ≅ 3pF plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To comparate add C2 such that: R2C2 ≅ R1C1

Fig. 12 - Positive peak detector



* Polycarbonate capacitor
D1 = Hi-speed, low-reverse leakage diode

Fig. 13 - Long interval RC timer



* Polycarbonate or Polystyrene Capacitor

Time (t) = R4 Cℓn (V_R/V_R-V_I), R3 - R4, R5 - 0.1 R6 if R1 = R2; t = 0.693 R4C

Design Example: 100 Second Timer

V_R = 10V	C = 1.0μF	R3 = R4 = 144M
R6 = 20k	R5 = 2.0k	R1 = R2 = 1.0k

Fig. 14 - 20Hz to 200Hz variable High-pass filter (G_v = 3dB)

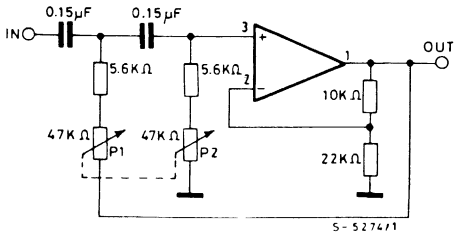
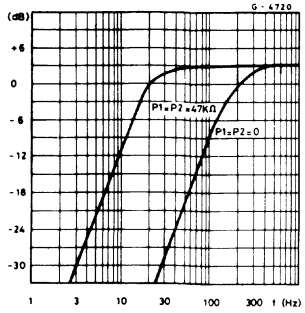


Fig. 15 - Frequency response of the high-pass filter of fig. 17

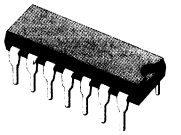


MC34004

JFET-INPUT QUAD OPERATIONAL AMPLIFIERS

- HIGH SLEW-RATE ... 13V/μs TYP.
- LOW POWER CONSUMPTION
- WIDE COMMON-RANGE AND DIFFERENTIAL VOLTAGE RANGES
- LOW INPUT BIAS AND OFFSET CURRENTS
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE ... JFET-INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH-UP-FREE OPERATION

The MC34004 JFET-input operational amplifiers are designed to offer high slew-rate, low input bias and offset current, and low offset voltage temperature coefficient. Each JFET-input operational amplifier incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit.

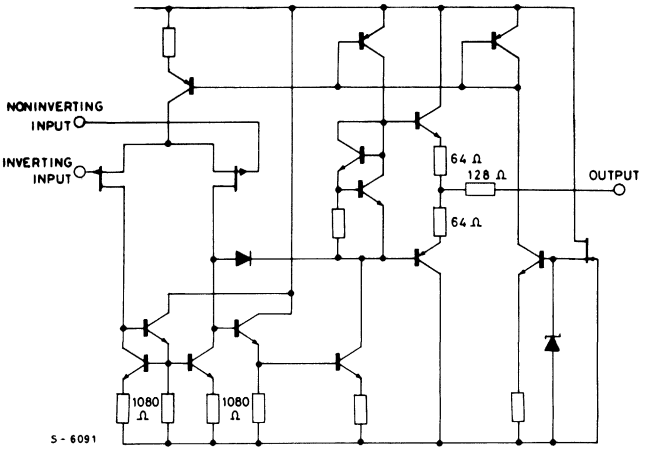


DIP-14
(Plastic and Ceramic)

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 18	V
V_{is}	Differential input voltage	± 30	V
V_i	Input voltage	± 16	V
T_{op}	Operating ambient temperature	0 to 70	°C
T_j	Operating junction temperature	115	°C
T_{stg}	Storage temperature	-65 to 150	°C

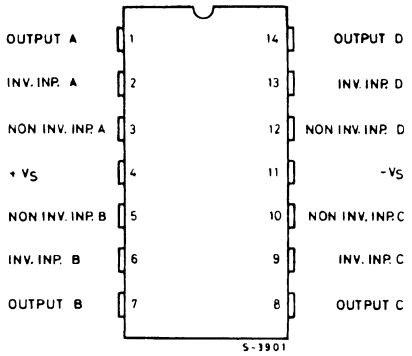
SCHEMATIC DIAGRAM
(one section)



MC34004

CONNECTION DIAGRAM

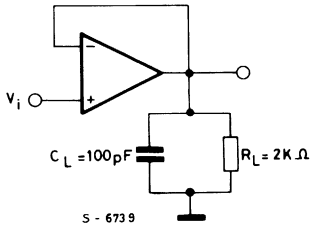
(top view)



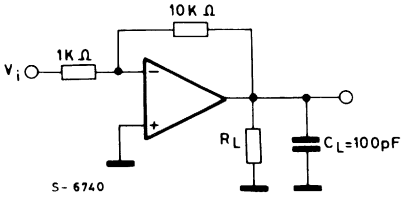
ORDERING NUMBERS

TYPE	PACKAGE	
	Plastic DIP-14	Ceramic DIP-14
MC34004	MC34004P	MC34004L
MC34004A	MC34004 AP	MC34004 AL
MC34004B	MC34004 BP	MC34004 BL

TEST CIRCUITS



Unity gain amplifier



Gain of 10 inverting amplifier

THERMAL DATA

			Ceramic DIP-14	Plastic DIP-14
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	150°C/W	200°C/W

ELECTRICAL CHARACTERISTICS ($V_s = \pm 15V$, $T_{amb} = 25°C$, otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_{OS}	Input offset voltage	$R_s < 10K\Omega$	MC34004A		1	2	mV
			MC34004B		3	5	
			MC34004		5	10	
		$R_s < 10K\Omega$, T_{amb} = full range	MC34004A			4	
			MC34004B			7	
			MC34004			13	
$\frac{\Delta V_{OS}}{\Delta T}$	Input offset voltage drift	$R_s < 10K\Omega$, T_{amb} = full range			10		$\mu V/°C$
I_{OS}	Input offset current		MC34004A		25	50	pA
			MC34004B		25	100	
			MC34004		25	100	
		T_{amb} = full range	MC34004A			2	nA
			MC34004B			4	
			MC34004			4	
I_b	Input bias current		MC34004A		50	100	pA
			MC34004B		50	200	
			MC34004		50	200	
		T_{amb} = full range	MC34004A			4	nA
			MC34004B			8	
			MC34004			8	
V_{CM}	Common mode input voltage range			11	15 12		V
		T_{amb} = full range		± 11			
V_{OPP}	Large signal voltage swing		$R_L > 10K\Omega$	± 12	± 14		V
			$R_L > 2K\Omega$	± 10	± 13		
		T_{amb} = full range	$R_L > 10K\Omega$	± 12			
			$R_L > 2K\Omega$	± 10			
G_V	Large signal voltage gain	$R_L \geq 2K\Omega$, $V_o = \pm 10V$	MC34004A	50	150		V/mV
			MC34004B	50	150		
			MC34004	25	100		
		$R_L \geq 2K\Omega$, $V_o = \pm 10V$, T_{amb} = full range	MC34004A	25			
			MC34004B	25			
			MC34004	25			
B	Unity gain bandwidth				4		MHz
R_I	Input resistance				10^{12}		Ω
CMR	Common mode rejection	$R_s < 10K\Omega$	MC34004A	80	100		dB
			MC34004B	80	100		
			MC34004	70	100		
		T_{amb} = full range	MC34004A	80			
			MC34004B	80			
			MC34004	70			

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
SVR	Supply voltage rejection	$R_s < 10K\Omega$	MC34004A	80	100		dB
			MC34004B	80	100		
			MC34004	70	100		
		T_{amb} = full range	MC34004A	80			
			MC34004B	80			
			MC34004	70			
I_S	Supply current	$R_L = \infty$	MC34004A		5.6	10	mA
			MC34004B		5.6	10	
			MC34004		5.6	10.8	
		$R_L = \infty$ T_{amb} = full range	MC34004A			11.2	
			MC34004B			11.2	
			MC34004			12	
SR	Slew-rate at unity gain	V_i = 10V C_L = 100pF	$R_L = 2K\Omega$		13		V/µs
e_N	Total input noise voltage	f = 1KHz			25		$\frac{nV}{\sqrt{Hz}}$
i_N	Total input noise current				0.01		$\frac{pA}{\sqrt{Hz}}$

Fig. 1 - Maximum peak to peak output voltage vs. frequency

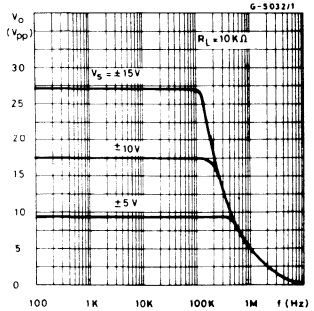


Fig. 2 - Maximum peak to peak output voltage vs. frequency

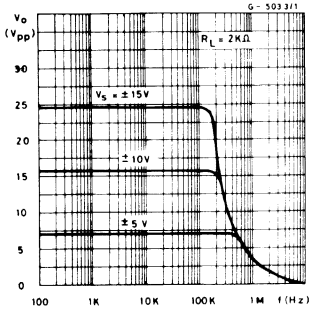


Fig. 3 - Maximum peak to peak output voltage vs. load resistance

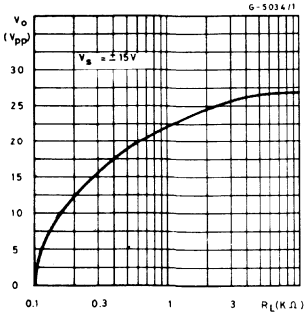


Fig. 4 - Input bias current vs. temperature

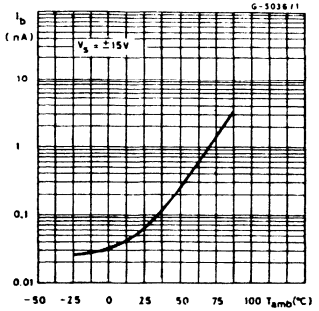


Fig. 5 - Supply current vs. temperature

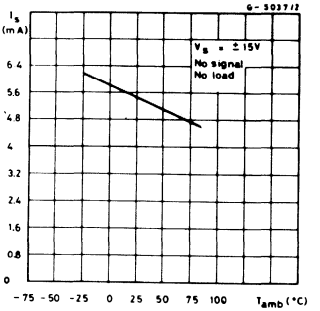


Fig. 6 - Supply current vs. supply voltage

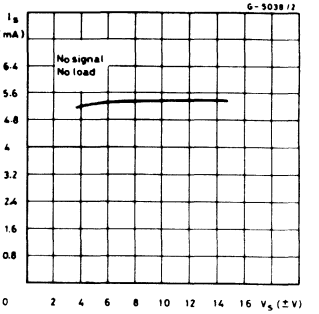


Fig. 7 - Large signal voltage gain and phase shift vs. frequency

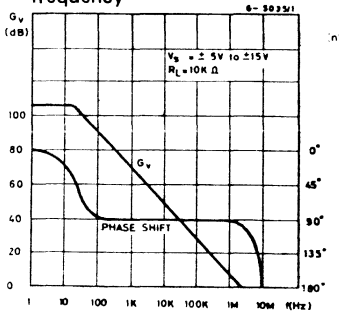


Fig. 8 - Equivalent input noise voltage vs. frequency

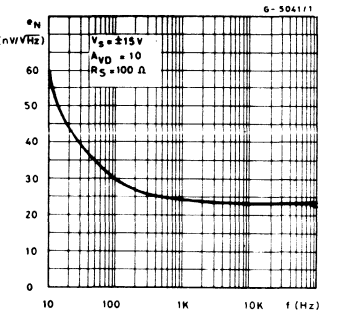
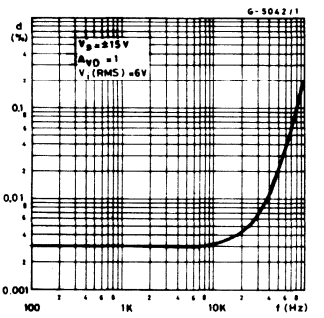


Fig. 9 - Total harmonic distortion vs. frequency



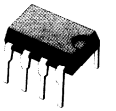
NE532

DUAL OPERATIONAL AMPLIFIERS

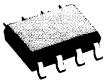
- SINGLE SUPPLY (3V to 30V) OR DUAL SUPPLIES (± 1.5V to 15V)
- VERY LOW SUPPLY CURRENT DRAIN (500μA) ESSENTIALLY INDIPENDENT OF SUPPLY VOLTAGE
- LOW INPUT BIASING CURRENT (TEMPERATURE COMPENSATED)
- LOW INPUT OFFSET VOLTAGE AND OFFSET CURRENT
- DIFFERENTIAL INPUT VOLTAGE RANGE EQUAL TO THE POWER SUPPLY VOLTAGE
- INTERNALLY FREQUENCY COMPENSATED FOR UNITY GAIN
- LARGE OUTPUT VOLTAGE SWING (3.5V WITH $V_s = 5V$)

The NE532 consists of two independent, high gain, internally frequency compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages. Operation from dual power supplies is also possible and the low power supply current drain is independent of the supply voltage.

In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage. The unity gain cross frequency is temperature compensated. The input bias current is also temperature compensated. The NE532 is available in minidip plastic or ceramic package and in a 8-lead micropackage version.

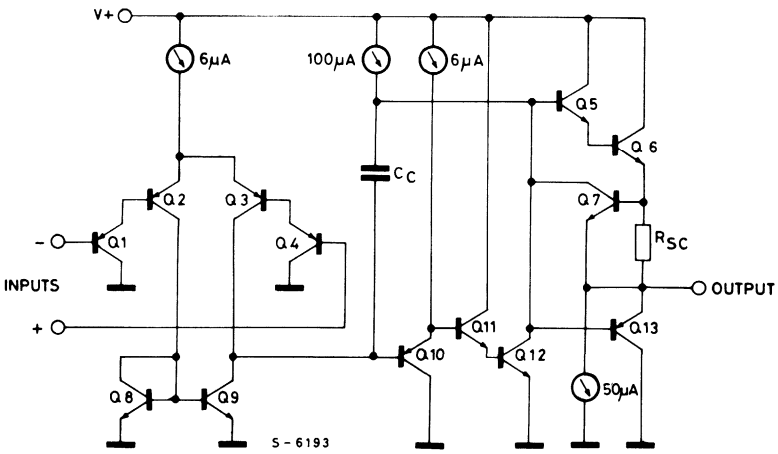


Minidip (Plastic and Ceramic)



SO-8

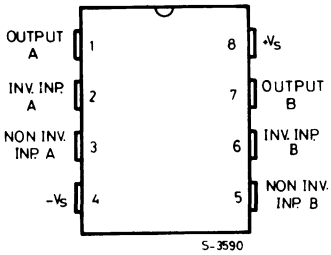
SCHEMATIC DIAGRAM (One section)



ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	32 or ± 16	V
V_i	Differential input voltage	32	V
V_i	Input voltage	-0.3 to + 32	V
	Output short-circuit to GND - V + < 15V and T_{amb} = 25°C	Continuous	
T_{op}	Operating temperature	0 to 70	°C
T_{stg}	Storage temperature	-65 to 150	°C
T_j	Junction temperature	150	°C

CONNECTION DIAGRAM AND ORDERING NUMBERS
(top view)



Ceramic Minidip	Plastic Minidip	SO-8
NE532FE	NE532N	NE532D

THERMAL DATA

			Plastic Minidip	Ceramic Minidip	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	120°C/W	150°C/W	200°C/W

ELECTRICAL CHARACTERISTICS (V_s = 5V, T_{amb} = 0 to 70°C)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
I_S	Supply current	$R_L = \infty$	V_s = 30V		1	2	mA
					0.5	1.2	
I_b	Input bias current	T_{amb} = 25°C			45	250	nA
						500	
V_{os}	Input offset voltage	R_g = 0 V_s = 5V to 30V	T_{amb} = 25°C		2	7	mV
						9	
$\frac{\Delta V_{os}}{\Delta T}$	Input offset voltage drift	R_g = 0			7		µV/°C
I_{os}	Input offset current	T_{amb} = 25°C			5	50	nA
						150	
$\frac{\Delta I_{os}}{\Delta T}$	Input offset current drift				10		pA/°C
I_{sc}	Output short circuit to ground current	T_{amb} = 25°C (*)			40	60	mA
G_v	Large signal open loop voltage gain	V_s = 15V $R_L \geq$ 2KΩ	T_{amb} = 25°C	88	100		dB
				83			
	Input common-mode voltage range	V_s = 30V	T_{amb} = 25°C	0		V_s-1.5	V
				0		V_s-2	
V_o	Output voltage swing	T_{amb} = 25°C	R_L = 2KΩ			V_s-1.5	V
			$R_L \geq$ 10KΩ				
		V_s = 30V	R_L = 2KΩ	26			V
			$R_L \geq$ 10KΩ	27	28		
$V_{o\ sat}$	Output saturation voltage to ground	$R_L \leq$ 10KΩ			5	20	mV
CMR	Common mode rejection	T_{amb} = 25°C		65	70		dB
SVR	Supply voltage rejection	T_{amb} = 25°C		65	70		dB
CS	Channel separation	f = 1KHz to 20KHz T_{amb} = 25°C (input referred)			120		dB
I_o+	Output source current	V_s = 15V V_i+ = 1V V_i- = 0V	T_{amb} = 25°C	20	40		mA
				10	20		
I_o-	Outpur sink current	V_i+ = 0V V_i- = 1V V_o = 200mV	T_{amb} = 25°C	12	50		µA
		V_i- = 1V V_i+ = 0V V_s = 15V	T_{amb} = 25°C	10	20		mA
				5	8		

(*) Short circuits from the output to positive supply voltage can cause excessive heating and eventual destruction. The maximum output current is a 40mA typ. Independent of the magnitude of V_s. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Fig. 1 - Supply current vs. supply voltage

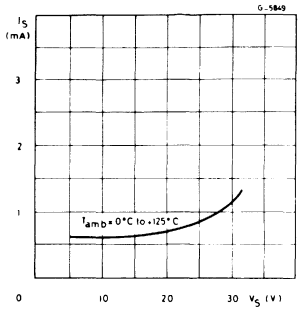


Fig. 2 - Input voltage range vs. supply voltage

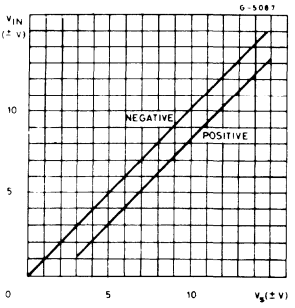


Fig. 3 - Output short circuit current vs. ambient temperature

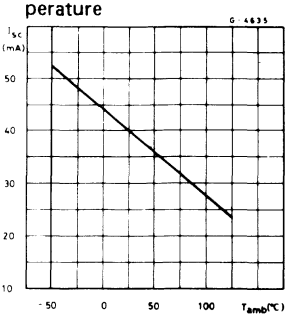


Fig. 4 - Open loop frequency reponse

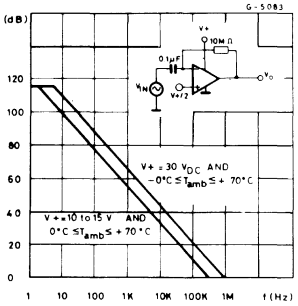


Fig. 5 - Large signal frequency response

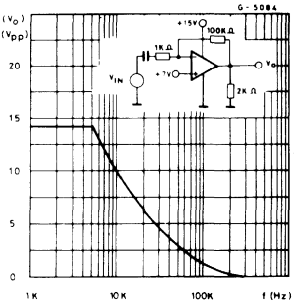


Fig. 6 - Voltage follower pulse response (small signal)

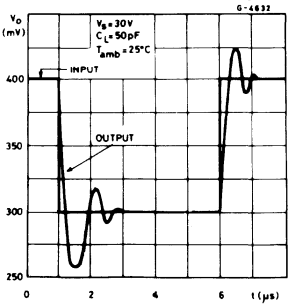


Fig. 7 - Input current

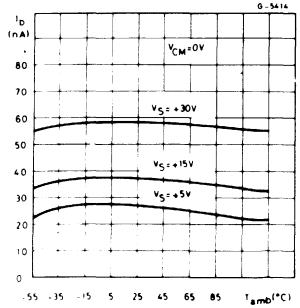


Fig. 8 - Output characteristics vs. current sourcing

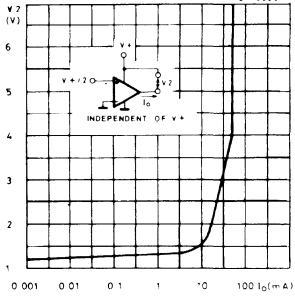
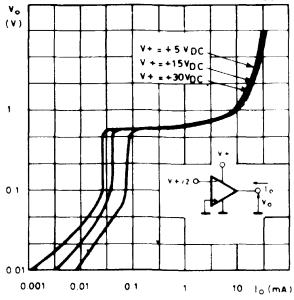


Fig. 9 - Output characteristics vs. current sinking



APPLICATION INFORMATION

The NE532 can operate with a single power supply voltage, has true-differential inputs and remains in the linear mode with an input common-mode voltage of 0V. The two included op amps work over a wide range of power supply voltage with little change in performance characteristics. At 25°C operation is possible down to a minimum supply voltage of 2.3V.

The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_s-15V, but either or both inputs can go to + 32V without damage.

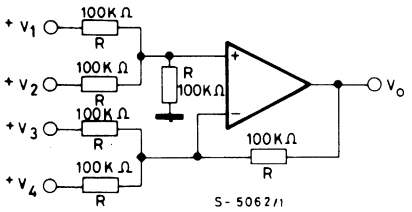
If the voltage at any of the input leads is driven negative (V_{in} < -0.3), the collector-base junction of the input PNP transistor becomes forward biased and thereby acts as an input diode clamps (max current: 50mA). In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This can cause the output voltage to go to the positive supply voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage again returns positive (V_{in} > -0.3V). The output stage design allows the amplifiers to both source and sink large output currents.

Therefore both NPN and PNP external current boost transistors can be used extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperature. **Putting direct short-circuit on more than one amplifier at a time, the total IC power dissipation will increase to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers.** The larger value of output source current which a available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

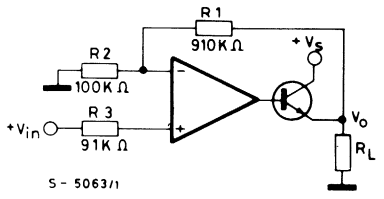
Typical single supply application circuits (V_s = 5V)

Fig. 10 - DC summing amplifier



where: $V_o = V_1 + V_2 - V_3 - V_4$
$(V_1 + V_2)' \geq (V_3 + V_4)$ to keep V_o > 0V

Fig. 11 - Power amplifier



V_o= 0V for V_{IN}= 0V
G_v= 20 dB

APPLICATION INFORMATION (continued)

Fig. 12 - LED driver

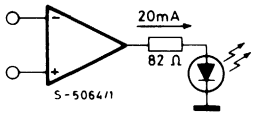


Fig. 13 - Lamp driver

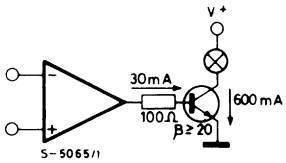
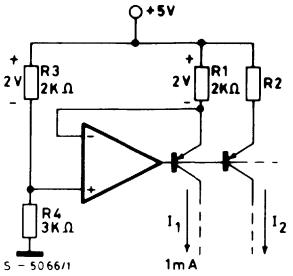
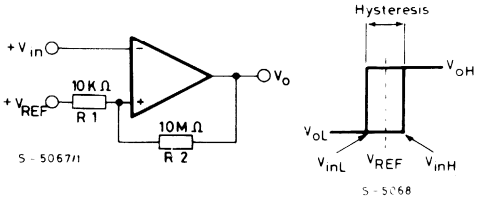


Fig. 14 - Fixed current sources



$$I_2 = \left(\frac{R1}{R2}\right) I_1$$

Fig. 15 - Comparator with Hysteresis

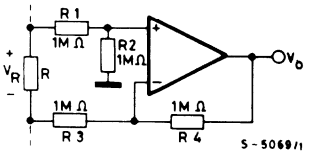


$$V_{in\ L} = \frac{R1}{R1 + R2} (V_{OL} - V_{REF}) + V_{REF}$$

$$V_{in\ H} = \frac{R1}{R1 + R2} (V_{OH} - V_{REF}) + V_{REF}$$

$$\text{Hysteresis} = \frac{R1}{R1 + R2} (V_{OH} - V_{OL})$$

Fig. 16 - Ground referencing a differential input signal



$$V_O = V_R$$

Fig. 17 - Driving TTL

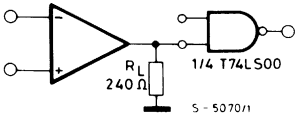
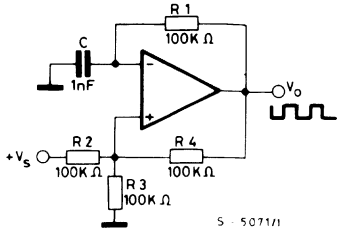
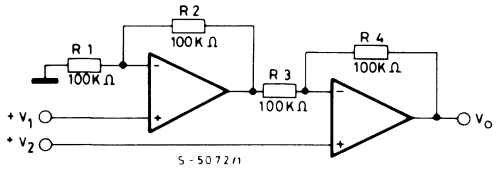


Fig. 18 - Squarewave oscillator



APPLICATION INFORMATION (continued)

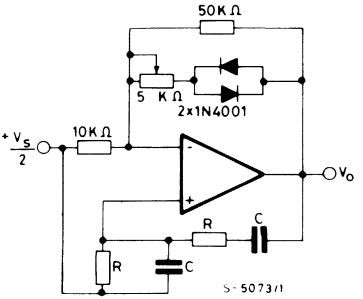
Fig. 19 - High input Z, DC differential amplifier



For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

$V_O = 1 + \frac{R4}{R3}$ (V2 – V1)

Fig. 20 - Wien bridge oscillator



$f_o = \frac{1}{2 \pi RC}$

Fig. 21 - Full wave rectifier

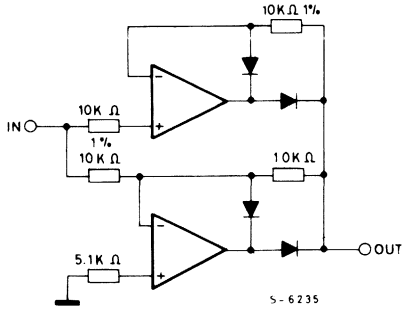


Fig. 22 - Half wave rectifier

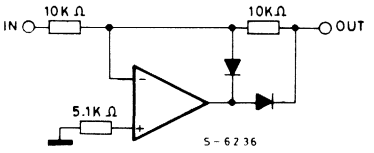
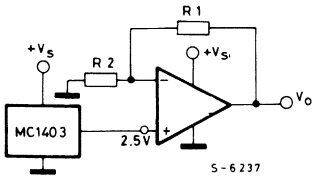
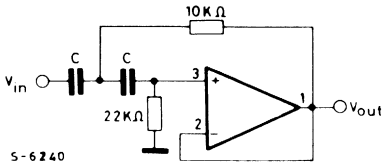


Fig. 23 - Low pass filter



$V_o = 2.5\ V\ (1 + \frac{R1}{R2})$

Fig. 24 - High-pass filter



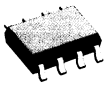
f_c = 100 Hz with C = 0.1 μF

TIMER

- TURN OFF TIME LESS THAN 2μs
- MAXIMUM OPERATING FREQUENCY GREATER THAN 500kHz
- TIMING FROM MICROSECONDS TO HOURS
- OPERATES IN BOTH ASTABLE AND MONOSTABLE MODES
- HIGH OUTPUT CURRENT
- ADJUSTABLE DUTY CYCLE
- TTL COMPATIBLE
- TEMPERATURE STABILITY OF 0.005% PER °C

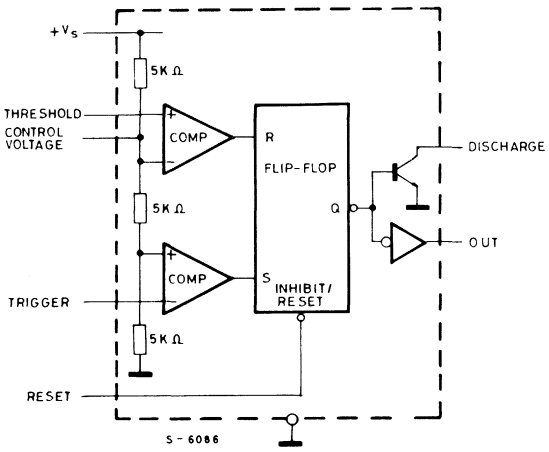
The NE555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA. The NE555 is available in plastic and ceramic Minidip package and in a 8-lead micropackage version.

Minidip
(Plastic and Ceramic)



SO-8

BLOCK DIAGRAM



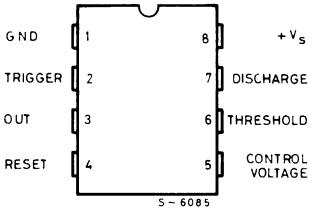
NE555
SA555
SE555

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage for **SE555**		18	V
	for **NE555**		16	V
T_{op}	Operating temperature range	for **NE555**	0 to 70	°C
		for **SA555**	-40 to 85	°C
		for **SE555**	-55 to 125	°C
T_j	Junction temperature		150	°C
T_{stg}	Storage temperature range		-65 to 150	°C

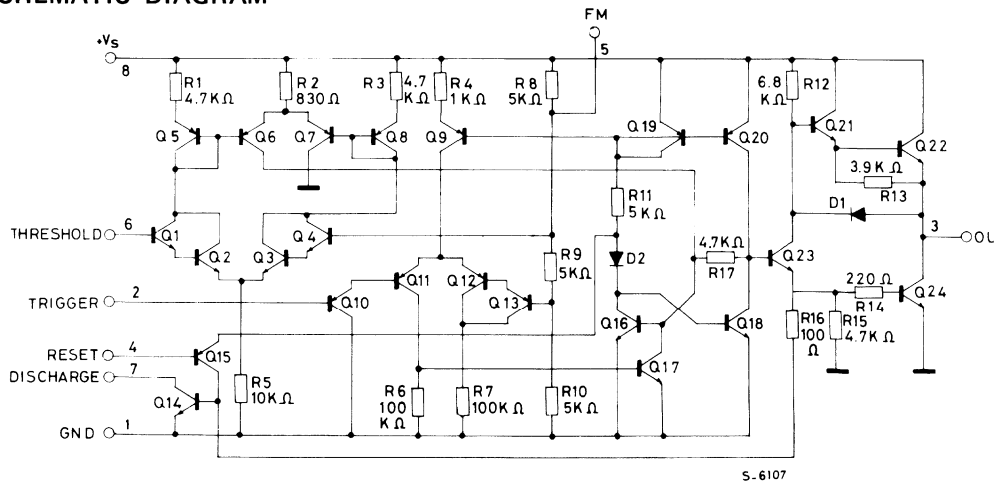
CONNECTION DIAGRAM AND ORDERING NUMBERS

(top view)



Temperature range	Plastic Minidip	Ceramic Minidip	SO-8
Commercial 0 to 70°C	NE555N	NE555FE	NE555D
Automotive -40 to 85°C	SA555N	–	–
Military -55 to 125°C	–	SE555FE	–

SCHEMATIC DIAGRAM



THERMAL DATA

			Plastic Minidip	Ceramic Minidip	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max.	120°C/W	150°C/W	200°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_s = 5 to 15V unless otherwise specified)

Parameter		Test conditions	NE555			SE555			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_s	Supply voltage		4.5		16	4.5		18	V
I_s	Supply current (low state) (1)	V_s= 5V R_L=∞ V_s= 15V R_L= ∞		3 10	6 15		3 10	5 12	mA mA
E_{tm}	Timing error (monostable) Initial accuracy (2) Drift with temperature Drift with supply voltage	R_A= 2 to 100KΩ C= 0.1μF		1 50 0.1	3 0.5		0.5 30 0.05	2 100 0.2	% ppm/°C %V
E_{ta}	Timing error (astable) Initial accuracy (2) Drift with temperature Drift with supply voltage	R_A, R_B= 1 to 100KΩ C= 0.1μF V_{cc}= 15V		2.25 150 0.3			1.5 90 0.15		% ppm/°C %/V
V_C	Control voltage level	V_s= 15V V_s= 5V	9 2.6	10 3.3	11 4	9.6 2.9	10 3.3	10.4 3.8	V V
V_T	Threshold voltage	V_s= 15V V_s= 5V	8.8 2.4	10 3.3	11.2 4.2	9.4 2.7	10 3.3	10.6 4.0	V V
I_T	Threshold current (3)			0.1	0.25		0.1	0.25	μA
VTR	Trigger voltage	V_s= 15V V_s= 5V	4.5 1.1	5 1.67	5.6 2.2	4.8 1.45	5 1.67	5.2 1.9	V V
I_{TR}	Trigger current	V_{TR}= 0		0.5	2		0.5	0.9	μA
V_R	Reset voltage (4)		0.4	0.7	1	0.4	0.7	1	V
I_R	Reset current	V_R= 0		0.4 0.1	1.5 0.4		0.4 0.1	1 0.4	mA mA
V_{OL}	Output voltage (low)	V_s= 15V I_{SINK}= 10mA I_{SINK}= 50mA I_{SINK}= 100mA I_{SINK}= 200mA V_s= 5V I_{SINK}= 8mA I_{SINK}= 5mA		 0.1 0.4 2 2.5 0.3 0.25	 0.25 0.75 2.5 0.4 0.35		 0.1 0.4 2 2.5 0.1 0.05	 0.15 0.5 2.2 0.25 0.2	 V V V V V V
V_{OH}	Output voltage (high)	V_s= 15V I_{SOURCE}= 200mA I_{SOURCE}= 100mA V_s= 5V I_{SOURCE}= 100mA	 12.75 2.75	 12.5 13.3 3.3	 	 13 3	 12.5 13.3 3.3	 	 V V V
t_{off}	Turn off time (5)	V_{RESET}= V_s		0.5			0.5	2	μs
t_r	Rise time of output			100	300		100	200	ns
t_f	Fall time of output			100	300		100	200	ns
I_L	Discharge leakage current			20	100		20	100	nA

NOTES

1. Supply current when output high typically 1mA less.
2. Tested at V_s = 5V and V_s = 15V
3. This will determine the maximum value of R_A + R_B, for 15V operation, the max total R = 10MΩ, and for 5V operation, the max total R= 3.5MΩ.
4. Specified with triggered input high.
5. Time measured from a positive going input pulse from 0 to 0.8 x V_s into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

Fig. 1 - Minimum pulse width required for triggering

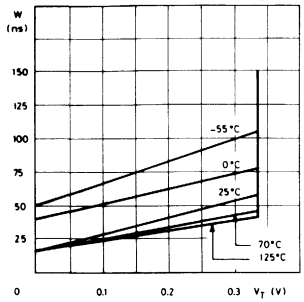


Fig. 2 - Supply current vs. supply voltage

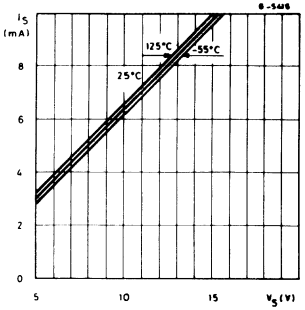


Fig. 3 - Delay time vs. temperature

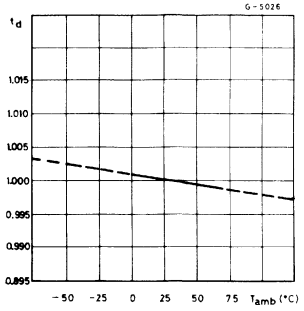


Fig. 4 - Low output voltage vs. output sink current

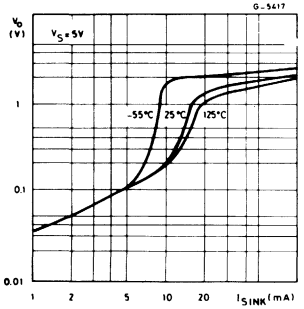


Fig. 5 - Low output voltage vs. output sink current

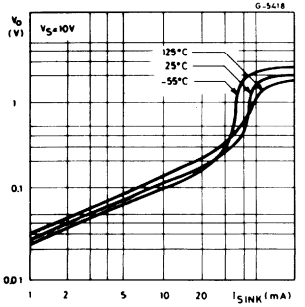


Fig. 6 - Low output voltage vs. output sink current

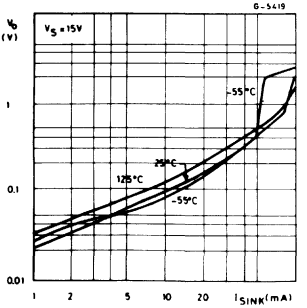


Fig. 7 - High output voltage drop vs. output source current

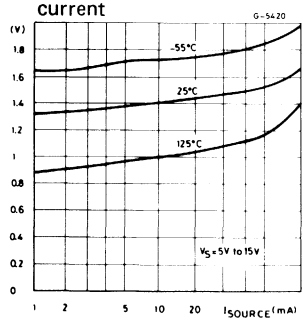


Fig. 8 - Delay time vs. supply voltage

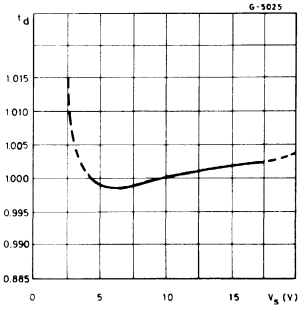
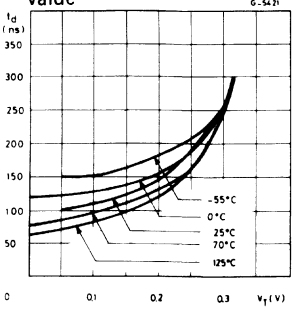


Fig. 9 - Propagation delay vs. voltage level of trigger value



APPLICATION INFORMATION

MONOSTABLE OPERATION

In the monostable mode, the timer functions as a one-shot. Referring to Figure 10 the external capacitor is initially held discharged by a transtor inside the timer.

The circuit triggers on a negative-going input signal when the level reaches 1/3 V_s. Once triggered, the circuit remains in this state until the set time has elapsed, even if it is triggered again during this interval. The duration of the output HIGH state is given by t = 1.1 R1C1 and is easily determined by figure 12. Notice that since the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the Reset terminal (pin 4) and the Trigger terminal (pin2) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse in applied, the output is driven to its LOW state.

When a negative trigger pulse is applied to pin 2, the flip-flop is set, releasing the short circuit across the external capacitor and driving the output HIGH. The voltage across the capacitor increases exponentially with the time constant τ = R1C1. When the voltage across the capacitor equals 2/3 V_s, the comparator resets the flip-flop which then discharge the capacitor rapidly and drivers the output to its LOW state.

Figure 11 shows the actual waveforms generated in this mode of operation.

When Reset is not used, it should be tied high to avoid any possibly or false triggering.

Fig. 10

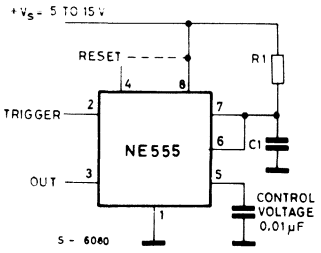


Fig. 11

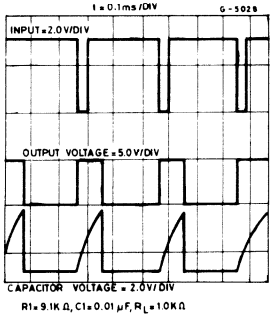
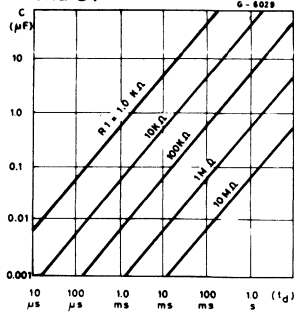


Fig. 12 - Time Delay vs R1 and C1



ASTABLE OPERATION

When the circuit is connected as shown in Figure 13 (pin 2 and 6 connected) it triggers itself and free runs as a multivibrator. The external capacitor charges through R1 and R2 and discharges through R2 only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

In the astable mode of operation, C1 charges and discharges between 1/3 V_s and 2/3 V_s. As in the triggered mode, the charge and discharge times and therefore frequency are independent of the supply voltage.

Figure 14 shows actual waveforms generated in this mode of operation.

The charge time (output HIGH) is given by:

$$t_1 = 0.693\ (R1 + R2)\ C1$$

and the discharge time (output LOW) by:

$$t_2 = 0.693\ (R2)\ C1$$

Thus the total period T is given by:

$$T = t_1 + t_2 = 0.693\ (R1 + 2R2)\ C1$$

The frequency of oscillation is then:

$$f = \frac{1}{T} = \frac{1.44}{(R1 + 2R2)\ C1}$$

and may be easily found by Figure 15

The duty cycle is given by:

$$D = \frac{R2}{R1 + 2R2}$$

APPLICATION INFORMATION (continued)

Fig. 13

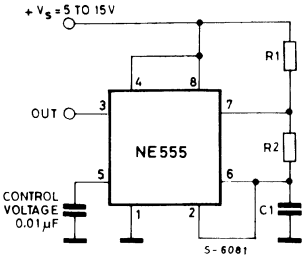


Fig. 14

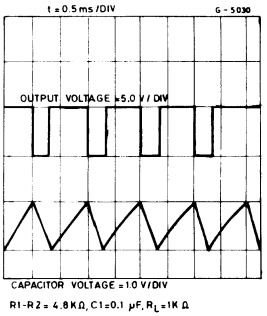
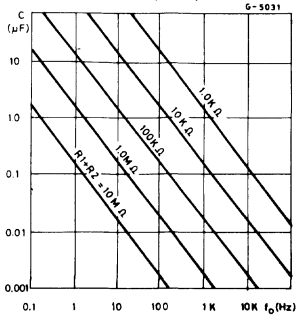


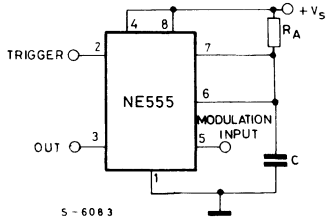
Fig. 15 - Free Running Frequency vs R1, R2, and C1



PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. Figure 16 shows the circuit.

Fig. 16 - Pulse Width Modulator



LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. Figure 17 shows a circuit configuration that will perform this function.

Fig. 17

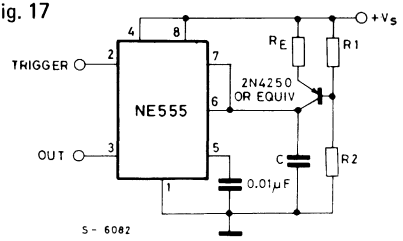
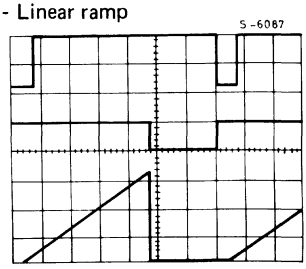


Figure 18 shows waveforms generator by the linear ramp.

The time interval is given by:

$$T = \frac{2/3\ V_S\ R_E\ (R_1 + R_2)\ C}{R_1\ V_S - V_{BE}\ (R_1 + R_2)} \qquad V_{BE} \cong 0.6V$$

Fig. 18 - Linear ramp



V_S = 5V
TIME = 20μs/DIV
R_1 = 47KΩ
R_2 = 100KΩ
R_E = 2.7KΩ
C = 0.01 μF

Top trace: input 3V/DIV
Middle trace: output 5V/DIV
Bottom trace: output 5V/DIV
Bottom trace: capacitor voltage 1V/DIV

50% DUTY CYCLE OSCILLATOR;

For a 50% duty cycle the resistors R_A and R_B may be connected as in Figure 19. The time period for the output high is the same as previous, $t_1 = 0.693\ R_A\ C$.

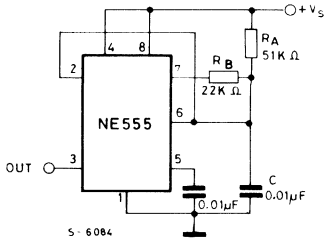
APPLICATION INFORMATION (continued)

For the output low it is $t_2 =$

$$[(R_A R_B)/(R_A + R_B)]\, C \ln\left\{\frac{R_B - 2R_A}{2R_B - R_A}\right\}$$

Thus the frequency of oscillation is $f = \dfrac{1}{t_1 + t_2}$

Figure 19 - 50% Duty cycle oscillator



Note that this circuit will not oscillate if R_B is greater than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_s and trigger the lower comparator.

ADDITIONAL INFORMATION

Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1μF in parallel with 1μF electrolytic.

Lower comparator storage time can be as long as 10μs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10μs minimum.

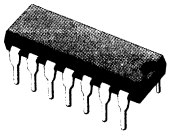
Delay time reset to output is 0.47μs typical. Minimum reset pulse width must be 0.3μs, typical. Pin 7 current switches within 30ns of the output (pin 3) voltage.

NE556
SA556
SE556

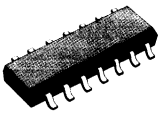
DUAL TIMER

- TURN OFF TIME LESS THAN 2μs
- MAXIMUM OPERATING FREQUENCY GREATER THAN 500kHz
- TIMING FROM MICROSECONDS TO HOURS
- OPERATES IN BOTH ASTABLE AND MONOSTABLE MODES
- HIGH OUTPUT CURRENT
- ADJUSTABLE DUTY CYCLE
- TTL COMPATIBLE
- TEMPERATURE STABILITY OF 0.005% PER °C

The NE556 dual monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA. The NE556 is available in plastic and ceramic package and in a 14-lead micropakage version.

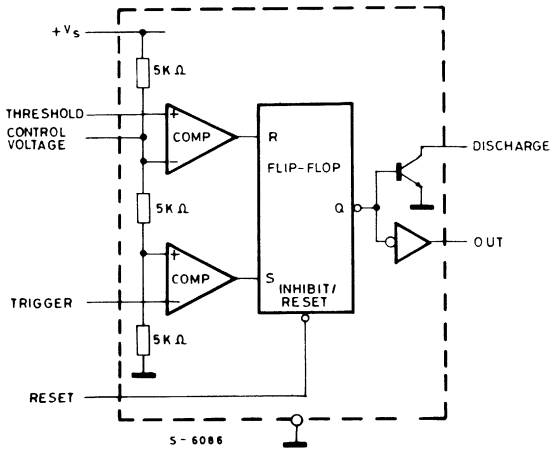


Plastic and Ceramic DIP-14



SO-14

BLOCK DIAGRAM (one section)

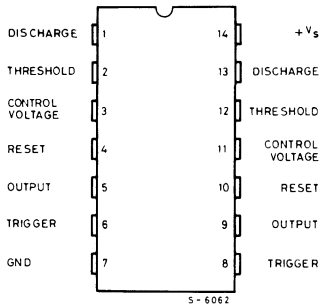


NE556
SA556
SE556

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	for **SE556**	18	V
		for **NE556**	16	V
T_{op}	Operating temperature range	for **NE556**	0 to 70	°C
		for **SA556**	-40 to 85	°C
		for **SE556**	-55 to 125	°C
T_{stg}	Storage temperature range		-65 to 150	°C
T_j	Junction temperature		150	°C

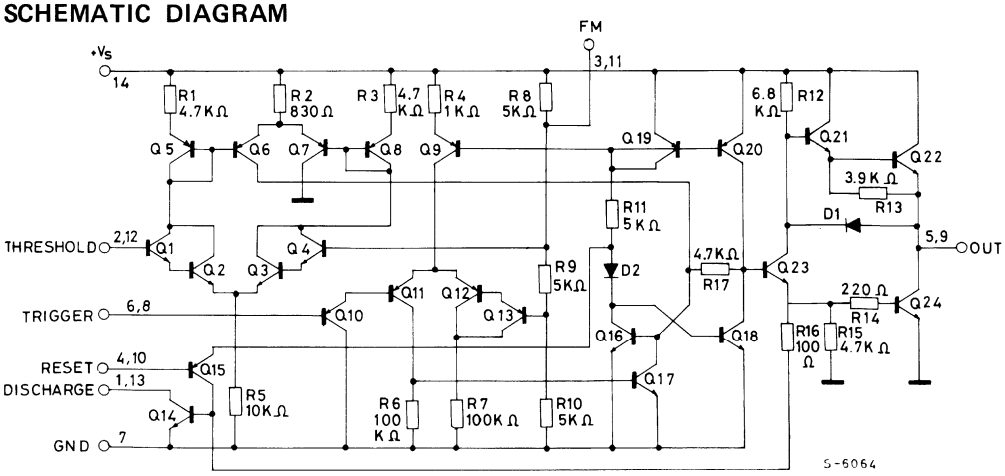
CONNECTION DIAGRAM



ORDERING NUMBERS

Temperature range	Plastic DIP-14	Ceramic DIP-14	SO-14
Commercial 0 to 70°C	NE556N	NE556F	NE556D
Automotive -40 to 85°C	SA556N	–	–
Military -55 to 125°C	–	SE556F	–

SCHEMATIC DIAGRAM



THERMAL DATA

			Ceramic DIP-14	SO-14	Plastic DIP-14
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max.	150°C/W	165°C/W	200°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_s = 5 to 15V unless otherwise specified)

Parameter		Test conditions	NE556/SA556			SE556			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_s	Supply voltage		4.5		16	4.5		18	V
I_s	Supply current (low state) (1)	V_s= 5V R_L=∞ V_s= 15V R_L= ∞		6 20	12 30		6 20	10 24	mA mA
E_{tm}	Timing error (monostable) Initial accuracy (2) Drift with temperature Drift with supply voltage	R_A= 2 to 100KΩ C= 0.1μF		 1 50 0.1	 3 0.5		 0.5 30 0.05	 2 100 0.2	 % ppm/°C %V
E_{ta}	Timing error (astable) Initial accuracy (2) Drift with temperature Drift with supply voltage	R_A, R_B= 1 to 100KΩ C= 0.1μF V_{cc}= 15V		 2.25 150 0.3	 		 1.5 90 0.15	 	 % ppm/°C %/V
V_C	Control voltage level	V_s= 15V V_s= 5V	9 2.6	10 3.3	11 4	9.6 2.9	10 3.3	10.4 3.8	V V
V_T	Threshold voltage	V_s= 15V V_s= 5V	8.8 2.4	10 3.3	11.2 4.2	9.4 2.7	10 3.3	10.6 4.0	V V
I_T	Threshold current (3)			0.1	0.25		0.1	0.25	μA
VTR	Trigger voltage	V_s= 15V V_s= 5V	4.5 1.1	5 1.67	5.6 2.2	4.8 1.45	5 1.67	5.2 1.9	V V
I_{TR}	Trigger current	V_{TR}= 0		0.5	2		0.5	0.9	μA
V_R	Reset voltage (4)		0.4	0.7	1	0.4	0.7	1	V
I_R	Reset current	V_R= 0		0.4 0.1	1.5 0.4		0.4 0.1	1 0.4	mA mA
V_{OL}	Output voltage (low)	V_s= 15V I_{SINK}= 10mA I_{SINK}= 50mA I_{SINK}= 100mA I_{SINK}= 200mA V_s= 5V I_{SINK}= 8mA I_{SINK}= 5mA		 0.1 0.4 2 2.5 0.3 0.25	 0.25 0.75 2.5 0.4 0.35		 0.1 0.4 2 2.5 0.1 0.05	 0.15 0.5 2.2 0.25 0.2	 V V V V V V
V_{OH}	Output voltage (high)	V_s= 15V I_{SOURCE}= 200mA I_{SOURCE}= 100mA V_s= 5V I_{SOURCE}= 100mA	 12.75 2.75	 12.5 13.3 3.3	 	 13 3	 12.5 13.3 3.3	 	 V V V
t_{off}	Turn off time (5)	V_{RESET}= V_s		0.5			0.5	2	μs
t_r	Rise time of output			100	300		100	200	ns
t_f	Fall time of output			100	300		100	200	ns
I_L	Discharge leakage current			20	100		20	100	nA

NOTES

1. Supply current when output high typically 1mA less.
2. Tested at V_s = 5V and V_s = 15V
3. This will determine the maximum value of R_A + R_B, for 15V operation, the max total R = 10MΩ, and for 5V operation, the max total R= 3.5MΩ.
4. Specified with triggered input high.
5. Time measured from a positive going input pulse from 0 to 0.8 x V_s into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

Fig. 1 - Minimum pulse width required for triggering

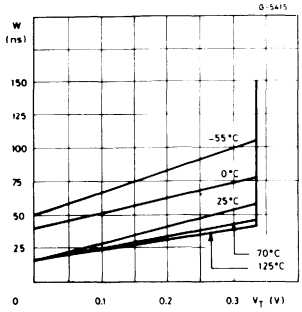


Fig. 2 - Supply current vs. supply voltage

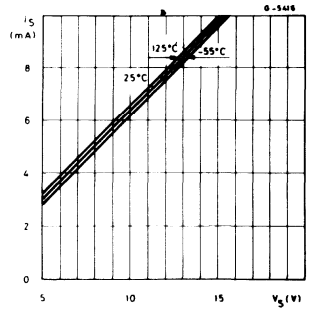


Fig. 3 - Delay time vs. temperature

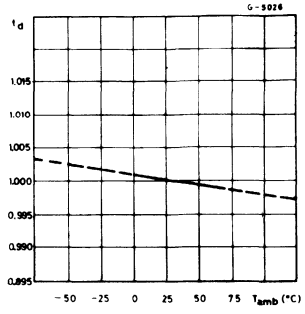


Fig. 4 - Low output voltage vs. output sink current

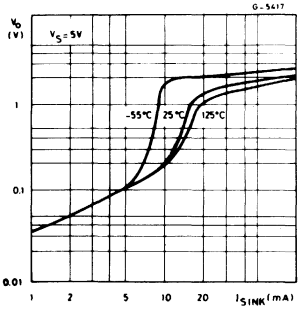


Fig. 5 - Low output voltage vs. output sink current

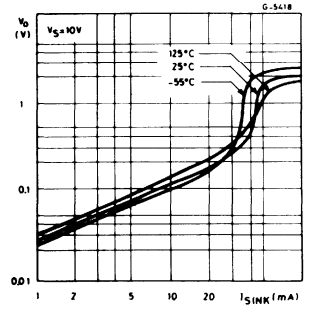


Fig. 6 - Low output voltage vs. output sink current

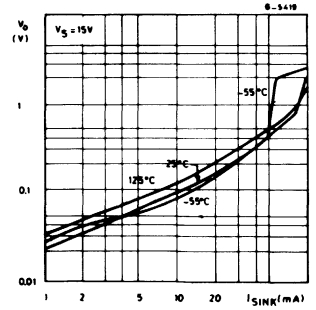


Fig. 7 - High output voltage drop vs. output source current

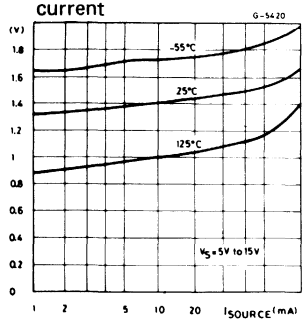


Fig. 8 - Delay time vs. supply voltage

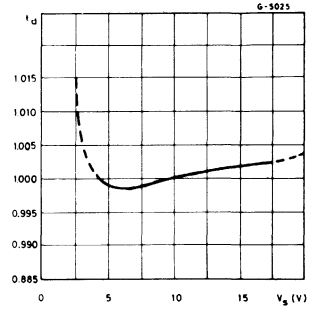
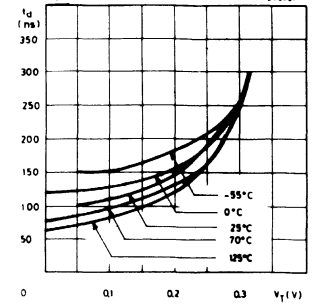


Fig. 9 - Propagation delay vs. voltage level of trigger value

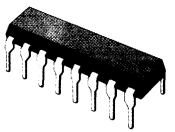


SG1524
SG2524
SG3524

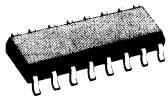
REGULATING PULSE WIDTH MODULATORS

- COMPLETE PWM POWER CONTROL CIRCUITRY
- UNCOMMITTED OUTPUTS FOR SINGLE-ENDED OR PUSH PULL APPLICATIONS
- LOW STANDBY CURRENT..8mA TYPICAL
- OPERATION UP TO 300 KHz
- 1% MAXIMUM TEMPERATURE VARIATION OF REFERENCE VOLTAGE

The SG1524, SG2524, and SG3524 incorporate on a single monolithic chip all the function required for the construction of regulating power supplies inverters or switching regulators. They can also be used as the control element for high power-output applications. The SG1524 family was designed for switching regulators of either polarity, transformer-coupled dc-to-dc converters, transformerless voltage doublers and polarity converter applications employing fixed-frequency, pulse-width modulation techniques. The dual alternating outputs allows either single-ended or push-pull applications. Each device includes an on-chip reference, error amplifier, programmable oscillator, pulse-steering flip-flop, two uncommitted output transistors, a high-gain comparator, and current-limiting and shut-down circuitry.



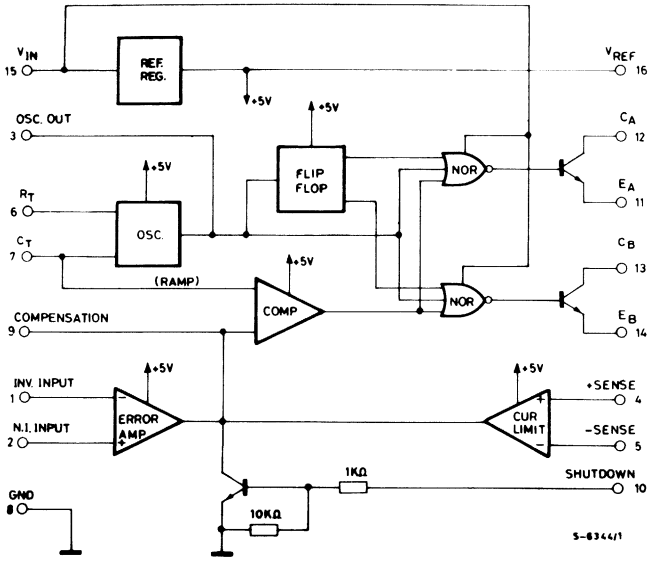
DIP-16 Plastic (0.25) **and Ceramic**



SO-16P

ORDERING NUMBERS: SG1524J - SG2524J - SG3524J (Ceramic)
SG2524N - SG3524N (Plastic)
SG2524P - SG3524P (SO-16P)

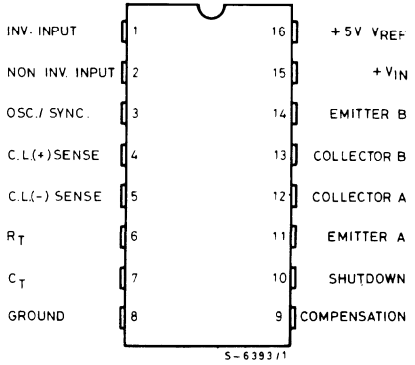
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{IN}	Supply voltage		40	V
I_c	Collector output current		100	mA
I_R	Reference output current		50	mA
I_T	Current through C_T terminal		-5	mA
P_{tot}	Total power dissipation at $T_{amb} = 70°C$		1000	mW
T_{stg}	Storage temperature range		-65 to 150	°C
T_{op}	Operating ambient temperature range	**SG1524**	-55 to 125	°C
		SG2524	-25 to 85	°C
		SG3524	0 to 70	°C

CONNECTION DIAGRAM



THERMAL DATA

			Plastic DIP-16	Ceramic DIP-16	SO-16P
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80°C/W	150°C/W	–
$R_{th\ j\text{-}aluminia}$	Thermal resistance junction-aluminia	max	–	–	50°C/W

* Thermal resistance junction-aluminia with the device soldered on the middle of an aluminia supporting substrate measuring 15 x 20 mm; 0.65 mm thickness with infinite heatsink.

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_j = -55°C to + 125°C for the SG1524, -25°C to + 85°C for the SG2524, and 0°C to + 70°C for the SG3524, V_{IN} = 20V, and f = 20KHz).

Parameter		Test condition	SG1524/SG2524			SG3524			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
REFERENCE SECTION									
V_{REF}	Output Voltage		4.8	5	5.2	4.6	5	5.4	V
ΔV_{REF}	Line Regulation	V_{IN} = 8 to 40V		10	20		10	30	mV
ΔV_{REF}	Load Regulation	I_L = 0 to 20mA		20	50		20	50	mV
	Ripple Rejection	f = 120Hz, T_j = 25°C		66			66		dB
	Short Circuit Curr. Limit	V_{REF} = 0, T_j = 25°C		100			100		mA
$\Delta V_{REF}/\Delta T$	Temp. Stability	Over Operating Temp. Range		0.3	1		0.3	1	%
ΔV_{REF}	Long Term Stability	T_j = 25°C, t = 1000 Hrs.		20			20		mV
OSCILLATOR SECTION									
f_{MAX}	Maximum Frequency	C_T = 0.001μF, R_T = 2kΩ		300			300		kHz
	Initial Accuracy	R_T and C_T Constant		5			5		%
	Voltage Stability	V_{IN} = 8 to 40V, T_j = 25°C			1			1	%
$\Delta f/\Delta T$	Temperature Stability	Over Operating Temp. Range			2			2	%
	Output Amplitude	Pin 3, T_j = 25°C		3.5			3.5		V
	Output Pulse Width	C_T = 0.01μF, T_j = 25°C		0.5			0.5		μs
ERROR AMPLIFIER SECTION									
V_{os}	Input Offset Voltage	V_{CM} = 2.5V		0.5	5		2	10	mV
I_b	Input Bias Current	V_{CM} = 2,5V		2	10		2	10	μA
G_V	Open Loop Volt. Gain		72	80		60	80		dB
CMV	Common Mode Volt.	T_j = 25°C	1.8		3.4	1.8		3.4	V
CMR	Comm. Mode Rejec.	T_j = 25°C		70			70		dB
B	Small Signal Bandwidth	A_v = 0dB, T_j = 25°C		3			3		MHz
V_o	Output Voltage	T_j = 25°C	0.5		3.8	0.5		3.8	V
COMPARATOR SECTION									
	Duty-Cycle	% Each Output On	0		45	0		45	%
V_{IT}	Input Threshold	Zero Duty-Cycle		1			1		V
V_{IT}	Input Threshold	Maximum Duty-Cycle		3.5			3.5		V
I_b	Input Bias Current			1			1		μA
CURRENT LIMITING SECTION									
	Sense Voltage	Pin 9 = 2V with Error Amplifier Set for Max. Out, T_j = 25°C	190	200	210	180	200	220	mV
	Sense Voltage T.C.			0.2			0.2		mV/°C
CMV	Common Mode Volt.		-1		+1	-1		+1	V
OUTPUT SECTION (Each Output)									
	Collector-Emitter Volt.		40			40			V
	Collector Leackage Cur.	V_{CE} = 40V		0.1	50		0.1	50	μA
	Saturation Voltage	I_c = 50mA		1	2		1	2	V
	Emitter Out. Voltage	V_{IN} = 20V	17	18		17	18		V
t_r	Rise Time	R_c= 2KΩ, T_j = 25°C		0.2			0.2		μs
t_f	Fall time	R_c= 2KΩ, T_j= 25°C		0.1			0.1		μs
I_q*	Total Standby Curr.	V_{IN} = 40V		8	10		8	10	mA

(*) Excluding oscillator charging current, error and current limit dividers, and with outputs open.

Fig. 1 - Open-loop voltage amplification of error amplifier vs. frequency.

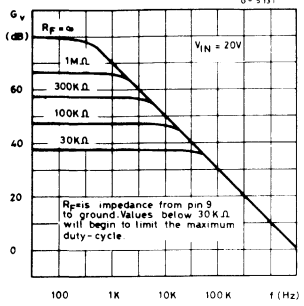


Fig. 2 - Oscillator frequency vs. timing components.

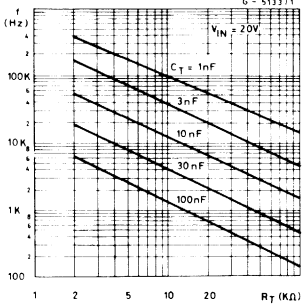


Fig. 3 - Output dead time vs. timing capacitance value.

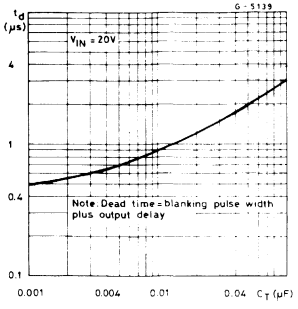


Fig. 4 Output saturation voltage vs. load current.

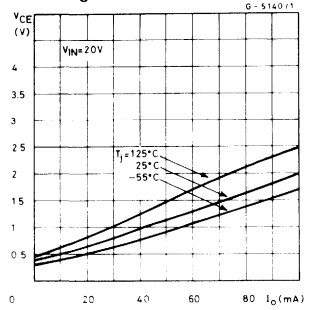
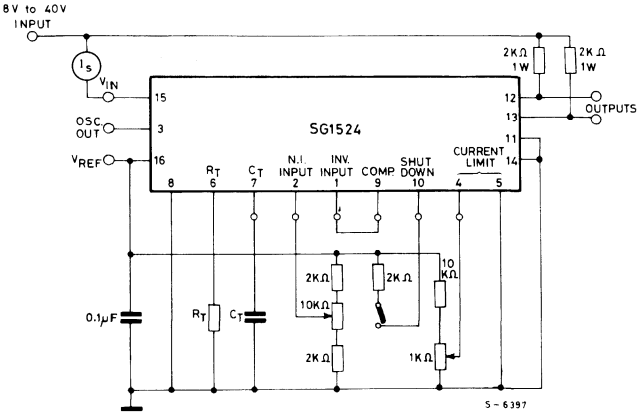


Fig. 5 - Open loop test circuit.



PRINCIPLES OF OPERATION

The SG1524 is a fixed-frequency pulse-with-modulation voltage regulator control circuit. The regulator operates at a frequency that is programmed by one timing resistor (R_T) and one timing capacitor (C_T). R_T established a constant charging current for C_T. This results in a linear voltage ramp at C_T, which is fed to the comparator providing linear control of the output pulse width by the error amplifier. The SG1524 contains, an on-board 5V regulator that serves as a reference as well as powering the SG1524's internal control circuitry and is also useful in supplying external support functions. This reference voltage is lowered externally by a resistor divider to provide a reference within the common-mode range of the error amplifier or an external reference may be used. The power supply output is sensed by a second resistor divider network to generale a feedback signal to the error amplifier. The amplifier output voltage is then compared to the linear voltage ramp at C_T. The resulting modulated pulse out of the high-gain comparator is then steered to the appropriate output pass transistors (Q_A or Q_B) by the pulse-steering flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to assure both outputs are never on simultaneously during the transition times. The width of the blanking pulse is controlled by the value of C_T. The

outputs may be applied in a push-pull configuration in which their frequency is half that of the base oscillator, or paralleled for single-ended applications in which the frequency is equal to that of the oscillator. The output of the error amplifier shares a common input to the comparator with the current limiting and shutdown circuitry and can be overridden by signals from either of these inputs. This common point is also available externally and may be employed to control the gain of, or to compensate, the error amplifier, or to provide additional control to the regulator.

RECOMMENDED OPERATING CONDITIONS

Supply voltage V_{IN}	8 to 40	V
Reference Output Current	0 to 20	mA
Current through C_T Terminal	-0.03 to -2	mA
Timing Resistor, R_T	1.8 to 100	KΩ
Timing Capacitor, C_T	0.001 to 0.1	μF

TYPICAL APPLICATIONS DATA

Oscillator

The oscillator controls the frequency of the SG1524 and is programmed by R_T and C_T according to the approximate formula:

$$f \simeq \frac{1.18}{R_T C_T}$$

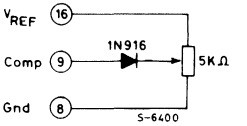
where R_T is in KΩ
C_T is in μF
f is in KHz

Pratical values of C_T fall between 0.001 and 0.1μF. Pratical values of R_T fall between 1.8 and 100KΩ. This results in a frequency range typically from 120Hz to 500KHz.

Blanking

The output pulse of the oscillator is used as a blanking pulse at the output. This pulse width is controlled by the value of C_T. If small values of C_T are required for frequency control, the oscillator output pulse width may still be increased by applying a shunt capacitance of up to 100pF from pin 3 to ground. If still greater dead-time is required, it should be accomplished by limiting the maximum duty cycle by clamping the output of the error amplifier. This can easily be done with the circuit below:

Fig. 6



Synchronous Operation

When an external clock is desired, a clock pulse of approximately 3V can be applied directly to the oscillator output terminal. The impedance to ground at this point is approximately 2KΩ. In this configuration R_T C_T must be selected for a clock period slightly greater than that of the external clock.

If two more SG1524 regulators are to be operated synchronously, all oscillator output terminals should be tied together, all C_T terminals connected to a single timing capacitor, and the timing resistor connected to a single R_T terminal. The other R_T terminals can be left open or shorted to V_{REF}. Minimum lead lengths should be used between the C_T terminals.

Fig. 7 - Push-pull transformer-coupled circuit.

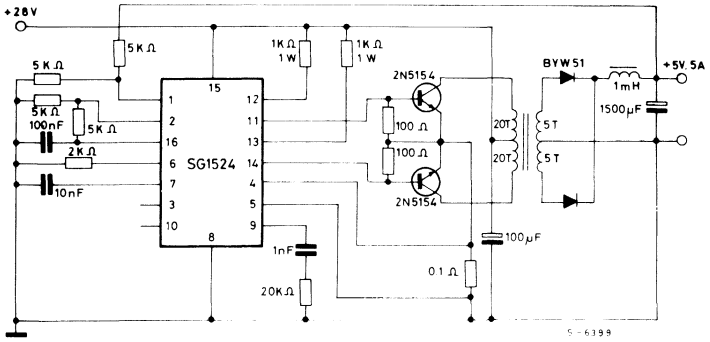
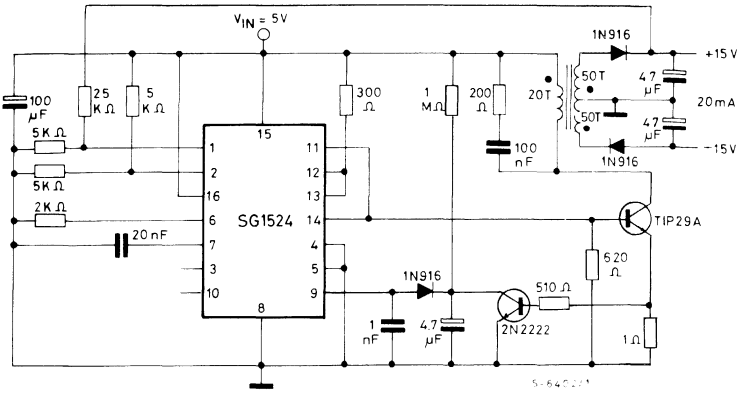


Fig. 8 - Flyback converter circuit



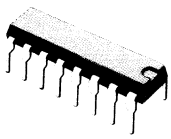
SG1525A/27A
SG2525A/27A
SG3525A/27A

REGULATING PULSE WIDTH MODULATORS

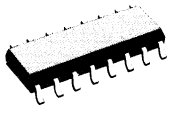
- 8 to 35V OPERATION
- 5.1V REFERENCE TRIMMED TO ± 1%
- 100Hz to 500KHz OSCILLATOR RANGE
- SEPARATE OSCILLATOR SYNC TERMINAL
- ADJUSTABLE DEADTIME CONTROL
- INTERNAL SOFT-START
- PULSE-BY-PULSE SHUTDOWN
- INPUT UNDERVOLTAGE LOCKOUT WITH HYSTERESIS
- LATCHING PWM TO PREVENT MULTIPLE PULSES
- DUAL SOURCE/SINK OUTPUT DRIVERS

The SG1525A/1527A series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The on-chip + 5.1V reference is trimmed to ± 1% and the input common-mode range of the error amplifier includes the reference voltage eliminating external resistors. A sync input to the oscillator allows multiple units to be slaved or a single unit to be synchronized to an external system clock. A single resistor between the C_T and the discharge terminals provide a wide range of dead time adjustment. These devices also feature built-in soft-start circuitry with only an external timing capacitor required.

A shutdown terminal controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for sub-normal input voltages. this lockout circuitry includes approximately 500mV of hysteresis for jitter-free operation. Another feature of these PWM circuits is a latch following the comparator. Once a PWN pulses has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200mA. The SG1525A output stage features NOR logic, giving a LOW output for an OFF state. The SG1527A utilizes OR logic which results in a HIGH output level when OFF.



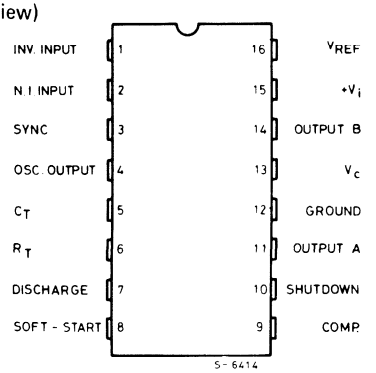
DIP-16 Plastic (0.25) **and Ceramic**



SO-16P

CONNECTION DIAGRAM AND ORDERING NUMBERS

(top view)



Type	Plastic DIP	Ceramic DIP	SO-16P
SG1525A	–	SG1525AJ	–
SG1527A	–	SG1527AJ	–
SG2525A	SG2525AN	SG2525AJ	SG2525AP
SG2527A	SG2527AN	SG2527AJ	SG2527AP
SG3525A	SG3525AN	SG3525AJ	SG3525AP
SG3527A	SG3527AN	SG3527AJ	SG3527AP

ABSOLUTE MAXIMUM RATINGS

V_i	Supply voltage	40	V
V_C	Collector supply voltage	40	V
I_{OSC}	Oscillator charging current	5	mA
I_o	Output current, source or sink	500	mA
I_R	Reference output current	50	mA
I_T	Current through C_T terminal	5	mA
	Logic inputs	-0.3 to +5.5	V
	Analog inputs	-0.3 to V_i	V
P_{tot}	Total power dissipation at T_{amb} = 70°C	1000	mW
T_j	Junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range	-65 to 150	°C
T_{op}	Operating ambient temperature: SG1525A/27A	-55 to 125	°C
	SG2525A/27A	-25 to 85	°C
	SG3525A/27A	0 to 70	°C

THERMAL DATA (DIP-16)

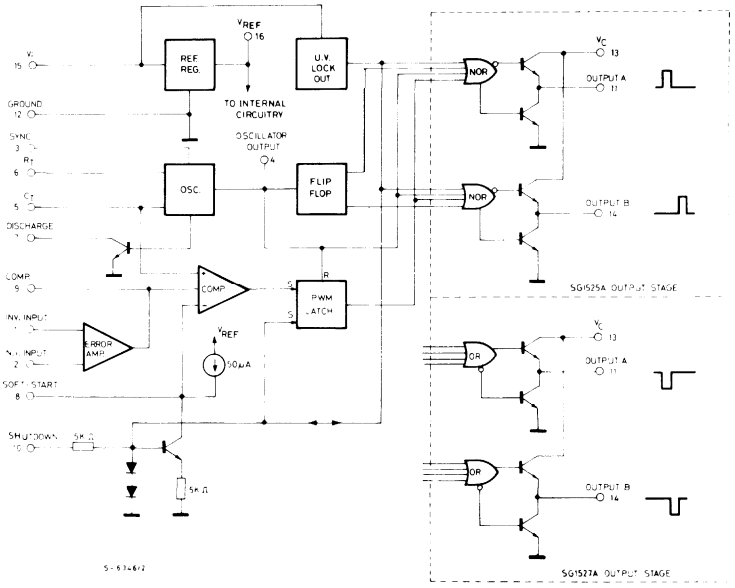
			Ceramic	Plastic
$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins	max	—	50°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	150°C/W	80°C/W

THERMAL DATA (SO-16P)

$R_{th\ j\text{-}alumina}$*	Thermal resistance junction-alumina	max	50	°C/W

(*) Thermal resistance junction-alumina with the device soldered on the middle of an alumina supporting substrate measuring 15 x 20 mm; 0.65 mm thickness with infinite heatsink.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (V_i = 20V, and over operating temperature, unless otherwise specified)

Parameter		Test conditions	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
REFERENCE SECTION									
V_{REF}	Output voltage	T_j = 25°C	5.05	5.1	5.15	5	5.1	5.2	V
ΔV_{REF}	Line regulation	V_i = 8 to 35V		10	20		10	20	mV
ΔV_{REF}	Load regulation	I_L = 0 to 20 mA		20	50		20	50	mV
$\Delta V_{REF}/\Delta T$*	Temp. stability	Over operating range		20	50		20	50	mV
*	Total output variation	Line, load and temperature	5		5.2	4.95		5.25	V
	Short circuit current	V_{REF}= 0 T_j = 25°C		80	100		80	100	mA
*	Output noise voltage	10Hz ≤ f ≤ 10kHz, T_j=25°C		40	200		40	200	μVrms
ΔV_{REF}*	Long term stability	T_j = 125°C, 1000 hrs		20	50		20	50	mV
OSCILLATOR SECTION**									
*, •	Initial accuracy	T_j = 25°C		± 2	± 6		± 2	± 6	%
*, •	Voltage stability	V_i = 8 to 35V		± 0.3	± 1		± 1	± 2	%
$\Delta f/\Delta T$*	Temp. stability	Over operating range		± 3	± 6		± 3	± 6	%
f_{MIN}	Minim. frequency	R_T = 200 KΩ C_T= 0.1 μF			120			120	Hz
f_{MAX}	Maxim. frequency	R_T = 2 KΩ C_T= 470 pF	400			400			KHz
	Current mirror	I_{RT}= 2 mA	1.7	2	2.2	1.7	2	2.2	mA
*, •	Clock amplitude		3	3.5		3	3.5		V
*, •	Clock width	T_j = 25°C	0.3	0.5	1	0.3	0.5	1	μs
	Sync threshold		1.2	2	2.8	1.2	2	2.8	V
	Sync input current	Sync voltage = 3.5V		1	2.5		1	2.5	mA
ERROR AMPLIFIER SECTION (V_{CM} = 5.1V)									
V_{OS}	Input offset voltage			0.5	5		2	10	mV

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_b	Input bias current			1	10		1	10	µA
I_{os}	Input offset current				1			1	µA
	DC open loop gain	$R_L \geq 10\,M\Omega$	60	75		60	75		dB
*	Gain bandwidth product	G_v = 0 dB T_j = 25°C	1	2		1	2		MHz
*, ■	DC transconduc.	$30K\Omega \leq R_L \leq 1M\Omega$ T_j = 25° C	1.1	1.5		1.1	1.5		mS
	Output low level			0.2	0.5		0.2	0.5	V
	Output high level		3.8	5.6		3.8	5.6		V
CMR	Comm.mode rejec.	V_{CM}= 1.5 to 5.2V	60	75		60	75		dB
PSR	Supply voltage rejection	V_i = 8 to 35V	50	60		50	60		dB

PWM COMPARATOR

	Minim. duty-cycle				0			0	%
	Maxim. duty-cycle		45	49		45	49		%
•	Input threshold	Zero duty-cycle	0.7	0.9		0.7	0.9		V
		Maximum duty-cycle		3.3	3.6		3.3	3.6	V
*	Input bias current			0.05	1		0.05	1	µA

SHUTDOWN SECTION

	Soft start current	V_{SD}= 0V, V_{SS}= 0V	25	50	80	25	50	80	µA
	Soft start low level	V_{SD}= 2.5V		0.4	0.7		0.4	0.7	V
	Shutdown threshold	To outputs, V_{SS}= 5.1V T_j = 25°C	0.6	0.8	1	0.6	0.8	1	V
	Shutdown input current	V_{SD} = 2.5V		0.4	1		0.4	1	mA
*	Shutdown delay	V_{SD} = 2.5V T_j = 25°C		0.2	0.5		0.2	0.5	µs

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
OUTPUT DRIVERS (Each output) (V_C = 20V)									
	Output low level	I_{sink} = 20 mA		0.2	0.4		0.2	0.4	V
		I_{sink} = 100 mA		1	2		1	2	V
	Output high level	I_{source} = 20 mA	18	19		18	19		V
		I_{source} = 100 mA	17	18		17	18		V
	Under-voltage lockout	V_{comp} and V_{ss} = high	6	7	8	6	7	8	V
I_C	Collector leakage	V_C = 35V			200			200	μA
t_r*	Rise time	C_L = 1 nF, T_j = 25°C		100	600		100	600	ns
t_f*	Fall time	C_L = 1 nF, T_j = 25°C		50	300		50	300	ns
TOTAL STANDBY CURRENT									
I_s	Supply current	V_i = 35V		14	20		14	20	mA

* These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

• Tested at f_{osc}= 40 KHz (R_T = 3.6 KΩ, C_T = 0.1 μF, R_D = 0Ω). Approximate oscillator frequency is defined by:

$$f = \frac{1}{C_T (0.7\ R_T + 3\ R_D)}$$

■ DC transconductance (g_M) relates to DC open-loop voltage gain (G_V) according to the following equation: $G_V = g_M R_L$ where R_L is the resistance from pin 9 to ground. The minimum g_M specification is used to calculate minimum G_V when the error amplifier output is loaded.

RECOMMENDED OPERATING CONDITIONS (•)

Input voltage (V_i)	8 to 35 V
Collector supply voltage (V_C)	4.5 to 35 V
Sink/source load current (steady state)	0 to 100 mA
Sink/source load current (peak)	0 to 400 mA
Reference load current	0 to 20 mA
Oscillator frequency range	100 Hz to 400 KHz
Oscillator timing resistor	2 KΩ to 150 KΩ
Oscillator timing capacitor	0.001 μF to 0.1 μF
Dead time resistor range	0 to 500 Ω

(•) Range over which the device is functional and parameter limits are guaranteed.

TEST CIRCUIT

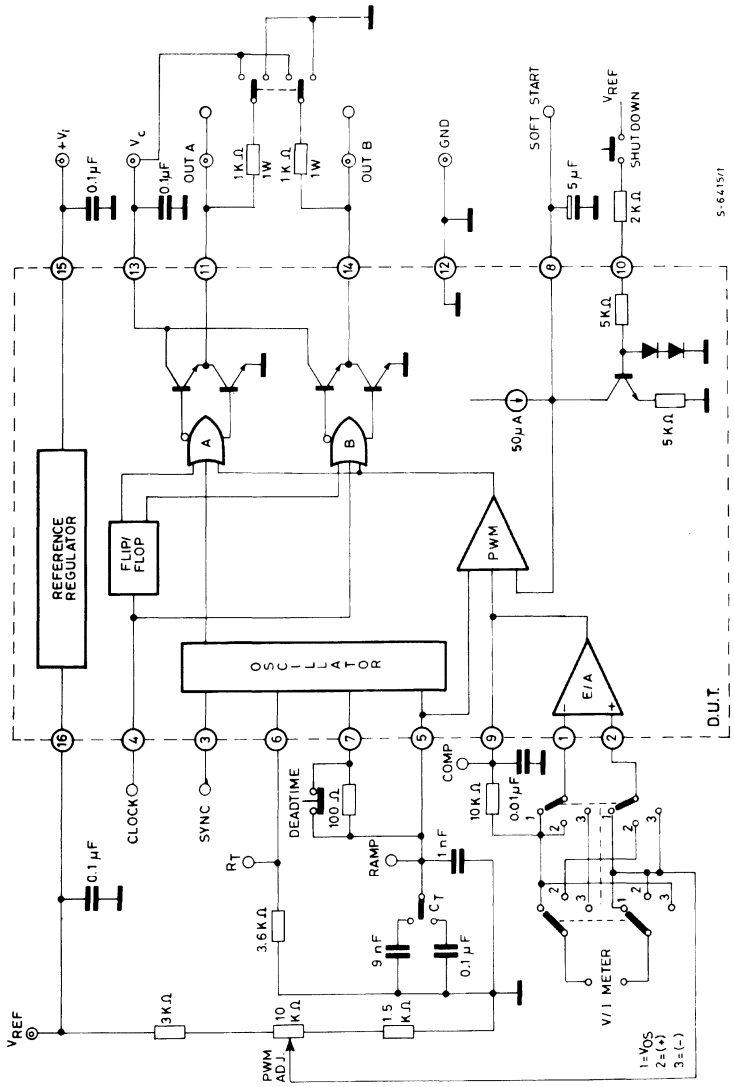


Fig. 1 - Oscillator charge time vs. R_T and C_T

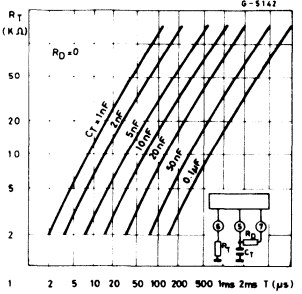


Fig. 2 - Oscillator discharge time vs. R_D and C_T

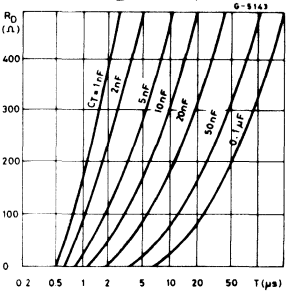


Fig. 3 - SG1525A output saturation characteristics

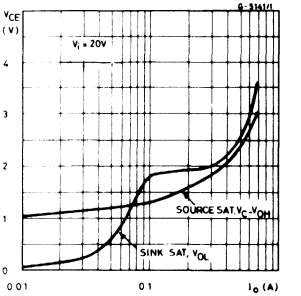


Fig. 4 - Error amplifier voltage gain and phase vs. frequency

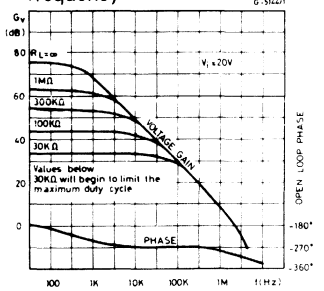
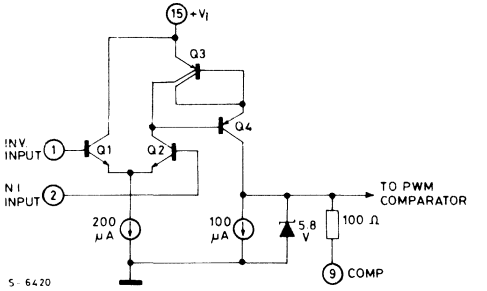


Fig. 5 - SG1525A error amplifier



PRINCIPLES OF OPERATION

SHUTDOWN OPTIONS (See Block Diagram)

Since both the compensation and soft-start terminals (Pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of 100 μA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions: the PWM latch is immediately set providing the fastest turn-off signal to the outputs; and a 150 μA current sink begins to discharge the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn-on upon release.

Pin 10 should not be left floating as noise pickup could conceivably interrupt normal operation.

Fig. 6 - SG1525A oscillator schematic

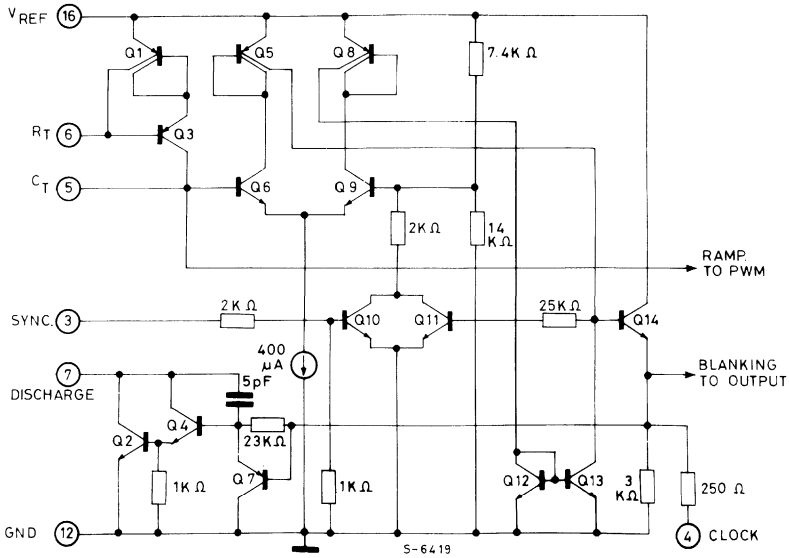


Fig. 7 - SG1525A output circuit (½ circuit shown)

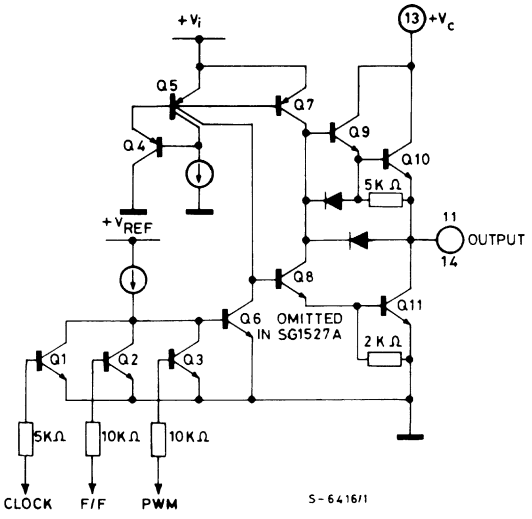
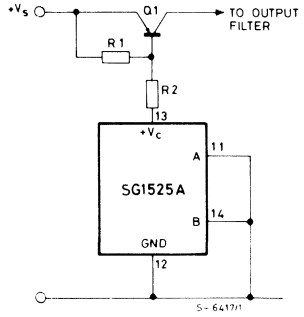
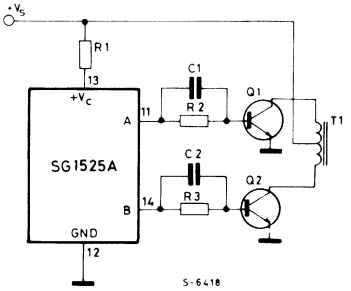


Fig. 7



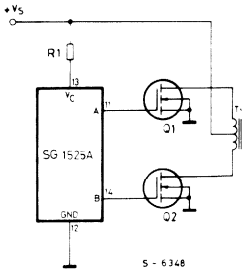
For single-ended supplies, the driver outputs are grounded. The V_c terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.

Fig. 8



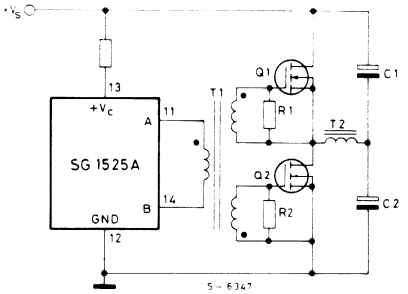
In conventional push-pull bipolar designs, forward base drive is controlled by R_1-R_3. Rapid turn-off times for the power devices are achieved with speed-up capacitors C_1 and C_2.

Fig. 9



The low source impedance of the output drivers provides rapid charging of Power Mos input capacitance while minimizing external components.

Fig. 10



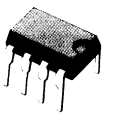
Low power transformers can be driven directly by the SG1525A. Automatic reset occurs during dead time, when both ends of the primary winding are switched to ground.

TDA2320

PREAMPLIFIER FOR INFRARED REMOTE CONTROL SYSTEMS

The TDA2320 is a monolithic integrated circuit in Minidip package specially designed to amplify the IR signal in remot controlled TV or radio sets. It directly interfaces with the digital control circuitry.
The TDA 2320 incorporates a two stages amplifier with excellent sensitivity and high noise immunity. It can work with a single 5V supply voltage and flash or carrier transmission modes as provided for example by the M709/M710C/ MOS transmitter.

The TDA2320 is particularly intended to be used in conjunction with the M104 and M206 + M3870 remote control receivers.



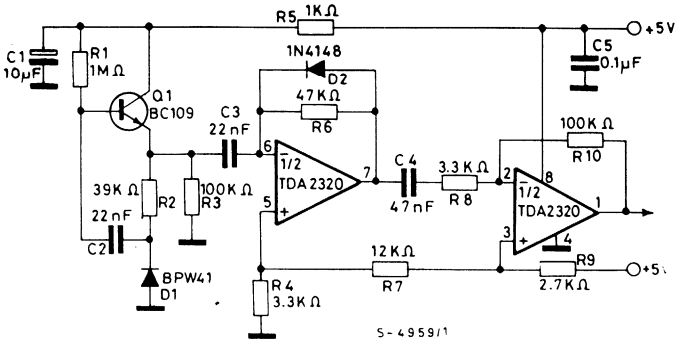
Minidip

ORDERING NUMBER: TDA2320

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	20	V
$T_{stg,\ j}$	Storage and Junction temperature	-40 to 150	°C
P_{tot}	Total power dissipation at $T_{amb} = 70°C$	400	mW

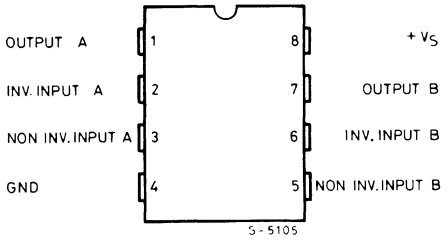
APPLICATION CIRCUIT (Flash mode preamplifier)

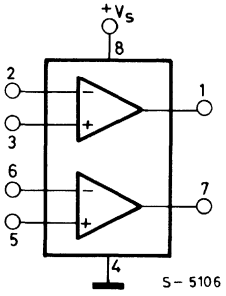


TDA2320

CONNECTION AND BLOCK DIAGRAM

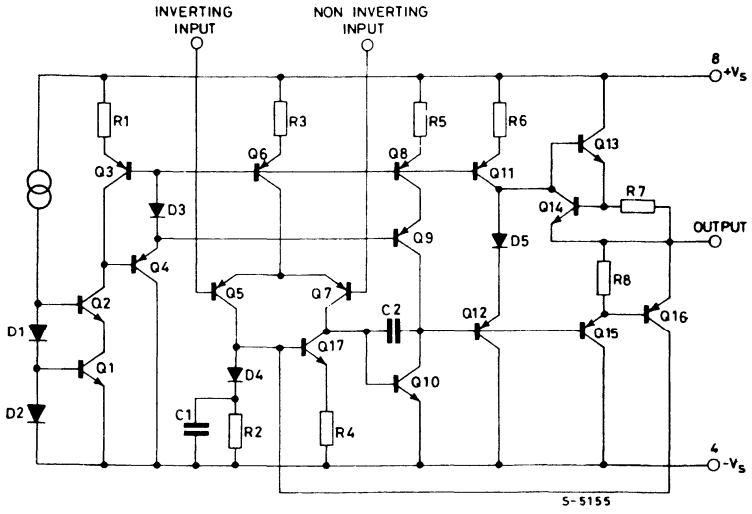
(top view)





SCHEMATIC DIAGRAM

(one section)



THERMAL DATA

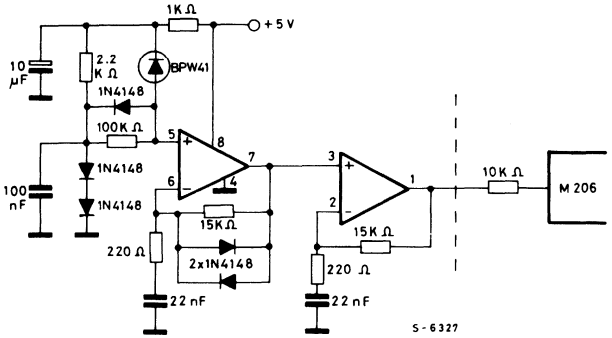
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	200	°C/W

ELECTRICAL CHARACTERISTICS (V_s= 5V, T_{amb}= 25°C, single amplifier, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		4		20	V
I_s	Total supply current	V_s = 20V		0.8	2	mA
I_b	Input bias current			100	500	nA
V_{os}	Input offset voltage	R_g < 10 KΩ		0.5		mV
I_{os}	Input offset current			15		nA
G_v	Open loop voltage gain	f = 1 KHz	64	70		dB
		f = 100 KHz		30		dB
B	Gain bandwidth product	f = 40 KHz	1.5	3		MHz
SR	Slew rate	R_L= 2 KΩ		1.5		V/μs
e_N	Total input noise voltage	f = 40 KHz Rg= 10KΩ		20		$nV\sqrt{Hz}$
V_o.	DC output voltage swing			2.5		Vpp
SVR	Supply voltage rejection	f = 100 Hz		80		dB

APPLICATION INFORMATION

Fig. 1 - Application circuit for carrier transmission mode



APPLICATION INFORMATION (continued)

Fig. 2 - Flash mode preamplifier

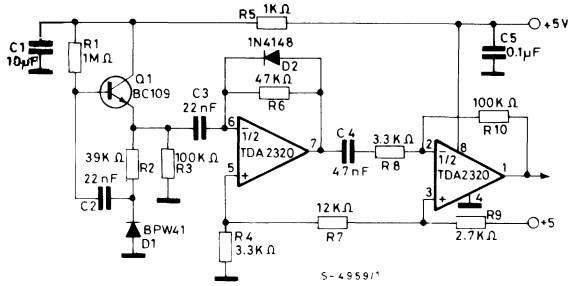


Fig. 3 - P.C. and components layout of the circuit of fig. 2 (1 : 1 scale)

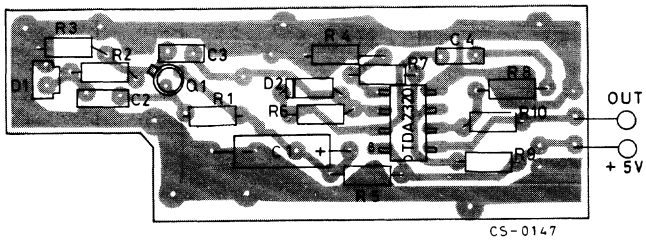


Fig. 4 - IR transmitter using M709 or M710

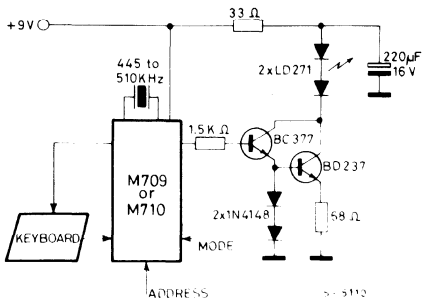
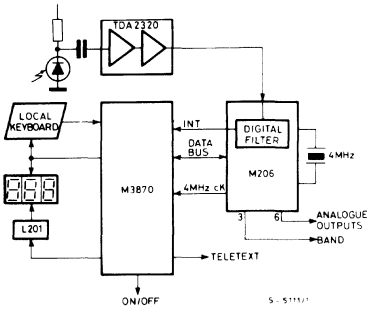
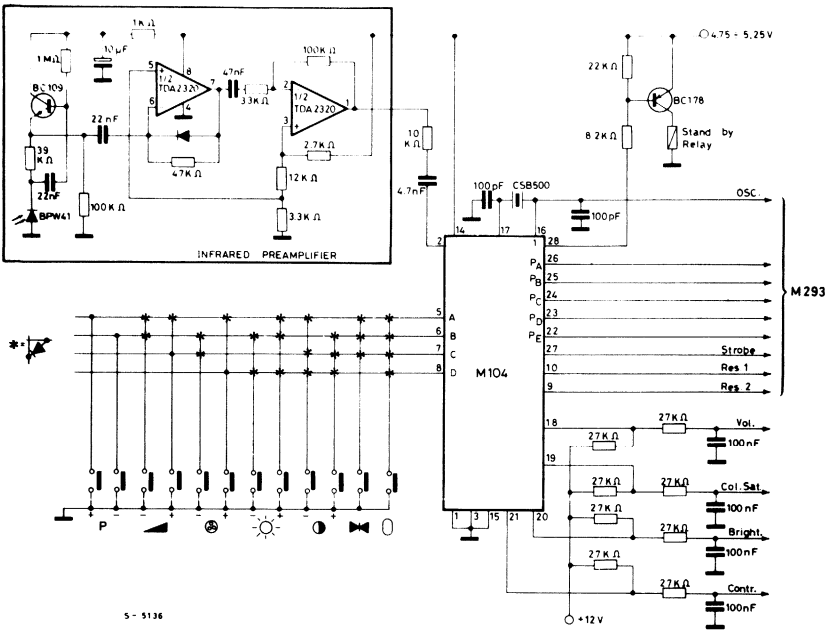


Fig. 5 - MMC II - PLL TV Frequency synthesizer



APPLICATION INFORMATION (continued)

Fig. 6 - IR Preamplifier and Remote Control receiver for 32 channel voltage synthesizer (EPM - M293)



TDA2320A

MINIDIP STEREO PREAMPLIFIER

- WIDE SUPPLY VOLTAGE RANGE (3 TO 36V)
- SINGLE OR SPLIT SUPPLY OPERATION
- VERY LOW CURRENT CONSUMPTION (0.8mA)
- VERY LOW DISTORTION
- NO POP-NOISE
- SHORT CIRCUIT PROTECTION

The TDA2320A is a stereo class A preamplifier intended for application in portable cassette players and high quality audio systems.

The TDA2320A is a monolithic integrated circuit a 8 lead minidip.

Minidip

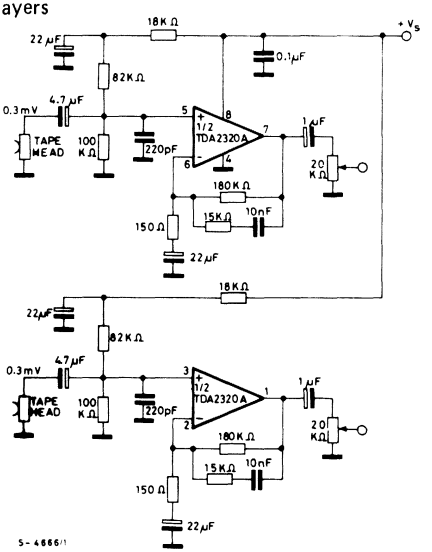
ORDERING NUMBER: TDA 2320A

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	36	V
P_{tot}	Total power dissipation at $T_{amb} = 70°C$	400	mW
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

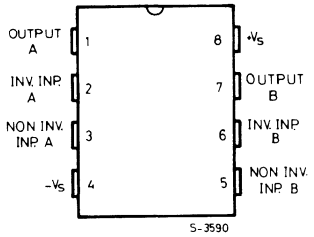
TYPICAL APPLICATION:

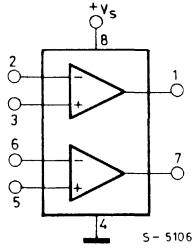
Stereo preamplifier for cassette players



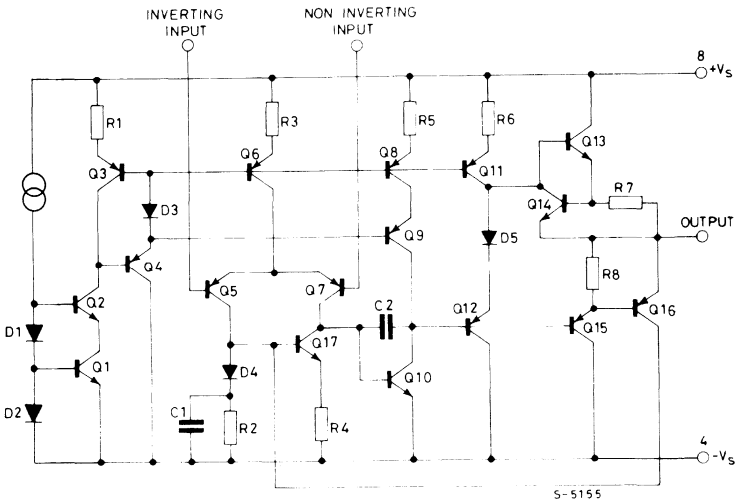
TDA2320A

CONNECTION AND BLOCK DIAGRAM
(top view)



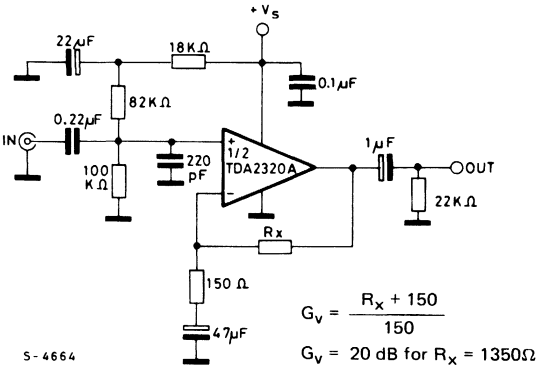


SCHEMATIC DIAGRAM
(one section)



TEST CIRCUITS

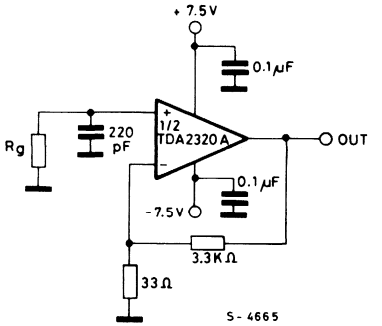
Fig. 1



$$G_v = \frac{R_x + 150}{150}$$

G_v = 20 dB for R_x = 1350Ω

Fig. 2



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	200	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuits, V_s = 15V, T_{amb} = 25°C, unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage (*)			3		36	V
I_s	Supply current (*)				0.8	2	mA
I_b	Input bias current				150	500	nA
V_{os}	Input offset voltage	$R_g < 10$ KΩ			1	5	mV
I_{os}	Input offset current				10	50	nA
G_v	Open loop voltage gain	V_s = 15V	f = 333 Hz		80		dB
			f = 1 KHz		70		
			f = 10 KHz		50		
		V_s = 4.5V	f = 1 KHz		70		
V_o	Output voltage swing (*)	f = 1 KHz	V_s= 15V		13		Vpp
		R_L= 600Ω	V_s= 4.5V		2.5		
B	Gain-bandwidth product	f = 20 KHz		1.5	2.5		MHz
BW	Power bandwidth (*)	V_o= 5 Vpp d = 1%		40	70		KHz
SR	Slew rate (*)			1	1.6		V/μS
d	Distortion (*)	V_o= 2V	f = 1 KHz		0.03		%
		G_v= 20 dB	f = 10 KHz		0.08		
e_N	Total input noise voltage (**)	Curve A	R_g= 50Ω		1		μV
			R_g= 600Ω		1.1	1.4	
			R_g= 5 KΩ		1.5		
		B = 22 Hz to 22 KHz	R_g= 50Ω		1.3		μV
			R_g= 600Ω		1.5		
			R_g= 5 KΩ		2		
		f = 1 KHz	R_g= 600Ω		9		$nV/\sqrt{Hz}$
Cs	Channel separation (**)		f = 1 KHz		100		dB
SVR	Supply voltage (**) rejection		f = 100 Hz		80		dB

(*) Test circuit of fig. 1.
(**) Test circuit of fig. 2.

Fig. 3 - Supply current vs. supply voltage

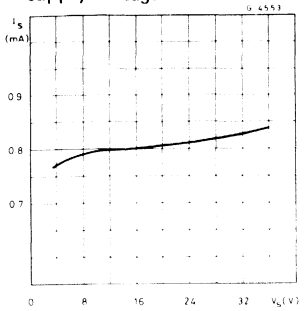


Fig. 4 - Supply current vs. ambient temperature

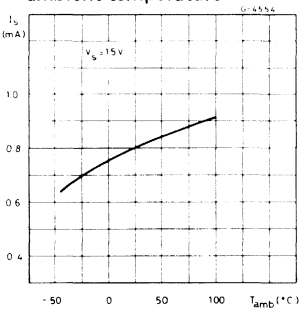


Fig. 5 - Output voltage swing vs. load resistance

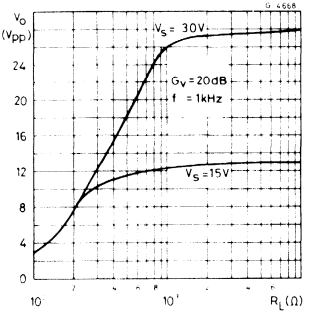


Fig. 6 - Power bandwidth

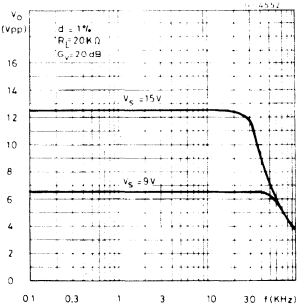


Fig. 7 - Total harmonic distortion vs. output voltage

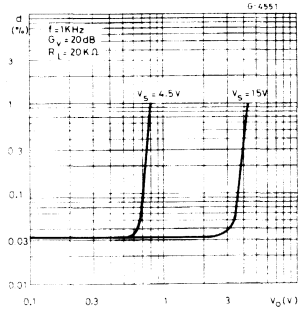


Fig. 8 - Total input noise vs. source resistance

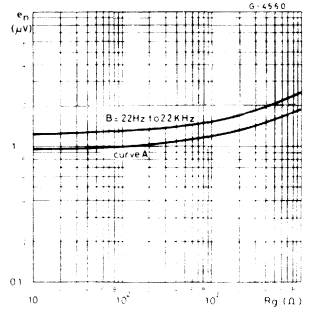


Fig. 9 - Noise density vs. frequency

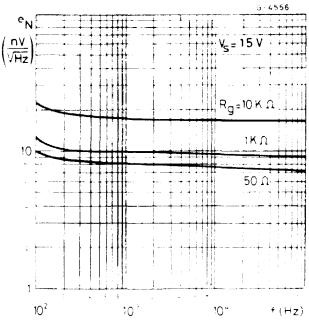


Fig. 10 - RIAA preamplifier response (circuit of fig. 12)

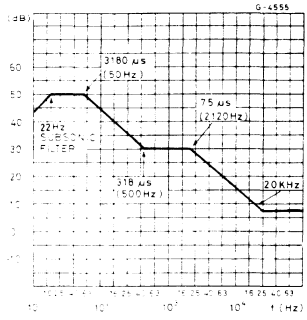
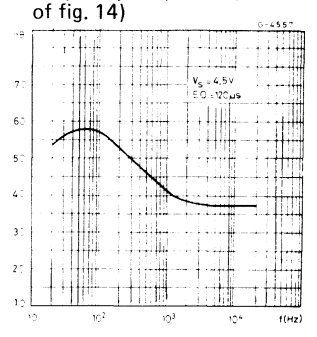


Fig. 11 - Tape preamplifier frequency response (circuit of fig. 14)



APPLICATION INFORMATION

Fig. 12 - Stereo RIAA preamplifier

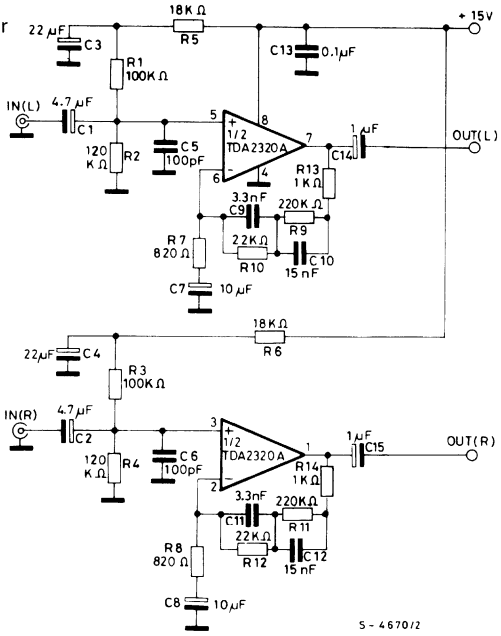
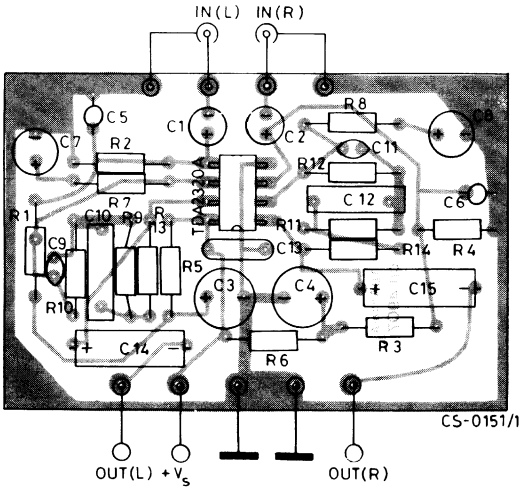


Fig. 13 - P.C. board and components layout of the circuit of fig. 12



APPLICATION INFORMATION (continued)

Fig. 14 - Stereo preamplifier for Walkman cassette players

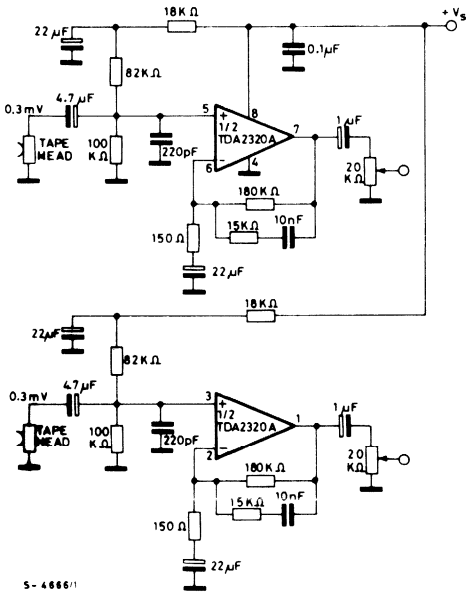


Fig. 15 - Second order 2 KHz Butterworth crossover filter for Hi-Fi active boxes

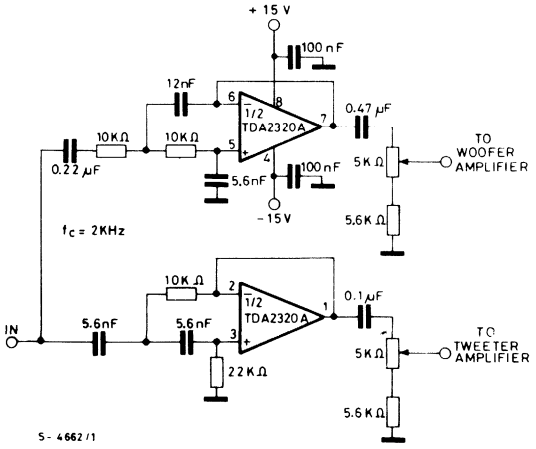
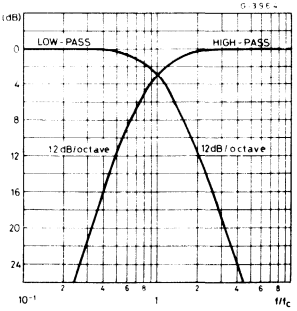


Fig. 16 - Frequency response (circuit of fig. 15)



APPLICATION INFORMATION (continued)

Fig. 17 - Third order 2.8 KHz Bessel crossover filter for Hi-Fi active boxes

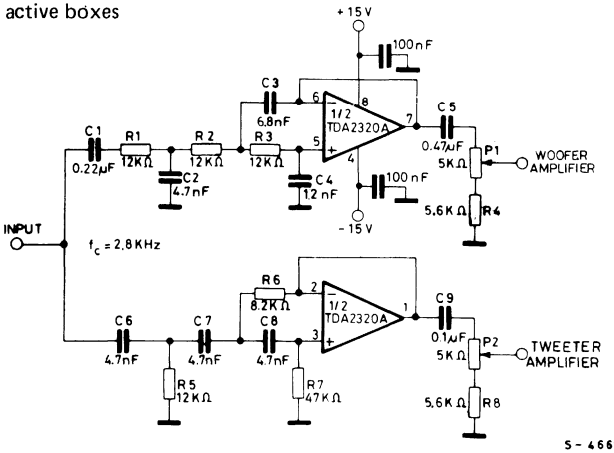


Fig. 18 - Frequency response (circuit of fig. 17)

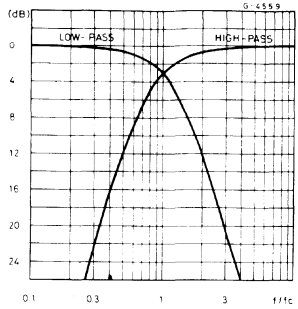


Fig. 19 - 200 Hz to 2 KHz Active Bandpass Filter for midrange speakers

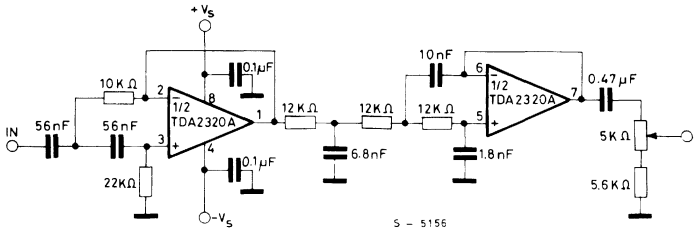
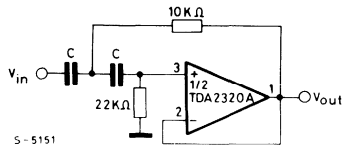
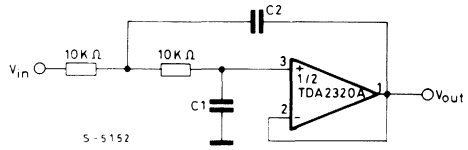


Fig. 20 - Subsonic filter



f_c (Hz)	C (µF)
15	0.68
22	0.47
30	0.33
55	0.22
100	0.1

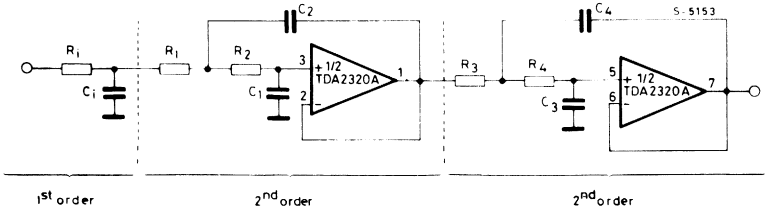
Fig. 21 - High-cut filter



f_c (KHz)	C1 (nF)	C2 (nF)
3	3.9	6.8
5	2.2	4.7
10	1.2	2.2
15	0.68	1.5

APPLICATION INFORMATION (continued)

Fig. 22 - Fifth order 3.4 KHz low-pass Butterworth filter



For f_c = 3.4 KHz and R_i = R1 = R2 = R3 = R4 = 10 KΩ, we obtain:

$C1 = 1.354 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 6.33$ nF

$C1 = 0.421 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.97$ nF

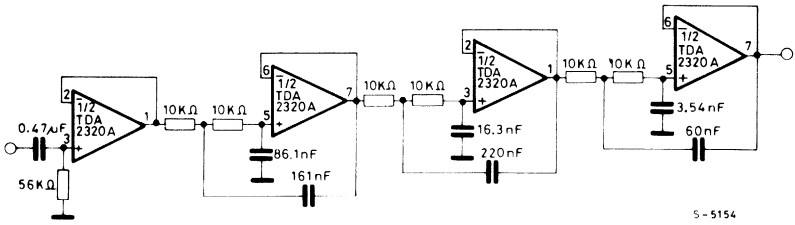
$C2 = 1.753 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 8.20$ nF

$C3 = 0.309 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.45$ nF

$C4 = 3.325 \cdot \frac{1}{R} \cdot \frac{1}{2,\pi f_c} = 15.14$ nF

The attenuation of the filter is 30 dB at 6.8 KHz and better than 60 dB at 15 KHz.

Fig. 23 - Sixth-pole 355 Hz low-pass filter (Chebychev type)



This is a 6- pole Chebychev type with ± 0.25 dB ripple in the passband. A decoupling stage is used to avoid the influence of the input impedance on the filter's characteristics. The attenuation is about 55 dB at 710 Hz and reaches 80dB at 1065 Hz. The in band attenuation is limited in practice to the ± 0.25 dB ripple and does not exceed 1/2 dB at 0.9 fc.

APPLICATION INFORMATION (continued)

Fig. 24 - Three band tone control

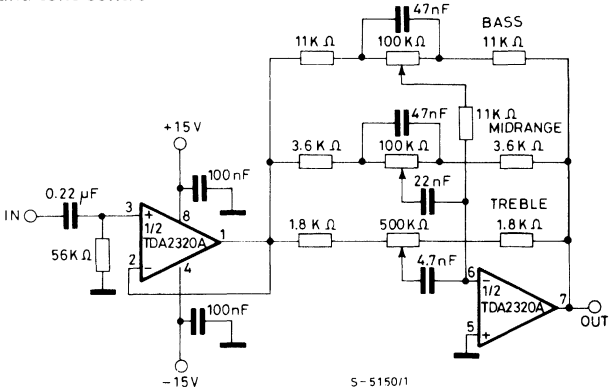
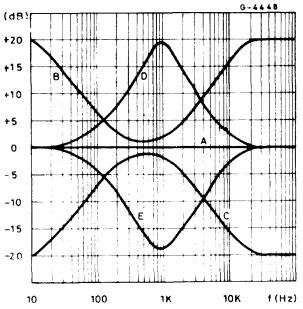


Fig. 25 - Frequency response of the circuit of fig. 24.



A : all controls flat
B : bass & treble boost, mid flat
C : bass & treble cut, mid flat
D : mid boost, bass & treble flat
E : mid cut, bass & treble flat

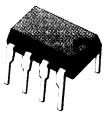
TL072

LOW NOISE JFET-INPUT QUAD OPERATIONAL AMPLIFIERS

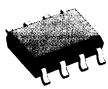
- LOW-NOISE
- LOW INPUT BIAS AND OFFSET CURRENTS
- HIGH INPUT IMPEDANCE . . . JFET-INPUT STAGE
- LOW POWER CONSUMPTION
- WIDE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- OUTPUT SHORT-CIRCUIT PROTECTION
- INTERNAL FREQUENCY COMPENSATION
- LATCH-UP-FREE OPERATION
- HIGH SLEW-RATE . . . 13V/μs TYP.

The TL072 JFET-input operational amplifiers are designed to offer low-noise high slew-rate, low input bias and offset current, and low offset voltage temperture coefficient. Each JFET-input operational amplifier incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit.

Devices with an "I" suffix are characterized for operation from -25°C to 85°C, and those with a "C" suffix are characterized for operation from 0°C to 70°C.

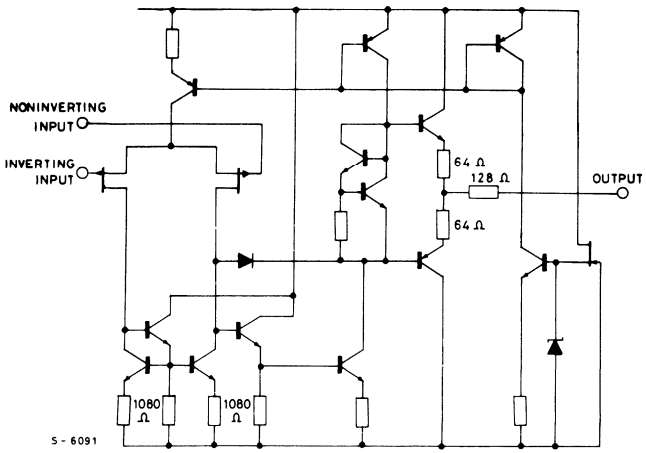


Minidip
(Plastic and Ceramic)



SO-8

SCHEMATIC DIAGRAM
(one section)



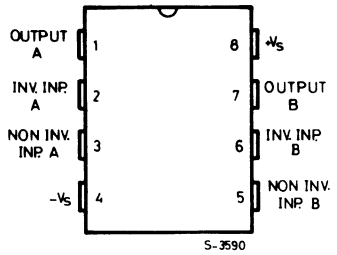
TL072

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 18	V
V_{is}	Differential input voltage	± 30	V
V_i	Input voltage	± 15	V
T_{op}	Operating temperature (TL072I)	-25 to 85	°C
	(TL072C)	0 to 70	°C
T_j	Junction temperature	150	°C
T_{stg}	Storage temperature	-55 to 150	°C

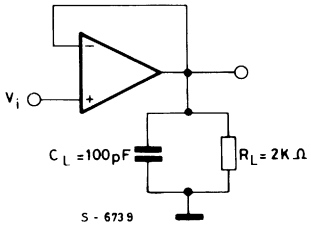
CONNECTION DIAGRAM AND ORDERING NUMBERS

(Top view)

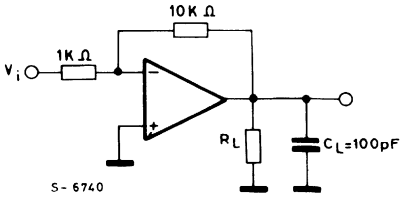


0 to 70°C	-25 + 85°C	Package
TL072CJG TL072ACJG TL072BCJG	TL072IJG — —	Ceramic Minidip
TL072CP TL072ACP TL0BCP	TL072IP — —	Plastic Minidip
TL072CD	TL072ID	SO-8

TEST CIRCUITS



Unity gain amplifier



Gain of 10 inverting amplifier

THERMAL DATA

			Plastic Minidip	Ceramic Minidip	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	120°C/W	150°C/W	200°C/W

ELECTRICAL CHARACTERISTICS (V_s = 15V, T_{amb} = 25°C, otherwise specified)

Parameter		Test conditions		"I"			"C"			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OS}	Input offset voltage	R_s = 50Ω	TL072		3	6		3	10	mV
			TL072A					3	6	
			TL072B					2	3	
		R_s = 50Ω, T_{amb} = full range	TL072			9			13	
			TL072A						7.5	
			TL072B						5	
$\frac{\Delta V_{OS}}{\Delta T}$	Input offset voltage drift	R_s = 500Ω, T_{amb} = full range			10			10		µV/°C
I_{OS}	Input offset current		TL072		5	50		5	50	pA
			TL072A					5	50	
			TL072B					5	50	
		T_{amb} = full range	TL072			10			2	nA
			TL072A						2	
			TL072B						2	
I_b	Input bias current		TL072		30	200		30	200	pA
			TL072A					30	200	
			TL072B					30	200	
		T_{amb} = full range	TL072			20			7	nA
			TL072A						7	
			TL072B						7	
V_{CM}	Common mode input voltage range		TL072	± 11	± 12		± 10	± 11		V
			TL072A				± 11	± 12		
			TL072B				± 11	± 12		
V_{OPP}	Large signal voltage swing		R_L = 10KΩ	24	27		24	27		V
		T_{amb} = full range	$R_L \geq$ 10KΩ	24			24			
			$R_L \geq$ 2KΩ	20	24		20	24		
G_V	Large signal voltage gain	$R_L \geq$ 2KΩ, V_o = ± 10V	TL072	50	200		25	200		V/mV
			TL072A				50	200		
			TL072B				50	200		
		$R_L \geq$ 2KΩ, V_o = ± 10V, T_{amb} = full range	TL072	25			15			
			TL072A				25			
			TL072B				25			
B	Unity gain bandwidth				3			3		MHz
R_i	Input resistance				10^{12}			10^{12}		Ω
CMR	Common mode rejection	$R_s \geq$ 10KΩ	TL072	80	86		70	76		dB
			TL072A				80	86		
			TL072B							
SVR	Supply voltage rejection	$R_s \geq$ 10KΩ	TL072	80	86		70	76		dB
			TL072A				80	86		
			TL072B				80	86		
I_S	Supply current	R_L = ∞			2.8	5		2.8	5	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions		"I"			"C"			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Cs	Channel separation	G_V = 100			120			120		dB
SR	Slew-rate at	V_i = 10V C_L = 100pF	R_L = 2KΩ		13			13		V/μs
t_r	Rise time	V_i = 20mV	R_L = 2KΩ		0.1			0.1		μs
	Overshot factor	C_L = 100pF			10			10		%
e_N	Total input noise voltage	R_S = 100Ω	F = 1KHz		18			18		$\frac{nV}{\sqrt{Hz}}$
			f = 10Hz to 10KHz		4			4		μV
I_N	Input noise current	f = 1KHz			0.01			0.01		$\frac{pA}{\sqrt{Hz}}$
d	Total harmonic distortion	V_O = 10V_{rms} R_S < 1KΩ R_L > 2KΩ	f = 1KHz		0.01			0.01		%

Fig. 1 – Maximum peak to peak output voltage vs. frequency.

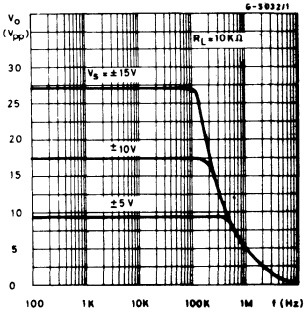


Fig. 2 – Maximum peak to peak output voltage vs. frequency

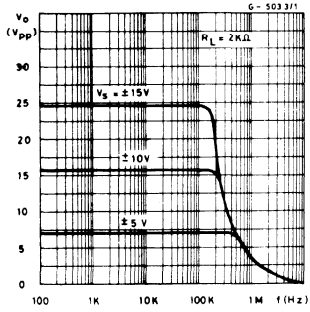


Fig. 3 – Maximum peak to peak output voltage vs. load resistance

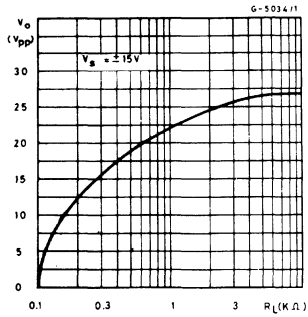


Fig. 4 – Large signal voltage gain and phase shift vs. frequency

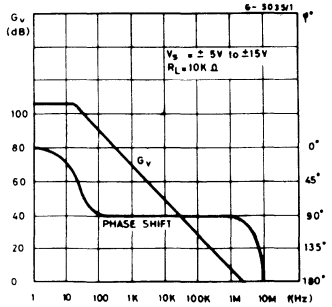


Fig. 5 Supply current vs. supply voltage

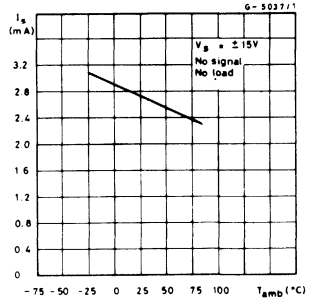


Fig. 6 – Supply current vs. supply voltage

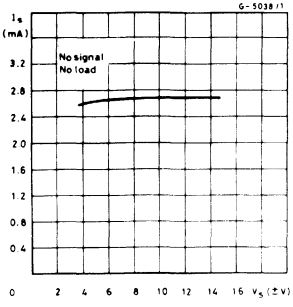


Fig. 7 – Input bias current vs. temperature

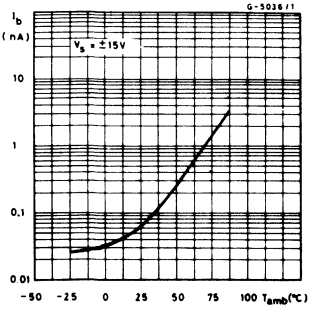


Fig. 8 – Voltage follower large signal pulse response

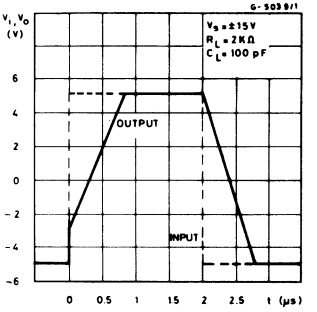


Fig. 9 – Output voltage vs. elapsed time

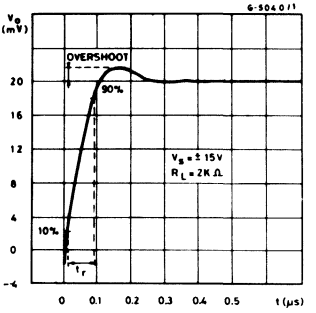


Fig. 10 – Equivalent input noise voltage vs. frequency

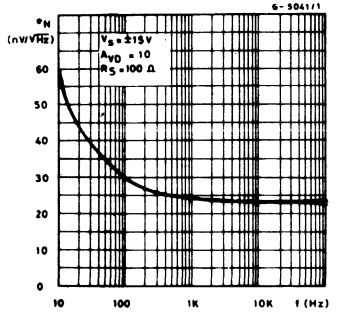


Fig. 11 – Total harmonic distortion vs. frequency

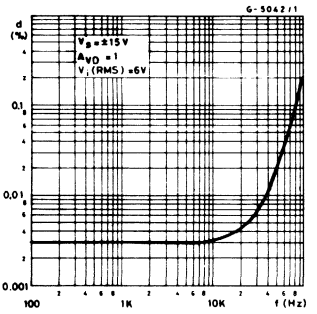
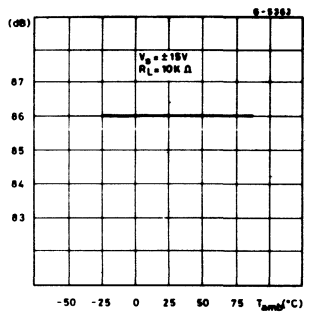
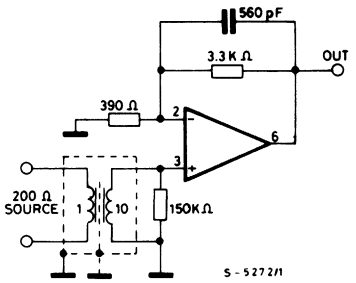


Fig. 12 Common mode rejection vs. temperature



APPLICATION INFORMATION

Fig. 13 – Low-Noise High Slew-Rate mike preamplifier (G_v = 40 dB)



APPLICATION INFORMATION (continued)

Fig. 14 – Second order high Q band pass filter (f_o = 100KHz, Q = 30, gain = 4)

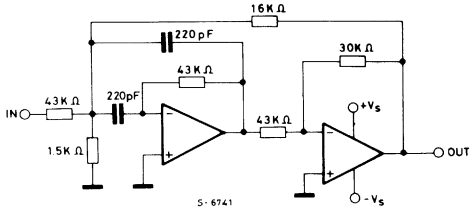
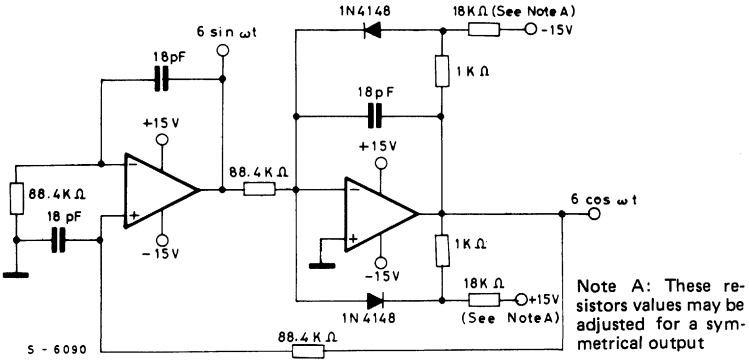


Fig. 15 – 100KHz quadrature oscillator



Note A: These resistors values may be adjusted for a symmetrical output

Fig 16 – 20Hz to 200Hz variable High-pass filter (G_v = 3dB)

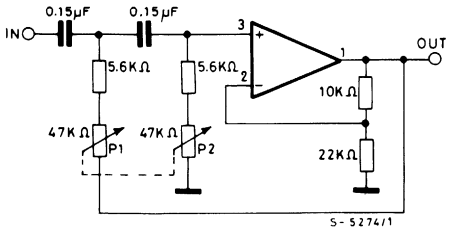
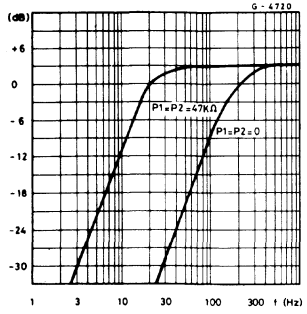


Fig. 17 - Frequency response of the high-pass filter of fig. 17



APPLICATION INFORMATION (continued)

Fig. 18 – Unity-gain absolute-value circuit

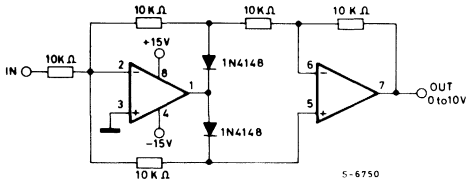


Fig. 19 – Single supply sample and hold

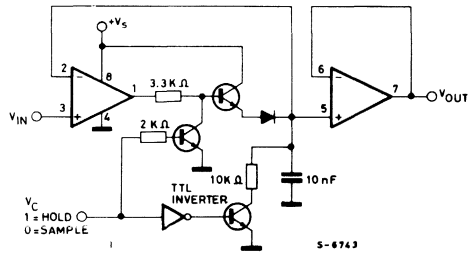
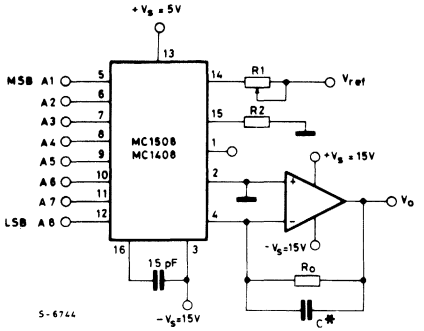


Fig. 20 – Output current to voltage transformation for a DA converter



(*) The value of C may be selected to minimize overshoot and ringing (C ≈ 68 pF).

Settling time to within 1/2 LSB (± 19.5 mV) is approximately 4.0 μs from the time all bits are switched.

Theoretical V_o :

$$V_o = \frac{V_{ref}}{R1}(R_o)\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

Adjust V_{ref}, R1 or R_o so that V_o with all digital inputs at high level is equal to 9.961 volts.

$V_{ref} = 2.0\ V_{dc}$
$R1 = R2 \approx 1.0\ k\Omega$
$R_o = 5.0\ k\Omega$

$$V_o = \frac{2\ V}{1\ k}(5\ k)\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256}\right]$$

$$= 10V\left[\frac{255}{256}\right] = 9.961V$$

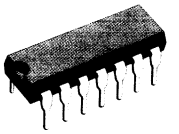
TL074

LOW NOISE JFET-INPUT QUAD OPERATIONAL AMPLIFIERS

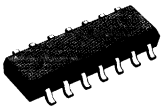
- LOW-NOISE
- LOW INPUT BIAS AND OFFSET CURRENTS
- HIGH INPUT IMPEDANCE . . . JFET-INPUT STAGE
- LOW POWER CONSUMPTION
- WIDE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- OUTPUT SHORT-CIRCUIT PROTECTION
- INTERNAL FREQUENCY COMPENSATION
- LATCH-UP-FREE OPERATION
- HIGH SLEW-RATE . . . 13V/μs TYP.

The TL074 JFET-input operational amplifiers are designed to offer low-noise high slew-rate, low input bias and offset current, and low offset voltage temperature coefficient. Each JFET-input operational amplifier incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit.

Devices with an "I" suffix are characterized for operation from -25°C to 85°C, and those with a "C" suffix are characterized for operation from 0°C to 70°C.

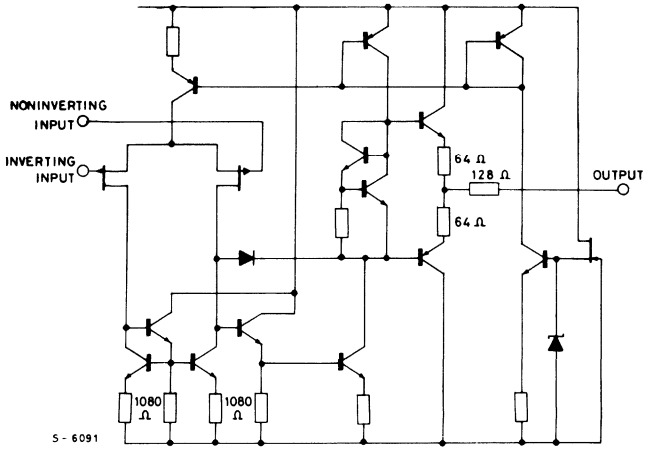


DIP-14
(Plastic and Ceramic)



SO-14

SCHEMATIC DIAGRAM
(one section)



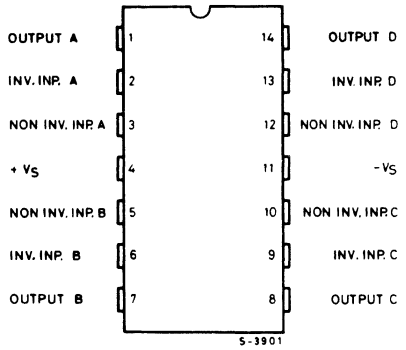
TL074

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 18	V
V_{is}	Differential input voltage	± 30	V
V_i	Input voltage	± 15	V
T_{op}	Operating temperature (TL074I)	-25 to 85	°C
	(TL074C)	0 to 70	°C
T_j	Junction temperature	150	°C
T_{stg}	Storage temperature	-55 to 150	°C

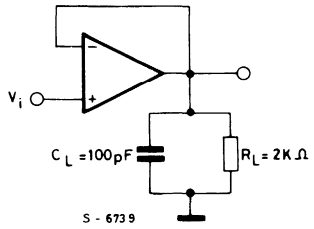
CONNECTION DIAGRAM AND ORDERING NUMBERS

(Top view)

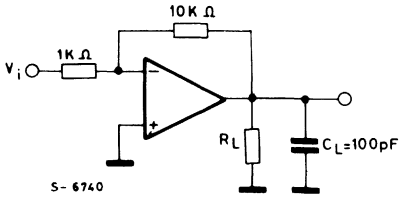


0 to 70°C	-25 + 85°C	Package
TL074CJ TL074ACJ TL074BCJ	TL074IJ – –	Ceramic DIP-14
TL074CN TL074ACN TL074BCN	TL074IN – –	Plastic DIP-14
TL074CD	TL074ID	SO-14

TEST CIRCUITS



Unity gain amplifier



Gain of 10 inverting amplifier

THERMAL DATA

			Ceramic DIP-14	SO-14	Plastic DIP-14
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	150°C/W	165°C/W	200°C/W

ELECTRICAL CHARACTERISTICS (V_s = 15V, T_{amb} = 25°C, otherwise specified)

Parameter		Test conditions		"I" Min.	"I" Typ.	"I" Max.	"C" Min.	"C" Typ.	"C" Max.	Unit
V_{OS}	Input offset voltage	R_s = 50Ω	TL074		3	6		3	10	mV
			TL074A					3	6	
			TL074B					2	3	
		R_s = 50Ω, T_{amb} = full range	TL074			9			13	
			TL074A						7.5	
			TL074B						5	
$\frac{\Delta V_{OS}}{\Delta T}$	Input offset voltage drift	R_s = 50Ω, T_{amb} = full range			10			10		µV/°C
I_{OS}	Input offset current		TL074		5	50		5	50	pA
			TL074A					5	50	
			TL074B					5	50	
		T_{amb} = full range	TL074			10			2	nA
			TL074A						2	
			TL074B						2	
I_b	Input bias current		TL074		30	200		30	200	pA
			TL074A					30	200	
			TL074B					30	200	
		T_{amb} = full range	TL074			20			7	nA
			TL074A						7	
			TL074B						7	
V_{CM}	Common mode input voltage range		TL074	± 11	± 12		± 10	± 11		V
			TL074A				± 11	± 12		
			TL074B				± 11	± 12		
V_{OPP}	Large signal voltage swing	T_{amb} = full range	R_L = 10KΩ	24	27		24	27		V
			$R_L \geq$ 10KΩ	24			24			
			$R_L \geq$ 2KΩ	20	24		20	24		
G_V	Large signal voltage gain	$R_L \geq$ 2KΩ, V_o = ± 10V	TL074	50	200		25	200		V/mV
			TL074A				50	200		
			TL074B				50	200		
		$R_L \geq$ 2KΩ, V_o = ± 10V, T_{amb} = full range	TL074	25			15			V/mV
			TL074A				25			
			TL074B				25			
B	Unity gain bandwidth				3			3		MHz
R_I	Input resistance				10^{12}			10^{12}		Ω
CMR	Common mode rejection	$R_s \geq$ 10KΩ	TL074	80	86		70	76		dB
			TL074A				80	86		
			TL074B				80	86		
SVR	Supply voltage rejection	$R_s \geq$ 10KΩ	TL074	80	86		70	76		dB
			TL074A				80	86		
			TL074B				80	86		
I_S	Supply current	R_L = ∞			5.6	10		5.6	10	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions		"I"			"C"			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Cs	Channel separation	G_V = 100			120			120		dB
SR	Slew-rate at unity gain	V_i = 10V, R_L = 2KΩ, C_L = 100pF			13			13		V/μs
t_r	Rise time	V_i = 20mV, R_L = 2KΩ, C_L = 100pF			0.1			0.1		μs
	Overshot factor				10			10		%
e_N	Total input noise voltage	R_S = 100Ω	f = 1KHz		18			18		$\frac{nV}{\sqrt{Hz}}$
			f = 10Hz to 10KHz		4			4		μV
I_N	Input noise current	f = 1KHz			0.01			0.01		$\frac{pA}{\sqrt{Hz}}$
d	Total harmonic distortion	V_O = 10Vrms, R_S < 1KΩ, R_L > 2KΩ	f = 1KHz		0.01			0.01		%

Fig. 1 – Maximum peak to peak output voltage vs. frequency.

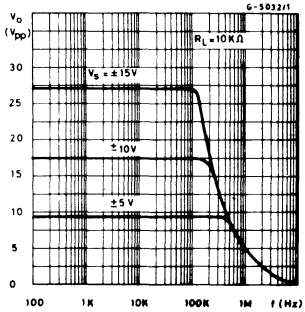


Fig. 2 – Maximum peak to peak output voltage vs. frequency

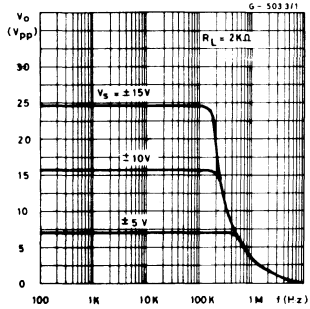


Fig. 3 – Maximum peak to peak output voltage vs. load resistance

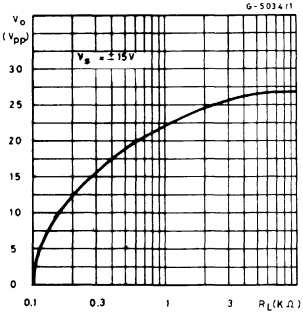


Fig. 4 – Large signal voltage gain and phase shift vs. frequency

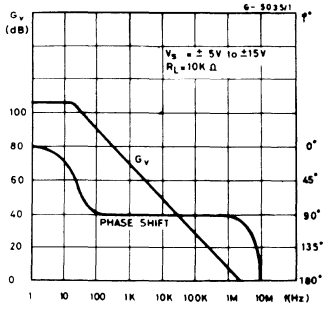


Fig. 5 Supply current vs. temperature

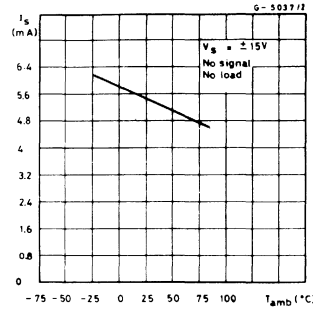


Fig. 6 – Supply current vs. supply voltage

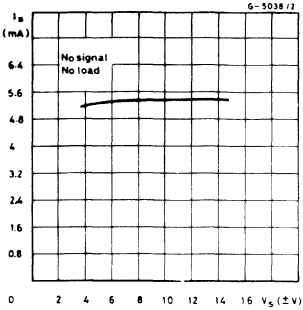


Fig. 7 – Input bias current vs. temperature

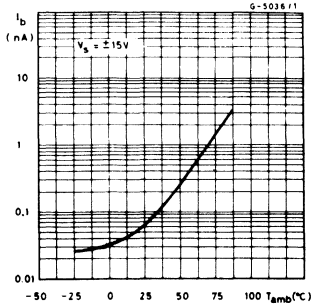


Fig. 8 – Voltage follower large signal pulse response

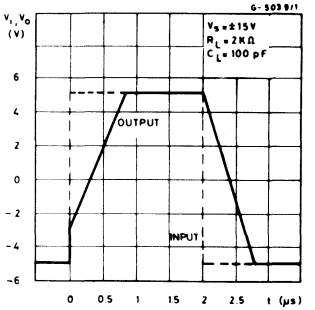


Fig. 9 – Output voltage vs. elapsed time

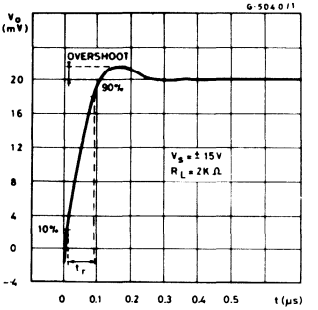


Fig. 10 – Equivalent input noise voltage vs. frequency

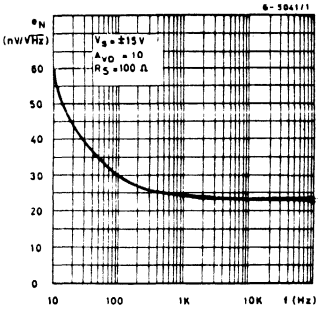


Fig. 11 – Total harmonic distortion vs. frequency

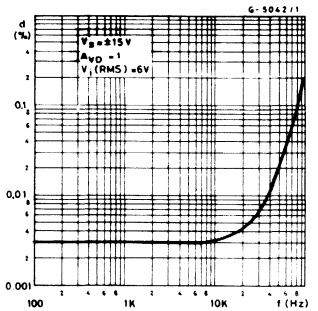
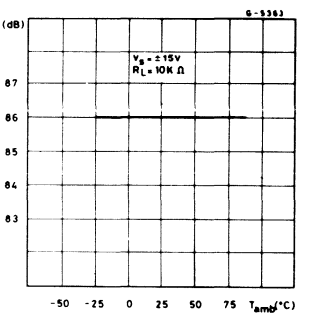
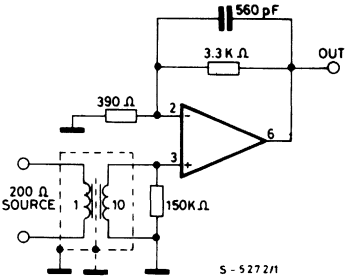


Fig. 12 Common mode rejection vs. temperature



APPLICATION INFORMATION

Fig. 13 - Low-Noise high Slew-Rate mike preamplifier (G_V = 40dB)



APPLICATION INFORMATION (continued)

Fig. 14 – Second order high Q band pass filter (f_o = 100KHz, Q = 30, gain = 4)

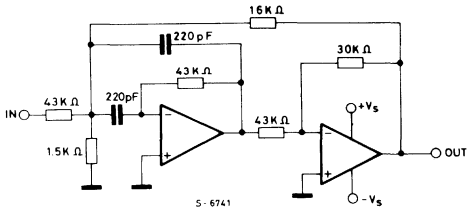
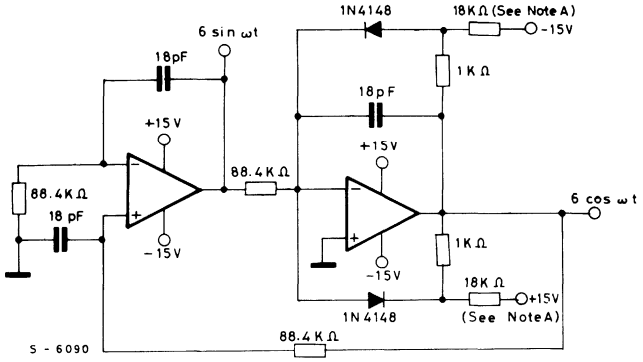


Fig. 15 – 100KHz quadrature oscillator



Note A: these resistor values may be adjusted for a simmetrical output

Fig 16 – 20Hz to 200Hz variable High-pass filter (G_v = 3dB)

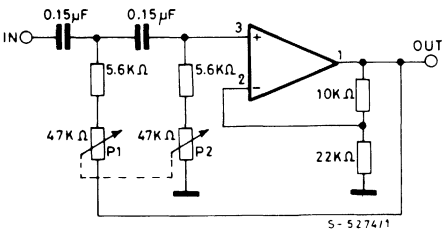
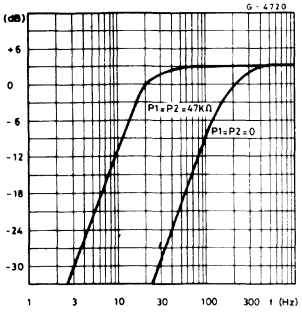


Fig. 17 – Frequency response fo the high-pass filter of fig. 16



APPLICATION INFORMATION (continued)

Fig. 18 – Unity-gain absolute-value circuit

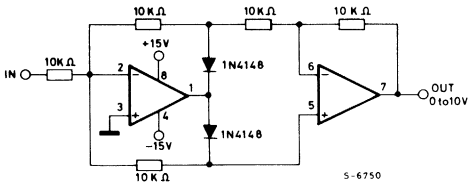


Fig. 19 – Single supply sample and hold

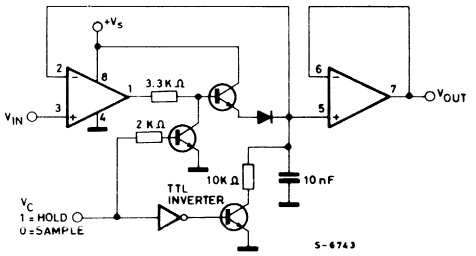
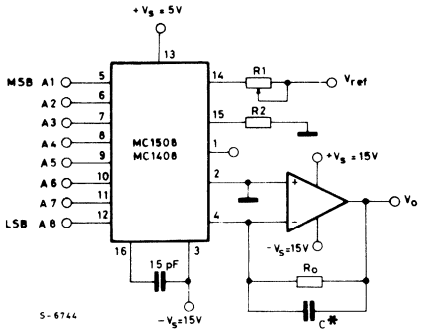


Fig. 20 – Output current to voltage transformation for a DA converter



(*) The value of C may be selected to minimize overshoot and ringing (C ≈ 68 pF).

Settling time to within 1/2 LSB (± 19.5 mV) is approximately 4.0 μs from the time all bits are switched.

Theoretical V_o :

$$V_o = \frac{V_{ref}}{R1}(R_o)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$$

Adjust V_{ref}, R1 or R_o so that V_o with all digital inputs at high level is equal to 9.961 volts.

$V_{ref} = 2.0\ V_{dc}$
$R1 = R2 \approx 1.0\ k\Omega$
$R_o = 5.0\ k\Omega$

$$V_o = \frac{2\ V}{1\ k}(5\ k)\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right]$$

$$= 10V\left[\frac{255}{256}\right] = 9.961V$$

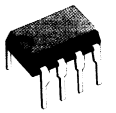
TL082

JFET-INPUT DUAL OPERATIONAL AMPLIFIERS

- HIGH SLEW-RATE ... 13 V/μs TYP.
- LOW POWER CONSUMPTION
- WIDE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW INPUT BIAS AND OFFSET CURRENTS
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE ... JFET-INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH-UP-FREE OPERATION

The TL082 JFET-input operational amplifiers are designed to offer high slew-rate, low input bias and offset current, and low offset voltage temperature coefficient. Each JFET-input operational amplifier incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit.

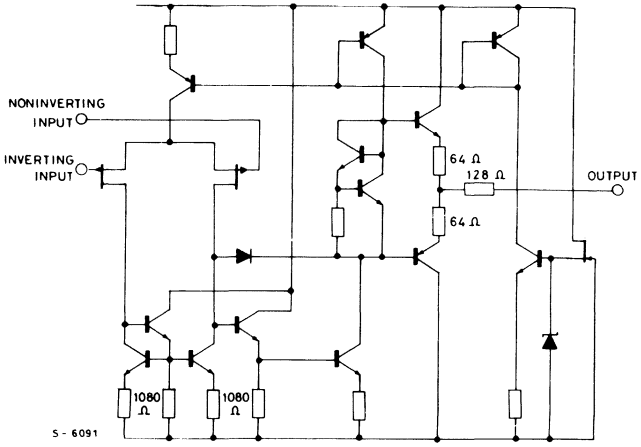
Devices with an "I" suffix are characterized for operation from -25°C to 85°C, and those with a "C" suffix are characterized for operation from 0°C to 70°C. The "M" devices are characterized for operation from -55 to 125°C.



Minidip (Plastic and Ceramic)

SO-8

SCHEMATIC DIAGRAM
(one section)



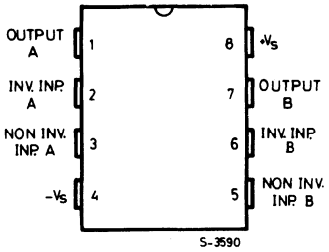
TL082

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage		± 18	V
V_{is}	Differential input voltage		± 30	V
V_i	Input voltage		± 15	V
T_{op}	Operating temperature	(TL082I)	-25 to 85	°C
		(TL082C)	0 to 70	°C
		(TL082M)	-55 to 125	°C
T_j	Junction temperature		150	°C
T_{stg}	Storage temperature		-65 to 150	°C

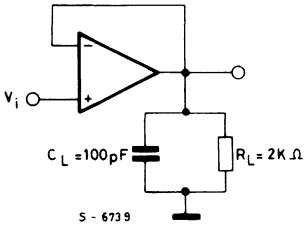
CONNECTION DIAGRAM AND ORDERING NUMBERS

(Top view)

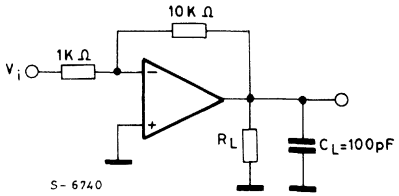


0 to 70°C	-25 to 85°C	-55 to 125°C	Package
TL082CJG TL082ACJG TL082BCJG	TL082IJG – –	TL082MJG – –	Ceramic Minidip
TL082CP TL082ACP TL082BCP	TL082IP – –	– – –	Plastic Minidip
TL082CD	TL082ID	–	SO-8

TEST CIRCUITS



Unity gain amplifier



Gain of 10 inverting amplifier

THERMAL DATA

			Plastic Minidip	Ceramic Minidip	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	120°C/W	150°C/W	200°C/W

ELECTRICAL CHARACTERISTICS ($V_s = \pm 15V$, $T_{amb} = 25°C$, otherwise specified)

Parameter		Test Conditions		"I"			"C"			"M"			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OS}	Input offset voltage	$R_s = 50\Omega$	TL082		3	6		5	15		3	6	mV
			TL082A					3	6				
			TL082B					2	3				
		$R_s = 50\Omega$, T_{amb} = full range	TL082			9			20			9	
			TL082A						7.5				
			TL082B						5				
$\frac{\Delta V_{OS}}{\Delta T}$	Input offset voltage drift	$R_s = 50\Omega$, T_{amb} = full range			10			10			10		$\mu V/°C$
I_{OS}	Input offset current		TL082		5	100		5	200		5	100	pA
			TL082A					5	100				
			TL082B					5	100				
		T_{amb} = full range	TL082			10			5			20	nA
			TL082A						3				
			TL082B						3				
I_b	Input bias current		TL082		30	200		30	400		30	200	pA
			TL082A					30	200				
			TL082B					30	200				
		T_{amb} = full range	TL082			20			10			50	nA
			TL082A						7				
			TL082B						7				
V_{CM}	Common mode input voltage range		TL082	± 11	± 12		± 10	± 11		± 11	± 12		V
			TL082A				± 11	± 12					
			TL082B				± 11	± 12					
V_{OPP}	Large signal voltage swing		$R_L = 10K\Omega$	24	27		24	27		24	27		V
		T_{amb} = full range	$R_L \geq 10K\Omega$	24			24			24			
			$R_L \geq 2K\Omega$	20	24		20	24		20	24		
G_V	Large signal voltage gain	$R_L \geq 2K\Omega$, $V_o = \pm 10V$	TL082	50	200		25	200					V/mV
			TL082A				50	200					
			TL082B				50	200					
		$R_L \geq 2K\Omega$, $V_o = \pm 10V$, T_{amb} = full range	TL082	25			15			15			
			TL082A				25						
			TL082B				25						
B	Unity gain bandwidth				3			3			3		MHz
R_i	Input resistance				10^{12}			10^{12}			10^{12}		Ω
CMR	Common mode	$R_s \geq 10K\Omega$	TL082	80	86		70	76		80	86		
			TL082A				80	86					
			TL082B				80	86					
SVR	Supply voltage	$R_s \geq 10K\Omega$	TL082	80	86		70	76		80	86		dB
			TL082A				80	86					
			TL082B				80	86					
I_S	Supply current	$R_L = \infty$			2.8	5.6		2.8	5.6		2.8	5.6	mA

ELECTRICAL CHARACTERISTICS (Continued)

Parameter		Test Conditions		"I"			"C"			"M"			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
CS	Channel separation	G_V = 100			120			120			120		dB
SR	Slew-rate at unity gain	V_I = 10V C_L = 100pF	R_L = 2KΩ		13			13		8	13		V/μs
t_r	Rise time	V_I = 20mV C_L = 100pF	R_L = 2KΩ		0.1			0.1			0.1		μs
	Overshot factor				10			10			10		%
e_N	Total input noise voltage	R_S = 100Ω f = 1KHz			25			25			25		$\frac{nV}{\sqrt{Hz}}$

Fig. 1 - Maximum peak to peak output voltage vs. frequency.

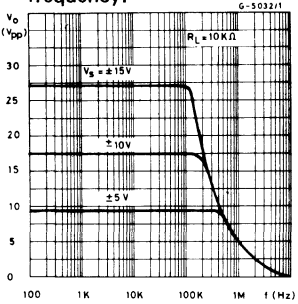


Fig. 2 - Maximum peak to peak output voltage vs. frequency.

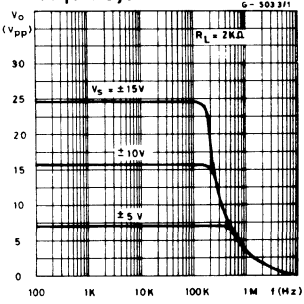


Fig. 3 - Maximum peak to peak output voltage vs. load resistance.

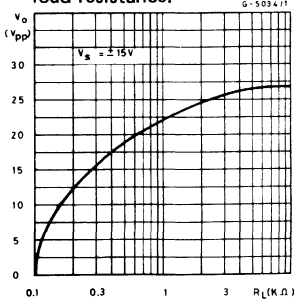


Fig. 4 - Large signal voltage gain and phase shift vs. frequency.

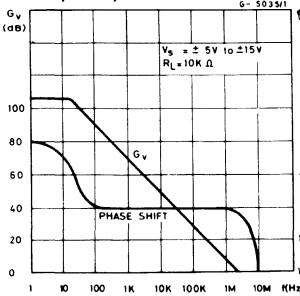


Fig. 5 - Supply current vs. temperature

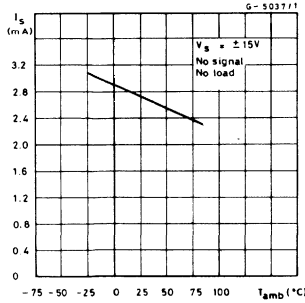


Fig. 6 - Supply current vs. supply voltage.

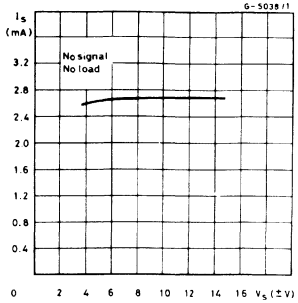


Fig. 7 - Input bias current vs. temperature.

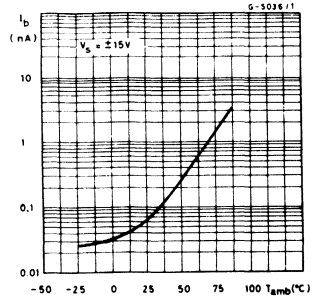


Fig. 8 - Voltage follower large signal pulse response

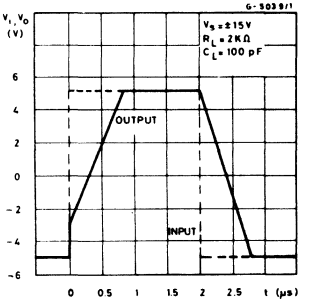


Fig. 9 - Output voltage vs. elapsed time.

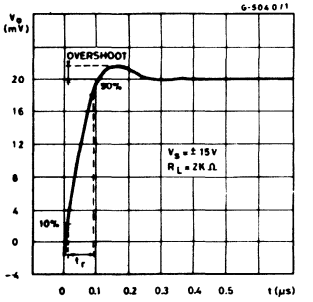


Fig. 10 - Equivalent input noise voltage vs. frequency.

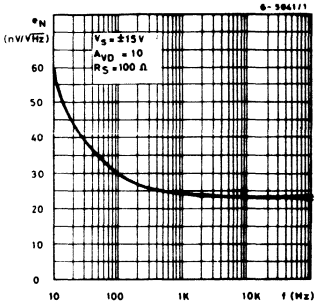


Fig. 11 - Total harmonic distortion vs. frequency.

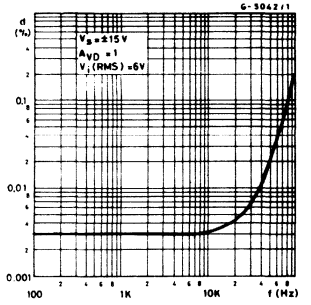
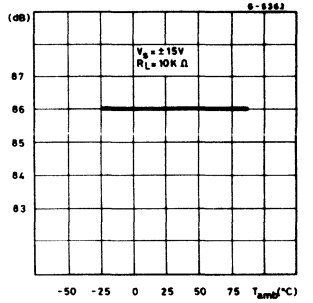
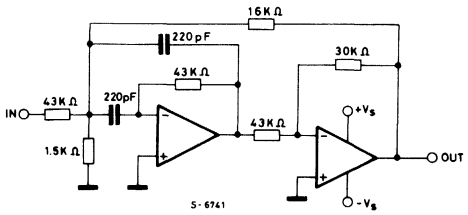


Fig. 12 - Common mode rejection vs. temperature



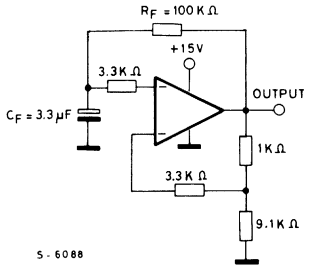
APPLICATION INFORMATION

Fig. 13 - Second order high Q band pass filter (f_o = 100 KHz, Q = 30, gain = 4)



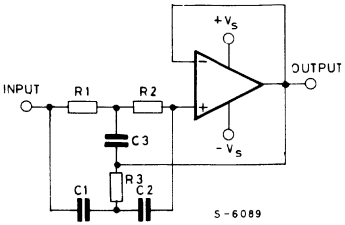
APPLICATION INFORMATION

Fig. 14 - 0.5 Hz square wave oscillator



$$f = \frac{1}{2\pi R_F C_F}$$

Fig. 15 - High Q Notch filter

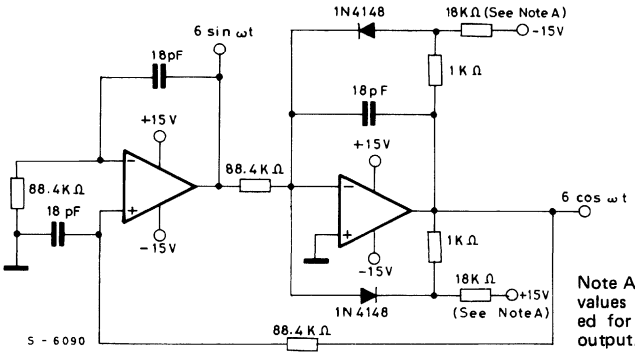


$$R1 = R2 = 2R3 = 1.5M\Omega$$

$$C1 = C2 = \frac{C3}{2} = 110\ pF$$

$$f_o = \frac{1}{2\pi R1\ C1} = 1\ KHz$$

Fig. 16 - 100 KHz quadrature oscillator



Note A: These resistor values may be adjusted for a symmetrical output.

Fig. 17 - 20 Hz to 200 Hz variable High-pass filter (G_v= 3 dB)

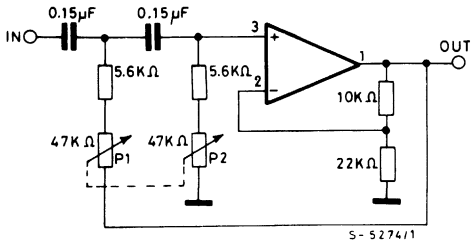
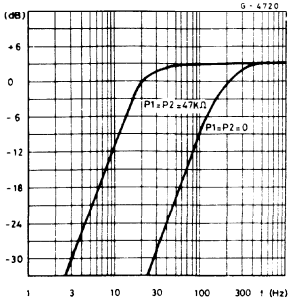


Fig. 18 - Frequency response of the high-pass filter of fig.17



APPLICATION INFORMATION (continued)

Fig. 19 - Unity-gain absolute-value circuit

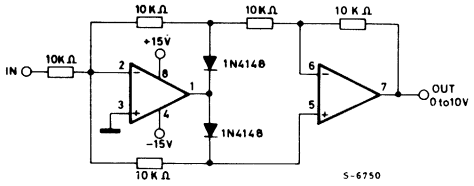


Fig. 20 - Single supply sample and hold

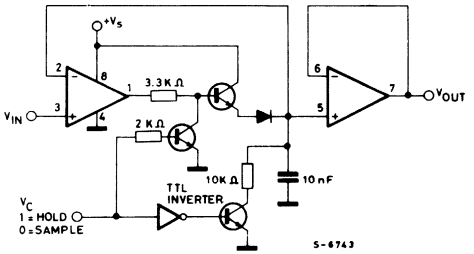
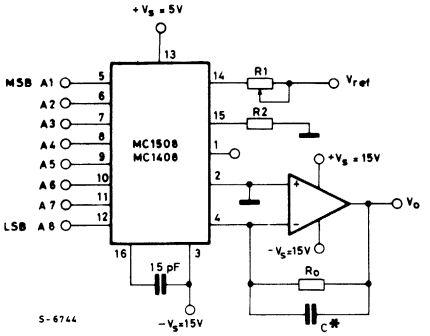


Fig. 21 - Output current to voltage transformation for a DA converter



(*) The value of C may be selected to minimize overshoot and ringing (C ≈ 68 pF).

Settling time to within 1/2 LSB (± 19.5 mV) is approximately 4.0 μs from the time all bits are switched.

Theoretical V_o :

$$V_o = \frac{V_{ref}}{R1}(R_o)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$$

Adjust V_{ref}, R1 or R_o so that V_o with all digital inputs at high level is equal to 9.961 volts.

$V_{ref} = 2.0\ V_{dc}$
$R1 = R2 \approx 1.0\ k\Omega$
$R_o = 5.0\ k\Omega$

$$V_o = \frac{2\ V}{1\ k}(5\ k)\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right]$$

$$= 10V\left[\frac{255}{256}\right] = 9.961V$$

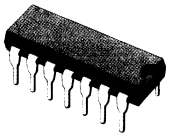
TL084

JFET-INPUT QUAD OPERATIONAL AMPLIFIERS

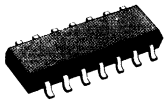
- HIGH SLEW-RATE . . . 13V/μs TYP.
- LOW POWER CONSUMPTION
- WIDE CONNOM-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW INPUT BIAS AND OFFSET CURRENTS
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE . . . JEFT-INPUT STAGE
- LATCH-UP-FREE OPERATION

The TL084 JFET-input operational amplifiers are designed to offer high slew-rate, low input bias and offset current, and low offset voltage temperature coefficient. Each JFET-input operational amplifier incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit.

Devices with an "I" suffix are characterized for operation from -25°C to 85°C, and those with a "C" suffix are characterized for operation from 0°C to 70°C. The "M" devices are characterized for operation from -55 to 125°C.

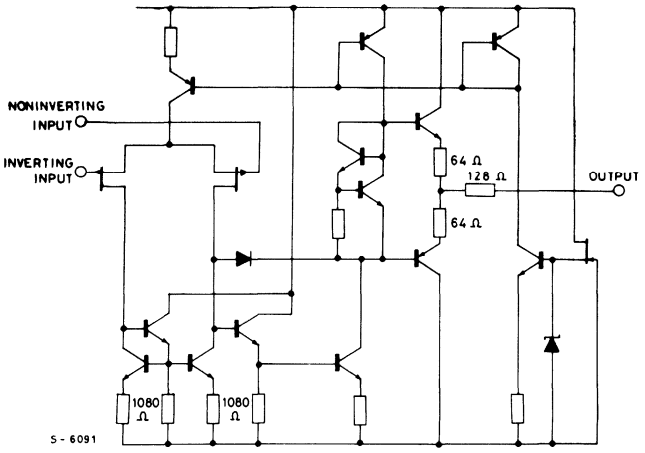


DIP-14
(Plastic and Ceramic)



SO-14

SCHEMATIC DIAGRAM
(one section)



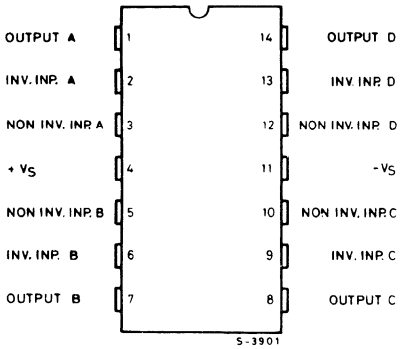
TL084

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage		± 18	V
V_{is}	Differential input voltage		± 30	V
V_i	Input voltage		± 15	V
T_{op}	Operating temperature	(TL084I)	-25 to 85	°C
		(TL084C)	0 to 70	°C
		(TL084M)	-55 to 125	°C
T_j	Junction temperature		150	°C
T_{stg}	Storage temperature		-55 to 150	°C

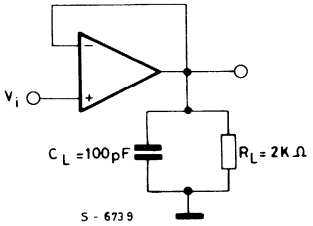
CONNECTION DIAGRAM AND ORDERING NUMBERS

(Top view)

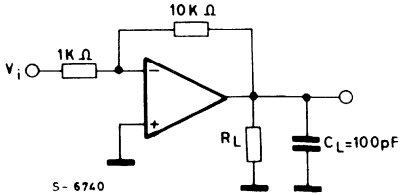


0 to 70°C	-25 + 85°C	-55 + 125°C	Package
TL084CJ TL084ACJ TL084BCJ	TL084IJ – –	TL084MJ – –	Ceramic DIP-14
TL084CN TL084ACN TL084BCN	TL084IN – –	– – –	Plastic DIP-14
TL084CD	TL084ID	–	SO-14

TEST CIRCUIT



Unity gain amplifier



Gain of 10 inverting amplifier

THERMAL DATA

			Ceramic DIP-14	SO-14	Plastic DIP-14
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	150°C/W	165°C/W	200°C/W

ELECTRICAL CHARACTERISTICS ($V_s = \pm 15V$, $T_{amb} = 25°C$, otherwise specified)

Parameter		Test Conditions		"I"			"C"			"M"			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OS}	Input offset voltage	$R_s = 50\Omega$	TL084		3	6		5	15		3	9	mV
			TL084A					3	6				
			TL084B					2	3				
		$R_s = 50\Omega$ T_{amb} = full range	TL084			9			20			15	
			TL084A						7.5				
			TL084B						5				
$\frac{\Delta V_{OS}}{\Delta T}$	Input offset voltage drift	$R_s = 50\Omega$ T_{amb} = full range			10			10			10		µV/°C
I_{OS}	Input offset current		TL084		5	100		5	200		5	100	pA
			TL084A					5	100				
			TL084B					5	100				
		T_{amb} = full range	TL084			10			5			20	nA
			TL084A						3				
			TL084B						3				
I_b	Input bias current		TL084		30	200		30	400		30	200	pA
			TL084A					30	200				
			TL084B					30	200				
		T_{amb} = full range	TL084			20			10			50	nA
			TL084A						7				
			TL084B						7				
V_{CM}	Common mode input voltage range		TL084	± 11	± 12		± 10	± 11		± 11	± 12		V
			TL084A				± 11	± 12					
			TL084B				± 11	± 12					
V_{OPP}	Large signal voltage gain		$R_L = 10K\Omega$	24	27		24	27		24	27		V
		T_{amb} = full range	$R_L \geq 10K\Omega$	24			24			24			
			$R_L \geq 2K\Omega$	20	24		20	24		20	24		
G_V	Large signal voltage gain	$R_L \geq 2K\Omega$ $V_o = \pm 10V$	TL084	50	200		25	200					V/mV
			TL084A				50	200					
			TL084B				50	200					
		$R_L \geq 2K\Omega$ $V_o = \pm 10V$ T_{amb} = full range	TL084	25			15			15			
			TL084A				25						
			TL084B				25						
B	Unity gain bandwidth				3			3			3		MHz
R_I	Input resistance				10^{12}			10^{12}			10^{12}		Ω
CMR	Common mode rejection	$R_s \geq 10K\Omega$	TL084	80	86		70	76		80	86		dB
			TL084A				80	86					
			TL084B				80	86					
SVR	Supply volage rejection	$R_s \geq 10K\Omega$	TL084	80	86		70	76		80	86		dB
			TL084A				80	86					
			TL084B				80	86					
I_S	Supply current	$R_L = \infty$			5.6	11.2		5.6	11.2		5.6	11.2	mA

ELECTRICAL CHARACTERISTICS (Continued)

Parameter		Test Conditions	"I"			"C"			"M"			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
CS	Channel separation	G_V = 100		120			120			120		dB
SR	Slew-rate at unity gain	V_i = 10V, R_L = 2KΩ, C_L = 100pF		13			12		8	13		V/μs
t_r	Rise time	V_i = 20mV, R_L = 2KΩ, C_L = 100pF		0.1			0.1			0.1		μs
	Overshot factor			10			10			10		%
e_N	Total input noise Voltage	R_S = 100Ω, f = 1KHz		25			25			25		$\frac{nV}{\sqrt{Hz}}$

Fig. 1 – Maximum peak to peak output voltage vs. frequency.

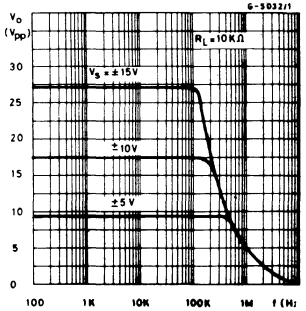


Fig. 2 – Maximum peak to peak output voltage vs. frequency

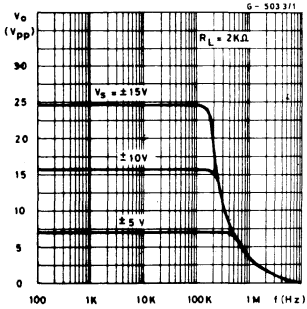


Fig. 3 – Maximum peak to peak output voltage vs. load resistance.

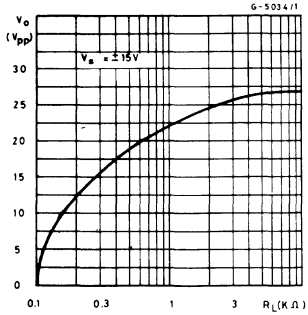


Fig. 4 – Large signal voltage gain and phase shift vs. frequency

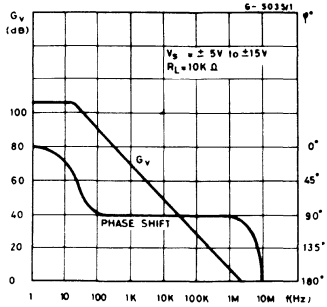


Fig. 5 – Supply current vs. temperature

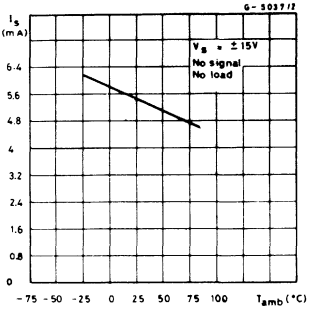


Fig. 6 – Supply current vs. supply voltage

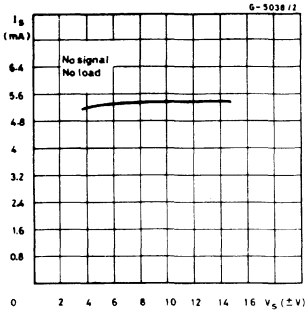


Fig. 7 – Input bias current vs. temperature

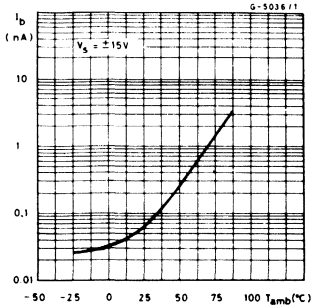


Fig. 8 – Voltage follower large signal pulse response

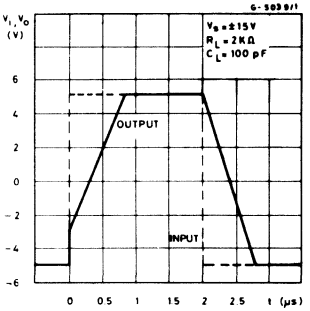


Fig. 9 – Output voltage vs. elapset time.

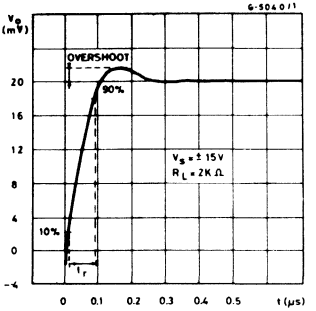


Fig. 10 – Equivalent input noise voltage vs. frequency

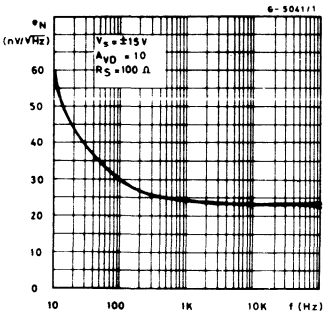


Fig. 11 Total harmonic distortion vs. frequency

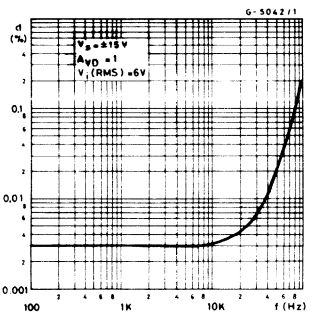
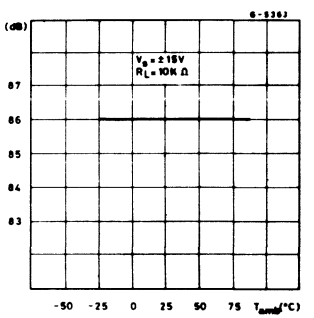
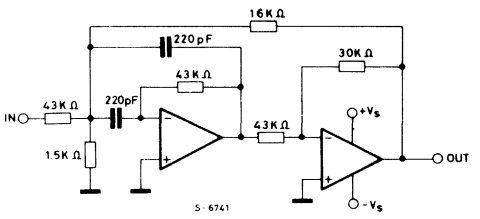


Fig. 12 – Common mode rejection vs. temperature



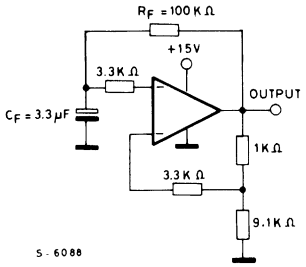
APPLICATION INFORMATION

Fig. 13 – Second order high Q band pass filter (f_o = 100KHz, Q = 30, gain = 4)



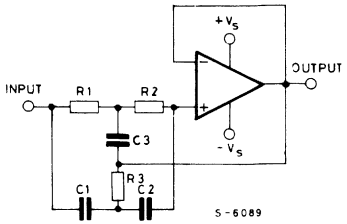
APPLICATION INFORMATION

Fig. 14 - 0.5 Hz square wave oscillator



$$f = \frac{1}{2\pi R_F C_F}$$

Fig. 15 - High Q Notch filter

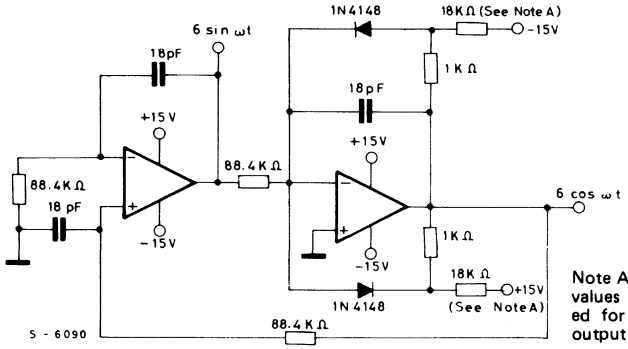


$$R1 = R2 = 2R3 = 1.5M\Omega$$

$$C1 = C2 = \frac{C3}{2} = 110\ pF$$

$$f_o = \frac{1}{2\pi R1\ C1} = 1\ KHz$$

Fig. 16 - 100 KHz quadrature oscillator



Note A: These resistor values may be adjusted for a symmetrical output.

Fig. 17 - 20 Hz to 200 Hz variable High-pass filter (G_v = 3 dB)

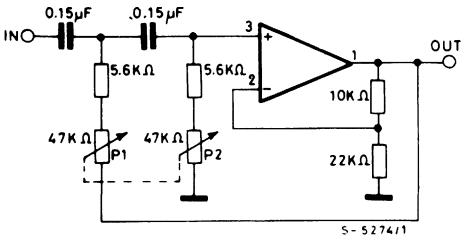
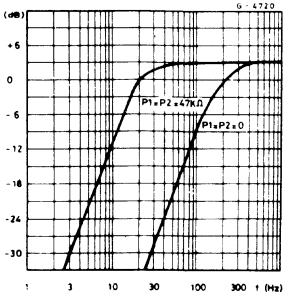


Fig. 18 - Frequency response of the high-pass filter of fig.17



APPLICATION INFORMATION (continued)

Fig. 19 – Unity-gain absolute-value circuit

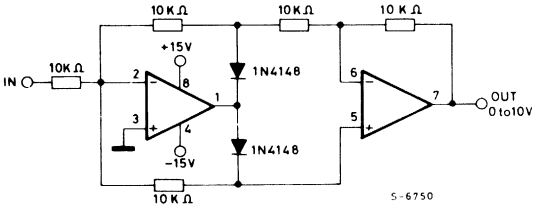


Fig. 20 – Single supply sample and hold

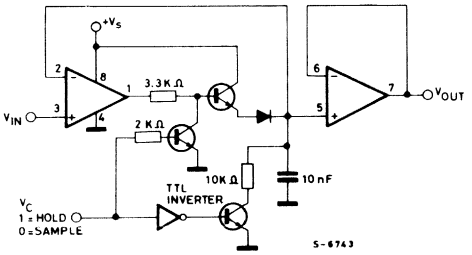
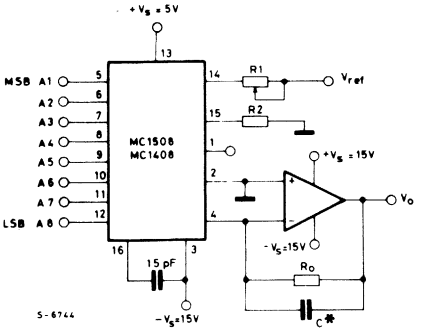


Fig. 21 - Output current to voltage transformation for a DA converter



(*) The value of C may be selected to minimize overshoot and ringing (C ≈ 68 pF).

Settling time to within 1/2 LSB (± 19.5 mV) is approximately 4.0 μs from the time all bits are switched.

Theoretical V_o :

$$V_o = \frac{V_{ref}}{R1}(R_o)\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

Adjust V_{ref}, R1 or R_o so that V_o with all digital inputs at high level is equal to 9.961 volts.

$V_{ref} = 2.0\ V_{dc}$
$R1 = R2 \approx 1.0\ k\Omega$
$R_o = 5.0\ k\Omega$

$$V_o = \frac{2\ V}{1\ k}(5\ k)\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256}\right]$$

$$= 10V\left[\frac{255}{256}\right] = 9.961V$$

TL7700A Series

SUPPLY VOLTAGE SUPERVISORS

- POWER-ON RESET GENERATOR
- AUTOMATIC RESET GENERATION AFTER VOLTAGE DROP
- WIDE SUPPLY VOLTAGE RANGE . . . 3V TO 18V
- PRECISION VOLTAGE SENSOR
- TEMPERATURE-COMPENSATED VOLTAGE REFERENCE
- TRUE AND COMPLEMENT RESET OUTPUTS
- EXTERNALLY ADJUSTABLE PULSE WIDTH

The TL7700A series are monolithic integrated circuit supply voltage supervisors specifically designed for use as reset controllers in microcomputer and microprocessor systems. During power-up the device tests the supply voltage and keeps the RESET and $\overline{\text{RESET}}$ outputs active (high and low, respectively) as long as the supply voltage has not reached its nominal voltage value. Taking $\overline{\text{RESIN}}$ low has the same effect. To ensure that the microcomputer system has reset, the TL7700A then initiates an internal time delay that delays the return of the reset outputs to their inactive states. Since the time delay for most microcomputers and microprocessors is in the order of several machine cycles, the device internal time delay is determined by an external time delay is determined by an external capacitor connected to the C_T input (pin 3).

$t_d = 1.3 \times 10^4 \times C_T$

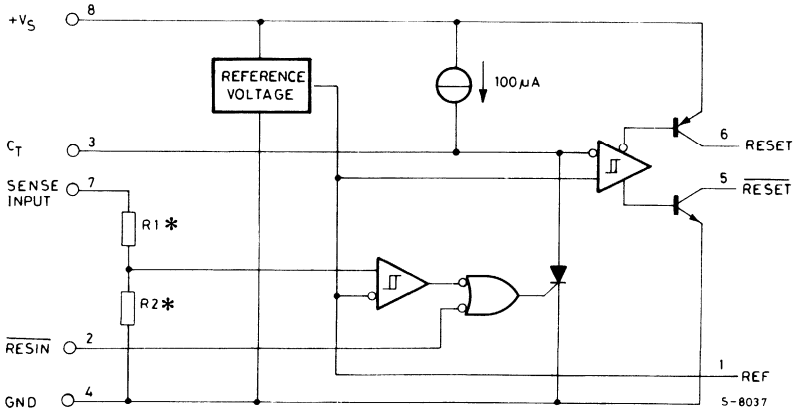
Where: C_T is in farads (F) and t_d is in seconds(s)

In addition, when the supply voltage drops below the nominal value, the outputs will be active until the supply voltage returns to the nominal value. An external capacitor (typically 0.1μF) must be connected to the REF output (pin 1) to reduce the influence of fast transients in the supply voltage.

The TL7700AI series is characterized for operation from -25°C to 85°C; the TL7700AC series is characterized from 0°C to 70°C.

Plastic Minidip SO-8

BLOCK DIAGRAM



* TL7702A R1 = 0Ω, R2 = open; TL7705A R1 = 7.8KΩ, R2 = 10KΩ; TL7709A R1 = 19.7KΩ, R2 = 10KΩ; TL7712A R1 = 32.7KΩ, R2 = 10KΩ; TL7715A R1 = 43.4KΩ, R2 = 10KΩ

ABSOLUTE MAXIMUM RATINGS

V_S	Supply voltage, V_{CC} (see Note 1)	20	V
V_i	Input voltage range at $\overline{RESIN}$	-0.3 to 20	V
V_i	Input voltage at SENSE: TL7702A (see Note 2)	-0.3 to 6	V
	TL7705A	-0.3 to 10	V
	TL7709A	-0.3 to 15	V
	TL7712A	-0.3 to 20	V
	TL7715A	-0.3 to 20	V
I_{OH}	High-level output current at $\overline{RESET}$	-30	mA
I_{OL}	Low-level output current at $\overline{RESET}$	30	mA
T_{amb}	Operating free-air temperature range: TL77XXAI	-40 to 85	°C
	TL77XXAC	0 to 70	°C
T_{stg}	Storage temperature range	-65 to 150	°C

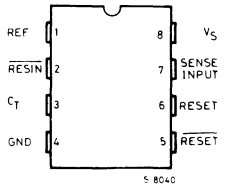
Notes: 1. All voltage values are with respect to the network ground terminal
2. For the TL7702A, the voltage applied to the SENSE terminal must never exceed V_S

RECOMMENDED OPERATING CONDITIONS

Parameters			Min.	Max.	Unit
V_S	Supply voltage		3.6	18	V
V_{IH}	High-level input voltage at RESIN		2		V
V_{IL}	Low-level input voltage at RESIN			0.6	V
V_i	Voltage at sense input	TL7702A	0	See Note 3	V
		TL7705A	0	10	
		TL7709A	0	15	
		TL7712A	0	20	
		TL7715A	0	20	
I_{OH}	High-level output current at RESET			-16	mA
I_{OL}	Low-level output current at $\overline{RESET}$			16	mA
T_{amb}	Operating free-air temperature range	TL77 - AI	-40	85	°C
		TL77 - AC	0	70	

Note 3: For proper operation of the TL7702A, the voltage applied to the SENSE terminal should not exceed V_S - 1V or 6V, whichever is less

CONNECTION DIAGRAM AND ORDERING NUMBER



Temperature range	Plastic Minidip	SO-8
Commercial 0 to 70°C	TL77XXACP	TL77XXACD
Industrial -40 to 85°C	TL77XXAIP	TL77XXAID

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max.	120	°C/W

ELECTRICAL CHARACTERISTICS

These specifications unless otherwise specified, apply for: T_{amb} = -40 to 85°C (TL77XXAI); T_{amb} = 0 to 70°C (TL77XXAC)

Parameter			Test Conditions (1)	Min.	Typ.	Max.	Unit
V_{OH}	High-level output voltage at RESET		I_{OH} = -16mA	V_S-1.5			V
V_{OL}	Low-level output voltage at $\overline{RESET}$		I_{OL} = 16mA			0.4	V
V_{ref}	Reference voltage		T_{amb} = 25°C	2.48	2.53	2.58	V
V_T	Threshold Voltage at SENSE input	TL7702A	V_S = 3.6V to 18V T_{amb} = 25°C	2.48	2.53	2.58	V
		TL7705A		4.5	4.55	4.6	
		TL7709A		7.5	7.6	7.7	
		TL7712A		10.6	10.8	11.0	
		TL7715A		13.2	13.5	13.8	
V_T	Threshold voltage at SENSE input	TL7702A	V_S = 3.6V to 18V	2.45	2.53	2.58	V
		TL7705A		4.45	4.55	4.6	
		TL7709A		7.4	7.6	7.7	
		TL7712A		10.4	10.8	11.0	
		TL7715A		13.0	13.5	13.8	
V_{T+}, V_{T-}	Hysteresis (2) at SENSE input	TL7702A	V_S = 3.6V to 18V T_{amb} = 25°C		10		mV
		TL7705A			15		
		TL7709A			20		
		TL7712A			35		
		TL7715A			45		
I_I	Input current at $\overline{RESIN}$ input		V_i = 2.4V to V_S			20	μA
			V_i = 0.4V			-100	
I_I	Input current at SENSE input	TL7702A	$V_{ref} < V_I < V_S$ -1.5V		0.5	2	
I_{OH}	High-level output current at $\overline{RESET}$		V_O = 18V			50	
I_{OL}	Low-level output current at RESET		V_O = 0V			-50	
I_S	Supply current		All inputs and out. open		1.8	3	mA

1. All characteristics are measured with C = 0.1μF from Pin 1 to GND, and with C = 0.1μF from Pin 3 to GND
2. Hysteresis is the difference between the positive going input threshold voltage. V_{T+}, and the negative going input threshold voltage, V_{T-}.

SWITCHING CHARACTERISTICS

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
t_{pi}	Pulse width at SENSE input	$V_{ih} = V_{ityp} + 0.04 \times V_i$ $V_{il} = V_{ityp} - 0.04 \times V_i$	0.9			µs
t_{pi}	Pulse width at $\overline{RESIN}$ input		0.4			µs
t_{po}	Pulse width at output	Cf = 0.1µF	0.65	1.3	2.6	ms
t_{pdHL}	Propagation delay time from $\overline{RESIN}$ to $\overline{RESET}$	V_S = 5V R_L = 4.7KΩ			1	µs
$t_{r/f}$	Rise/Falltime at RESET and $\overline{RESET}$	V_S = 5V R_L = 4.7KΩ			1	µs

Fig. 1 - Multiple power supply system reset generation

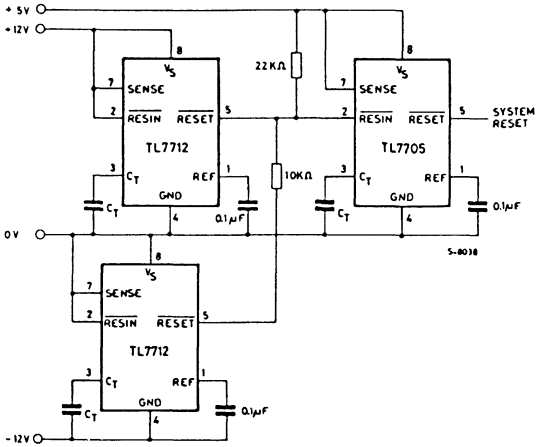
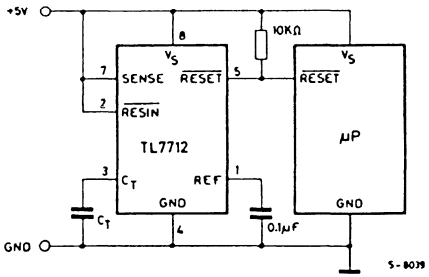


Fig. 2 - Reset controller for µP



UC1840
UC2840
UC3840

PRELIMINARY DATA

PROGRAMMABLE, OFF-LINE, PWM CONTROLLER

- ALL CONTROL, DRIVING, MONITORING, AND PROTECTION FUNCTIONS INCLUDED
- LOW-CURRENT, OFF-LINE START CIRCUIT
- FEED-FORWARD LINE REGULATION OVER 4 TO 1 INPUT RANGE
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- PULSE-BY-PULSE CURRENT LIMITING PLUS SHUTDOWN FOR OVER-CURRENT FAULT
- NO START-UP OR SHUTDOWN TRANSIENTS
- SLOW TURN-ON AND MAXIMUM DUTY-CYCLE CLAMP
- SHUTDOWN UPON OVER- OR UNDER-VOLTAGE SENSING
- LATCH OFF OR CONTINUOUS RETRY AFTER FAULT
- REMOTE, PULSE-COMMANDABLE START/STOP
- PWM OUTPUT SWITCH USABLE TO 1A PEAK CURRENT
- 1% REFERENCE ACCURACY
- 500 kHz OPERATION

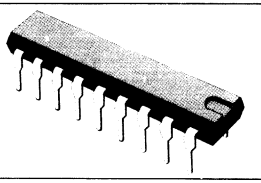
Although containing most of the features required by all types of switching power supply controllers, the UC1840 family has been optimized for highly-efficient boot-strapped primary-side operation in forward or flyback power converters. Two important features for this mode are a starting circuit which requires little current from the primary input voltage and feed-forward control for constant volt-second operation over a wide input voltage range.

In addition to startup and normal regulating PWM functions, these devices offer built-in protection from over-voltage, under-voltage, and over-current fault conditions. This monitoring circuitry contains the added features that any fault will initiate a complete shutdown with provisions for either latch off or automatic restart. In the latch-off mode. the controller may be started and stopped with external pulsed or steady-state commands.

Other performance features of these devices include a 1% accurate reference, provision for slow-turn-on and duty-cycle limiting, and high-speed pulse-by-pulse current limiting in addition to current fault shutdown.

The UC1840's PWM output stage includes a latch to insure only a single pulse per period and is designed to optimize the turn off of an external switching device by conducting during the "OFF" time with a capability for both high peak current and low saturation voltage. These devices are available in an 18-pin dual-in-line plastic or ceramic package.

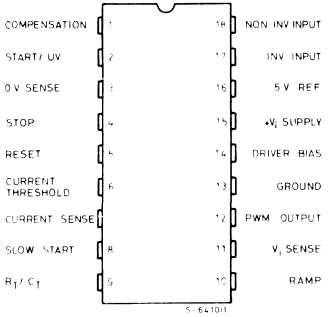
The UC1840 is characterized for operation over the full military temperature range of -55°C to +125°C. The UC2840 and UC3840 are designed for operation from -25°C to +85°C and 0°C to +70°C, respectively.



DIP-18 Plastic

CONNECTION DIAGRAM AND ORDERING NUMBERS

(top view)

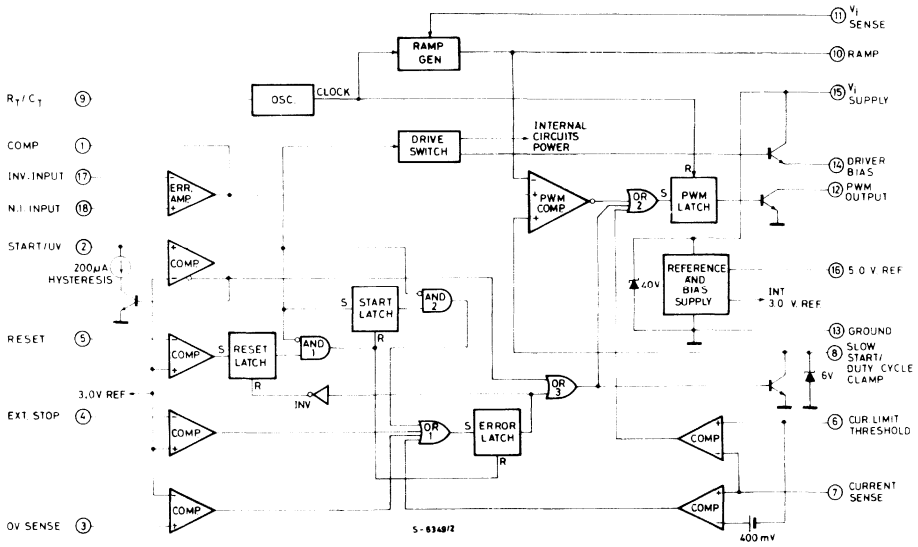


Type	Plastic	Ceramic
UC1840	—	UC1840J
UC2840	UC2840N	UC2840J
UC3840	UC3840N	UC3840J

ABSOLUTE MAXIMUM RATINGS

V_i	Supply voltage + V_i (pin 15)		
	Voltage driven	32	V
	Current driven 100 mA maximum	self limiting	
V_o	PWM output voltage (pin 12)	40	V
I_o	PWM output current, steady-state (pin 12)	400	mA
E_{op}	PWM output peak energy discharge	20	μJ
	Driver bias current (pin 14)	-200	mA
$I_{o(REF)}$	Reference output current (pin 16)	-50	mA
	Slow start sink current (pin 8)	20	mA
	V_i sense current (pin 11)	10	mA
	Current limit inputs (pin 6, 7)	-0.5 to +5.5	V
	Comparator inputs (pins 2, 3, 4, 5, 17, 18)	-0.3 to +32	V
P_{tot}	Power dissipation at $T_{amb} = 70°C$	1000	mW
T_j	Junction temperature range	-55 to 150	°C
T_{op}	Operating ambient temperature range: UC1840	-55 to 125	°C
	UC2840	-25 to 85	°C
	UC3840	0 to 70	°C
T_{stg}	Storage temperature	-65 to + 150	°C

BLOCK DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

FUNCTIONAL DESCRIPTION

Name	Function
PWM CONTROL	
OSCILLATOR	Generates a fixed-frequency internal clock from an external R_T and C_T. Frequency $= \frac{K_c}{R_T C_T}$ where K_c is a first-order correction factor $\approx$ 0.3 log (C_T X 10^{12}).
RAMP GENERATOR	Develops a linear ramp with a slope defined externally by $\frac{dv}{dt} = \frac{\text{sense voltage}}{R_R\ C_R} \cdot C_R$ is normally selected $\leqslant C_T$ and its value will have some effect upon valley voltage. C_R terminal can be used as an input port for current mode control.
ERROR AMPLIFIER	Conventional operational amplifier for closed-loop gain and phase compensation. Low output impedance: unity-gain stable.
REFERENCE GENERATOR	Precision 5.0V for internal and external usage to 50 mA. Tracking 3.0V reference for internal usage only with nominal accuracy of ± 2%. 40V clamp zener for chip O.V. protection, 100mA maximum current.
PWM COMPARATOR	Generates output pulse which starts at termination of clock pulse and ends when the ramp input crosses the lowest of two positive inputs.
PWM LATCH	Terminates the PWM output pulse when set by inputs from either the PWM comparator, the pulse-by-pulse current limit comparator, or the error latch. Resets with each internal clock pulse.
PWM OUTPUT SWITCH	Transistor capable of sinking current to ground which is off during the PWM on-time and turns on to terminate the power pulse. Current capacity is 400mA saturated with peak capacitance discharge in excess of one amp.

FUNCTIONAL DESCRIPTION (continued)

Name	Function
SEQUENCING FUNCTIONS	
START/U.V. SENSE	This comparator performs three functions. With an increasing voltage, it generates a turn-on signal at a start threshold. With a decreasing voltage, it generates a U.V. fault signal at a lower level separated by a 200 μA hysteresis current. At the U.V. threshold, it also resets the Error Latch if the Reset Latch has been set.
DRIVE SWITCH	Disables most of the chip to hold internal current consumption low, and Driver Bias OFF, until input voltage reaches start threshold.
DRIVE BIAS	Supplies drive current to external power switch to provide turn-on bias.
SLOW START	Clamps low to hold PWM OFF. Upon release, rises with rate controlled by R_SC_S for slow increase of output pulse width. Also used to clamp maximum duty cycle with divider R_S R_{DC}.
START LATCH	Keeps low input voltage at initial turn-on from being defined as a U.V. fault. Sets at start level to monitor for U.V. fault.
RESET LATCH	When reset, this latch insures no reset signal to either Start or Error latches so that first fault will lock the PWM off. When set, this latch resets the Start and Error latches at the U.V. low threshold, allowing a restart.
PROTECTION FUNCTIONS	
ERROR LATCH	When set by momentary input, this latch insures immediate PWM shutdown and hold off until reset. Inputs to Error Latch are: a. U.V. low (after turn-on) b. O.V. high c. Step low d. Current Sense 400mV over threshold. Error Latch resets at U.V. threshold if Reset Latch is set.
CURRENT LIMITING	Differential input comparator terminates individual output pulses each time sense voltage rises above threshold. When sense voltage rises to 400 mV above threshold, a shutdown signal is sent to Error Latch.

ELECTRICAL CHARACTERISTICS (Refer to the test circuit. Unless otherwise stated, these specifications apply for T_j = -55 to + 125°C for the UC1840, -25°C to + 85°C for the UC2840 and 0 to 70°C for the UC3840; V_i = 20V, R_T = 20KΩ, C_T = 0.001 μF, C_R = 0.001 μF, current limit threshold = 200mV

Parameter		Test conditions	UC1840 UC2840			UC3840			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
POWER INPUTS									
I_{ST}	Start-up current	V_i = 30V, Pin 2= 2.5V, T_j = 25°C		4	5.5		4	5.5	mA
	*Start-up current T.C.	V_i = 30V, Pin 2= 2.5V		-0.1	-0.2		-0.1	-0.2	%/°C
I_i	Operating current	V_i = 30V, Pin 2= 3.5V	5	10	15	5	10	15	mA
V_{SOV}	Supply O.V. clamp	I_i = 20mA	33	40	45	33	40	48	V
REFERENCE SECTION									
V_{REF}	Reference voltage	T_j = 25°C	4.95	5	5.05	4.9	5	5.1	V
ΔV_{REF}	Line regulation	V_i = 8 to 30V		10	15		10	20	mV
ΔV_{REF}	Load regulation	I_L = 0 to 20 mA		10	20		10	30	mV
$\Delta V_{REF}/\Delta T$*	Temperat. coeff.	Over op. temp. range			± 0.4			± 0.4	mV/°C
I_{SC}	Short circuit curr.	V_{REF}= 0, T_j = 25°C		-80	-100		-80	-100	mA
OSCILLATOR									
f_s	Nominal frequency	T_j = 25°C	47	50	53	45	50	55	KHz
	Voltage stability	V_i = 8 to 30V		0.5	1		0.5	1	%
	* Temperature coeff.	Over op. temp. range			± 0.08			± 0.08	%/°C
$f_{s(max)}$	Maxim. frequency	R_T= 2KΩ, C_T= 330pF	500			500			KHz
RAMP GENERATOR									
	Ramp current min.	I_{SENSE}= -10 μA		-11	-14		-11	-14	μA
	Ramp current max.	I_{SENSE}= 1 mA	-0.9	-0.95		-0.9	-0.95		mA
	Ramp valley		0.3	0.5	0.7	0.3	0.5	0.7	V
	Ramp peak	Clamping level	3.9	4.2	4.5	3.9	4.2	4.5	V
ERROR AMPLIFIER									
V_{os}	Input offset voltage	V_{CM}= 5V		0.5	5		2	10	mV
I_b	Input bias current			0.5	2		1	5	μA
I_{os}	Input offset current				0.5			0.5	μA
G_v	Open loop gain	ΔV_o= 1 to 3V	60	66		60	66		dB
	Output swing (max Out ⩽ Ramp peak -100 mV)	Minimum total range	0.3		3.5	0.3		3.5	V
CMR	Common mode rejection	V_{CM}= 1.5 to 5.5V	70	80		70	80		dB
SVR	Supply voltage rejection	V_i = 8 to 30V	40	50		40	50		dB

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	UC1840 UC2840			UC3840			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{SC}	Short circuit curr.	V_{comp} = 0V		-4	-10		-4	-10	mA
B*	Gain bandwidth	T_j = 25°C, G_V = 0 dB	1	2		1	2		MHz
SR*	Slew rate	T_j = 25°C, G_V = 0 dB		0.8			0.8		V/μs

PWM SECTION

	* Continuous duty cycle range (other than zero)	Min. total cont. range Ramp peak < 4.2V	5		95	5		95	%
$V_{o(sat)}$	Output saturation	I_o = 20 mA		0.2	0.4		0.2	0.4	V
$V_{o(sat)}$	Output saturation	I_o = 200 mA		1.7	2.2		1.7	2.2	V
I_{OL}	Output leakage	V_o = 40V		0.1	10		0.1	10	μA
τ_d	* Comparator delay	Pin 8 to pin 12 T_j= 25°C, R_L= 1 KΩ		300	500		300	500	ns

SEQUENCING FUNCTIONS

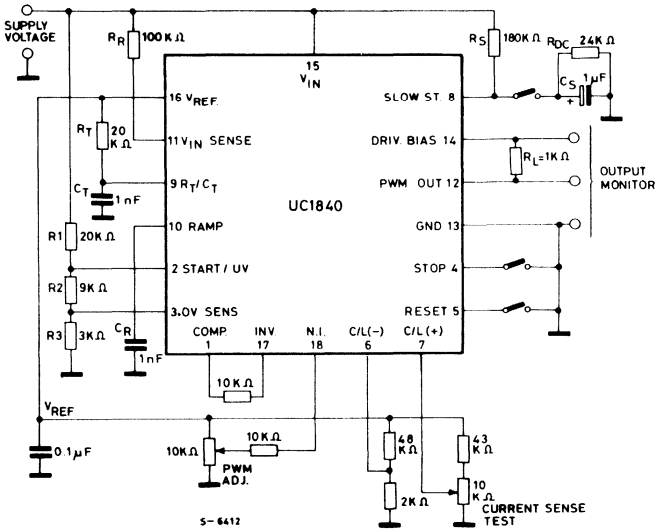
V_T	Comparator threshold	Pins 2, 3, 4, 5	2.8	3	3.2	2.8	3	3.2	V
I_b	Input bias current	Pins 3, 4, 5 = 0V		-1	-3		-1	-3	μA
	Start/UV Hysteresis current	Pin 2 = 2.5V, T_j = 25°C	180	200	220	170	200	230	μA
	Input leakage	V_i = 20V		0.1	10		0.1	10	μA
	Driver bias saturation voltage V_{IN}-V_{OH}	I_B = -50 mA		2	3		2	3	V
	Driver bias leakage	V_B = 0V		-0.1	-10		-0.1	-10	μA
	Slow-start saturat.	I_s = 2 mA		0.2	0.5		0.2	0.5	V
	Slow-start leakage	V_s = 4.5V		0.1	2		0.1	2	μA

CURRENT CONTROL

	Current limit offset			0	5		0	10	mV
	Current shutdown offset		370	400	430	360	400	440	mV
I_b	Input bias current	Pin 7 = 0V		-2	-5		-2	-5	μA
	* Common mode range		-0.4		3	-0.4		3	V
τ_d*	Current limit delay	T_j= 25°C, Pin 7 to 12, R_L= 1KΩ		200	400		200	400	ns

* Guaranteed by design. Not 100% tested in production.

Fig. 1 - Open loop test circuit



Nominal frequency = $\frac{1}{R_T C_T}$ = 50 kHz

Start voltage = $3\left(\frac{R1 + R2 + R3}{R2 + R3}\right) + 0.2\,R1 = 12V$

U.V. fault voltage = $3\left(\frac{R1 + R2 + R3}{R2 + R3}\right) = 8V$

O.V. fault voltage = $3\left(\frac{R1 + R2 + R3}{R3}\right) = 32V$

Current limit = 200 mV
Current fault voltage = 600 mV
Duty cycle clamp = 50%

Fig. 2 - Start U.V. hysteresis current

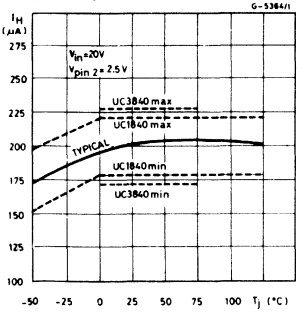


Fig. 3 - PWM Output saturation voltage

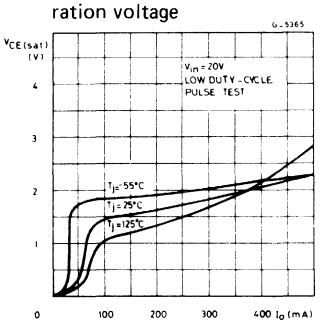


Fig. 4 - Oscillator frequency

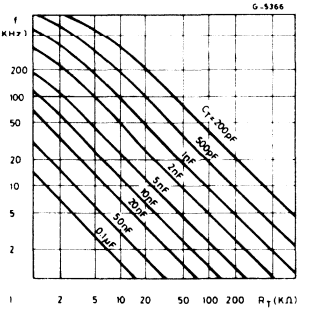


Fig. 5 - PWM output minimum pulse width

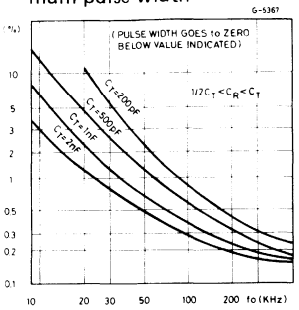


Fig. 6 - Error amplifier open-loop gain and phase

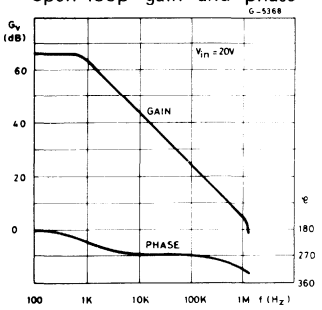
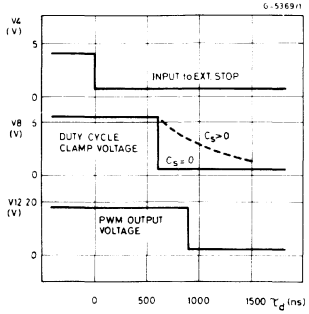
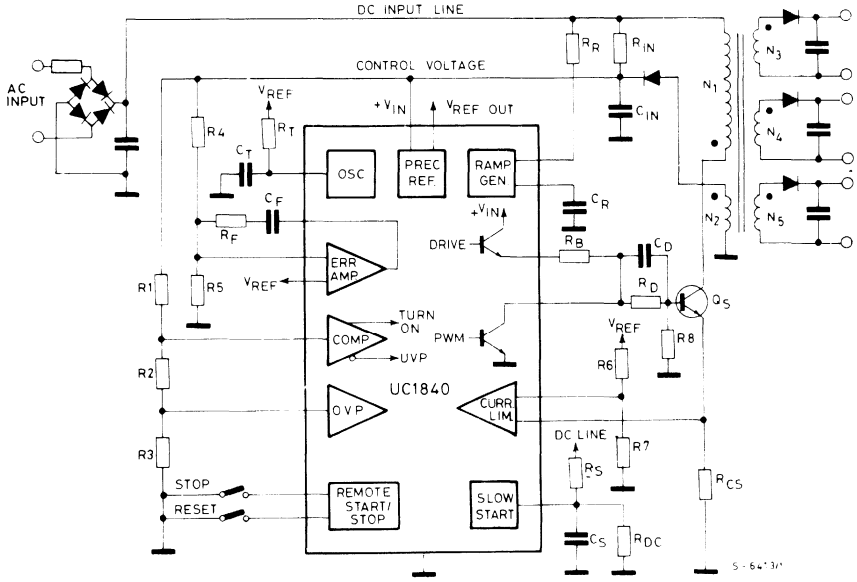


Fig. 7 - Shutdown timing



APPLICATION INFORMATION

Fig. 8 - Programmable PWM controller in a simplified flyback regulator



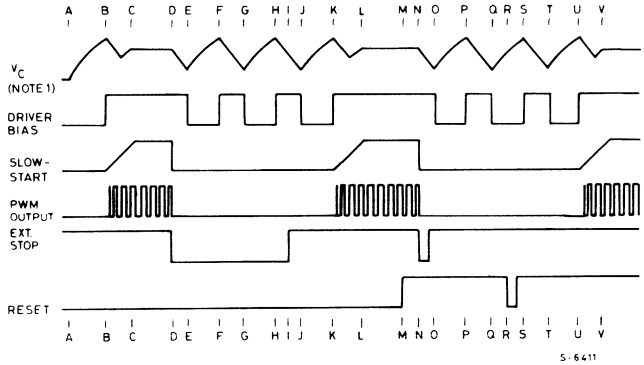
APPLICATION INFORMATION (continued)

In this application (see Fig. 8) complete control is maintained on the primary side. Control power is provided by R_{IN} and C_{IN} during start-up, and by a primary-referenced low voltage winding. N2, for efficient operation after start. The error amplifier loop is closed to regulate the DC voltage from N2 with other outputs following through their magnetic coupling – a task made even easier with the UC1840's feed-forward line regulation.

The UC1840 will readily accept digital start/stop commands transmitted from the secondary side by means of optical couplers.

Not shown are protective snubbers or additional interface circuitry which may be required by the choice of the high-voltage switch, Qs, or the application.

Fig. 9 - Power sequencing functions



Notes: 1. VC represents an analog of the output voltage generated by a primary-referenced secondary winding on the power transformer. It is the voltage monitored by the start/U.V. comparator and, in most cases, is the supply voltage, V_i, for the UC1840.

2. Although input to External Stop, Pin 4, is shown, results are the same for any fault input which sets the Error Latch.

Power Frequency Functions

Time	Event
A	Initial turn-on, V_c rises with light load
B	Start threshold. Driver Bias loads V_c
C	Operating PWM regulates V_c
D	Stop input sets Error Latch turning off PWM
E	U.V. low threshold. Error Latch remain set
F	Start turns on Driver Bias bus Error Latch still set
G, H	V_c and Driver Bias continue to cycle
I	Stop command removed
J	Error Latch reset at U.V. low threshold
K	Start threshold now removes slow-start clamp
L	Return to normal run state
M	Reset Latch set signal removed
N	Error Latch set with momentary fault
O	Error Latch does not reset as Reset Latch is reset
P, Q	V_c and Driver Bias recycle with no turn-on
R	Reset Latch set is set with momentary Reset signal
S	V_c must complete cycle to turn-on
T	Start and Error Latches reset
U	Normal start initiated
V	Return to normal run state

UC1842/3/4/5
UC2842/3/4/5
UC3842/3/4/5

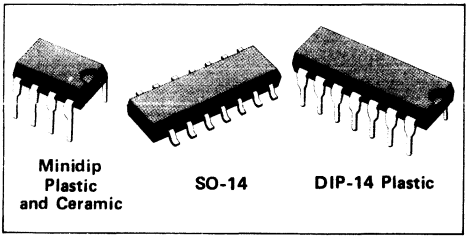
ADVANCE DATA

CURRENT MODE PWM CONTROLLER

- OPTIMIZED FOR OFF-LINE AND DC TO DC CONVERTERS
- LOW START-UP CURRENT (< 1mA)
- AUTOMATIC FEED FORWARD COMPENSATION
- PULSE-BY-PULSE CURRENT LIMITING
- ENHANCED LOAD RESPONSE CHARACTERISTICS
- UNDER-VOLTAGE LOCKOUT WITH HYSTERESIS
- DOUBLE PULSE SUPPRESSION
- HIGH CURRENT TOTEM POLE OUTPUT
- INTERNALLY TRIMMED BANDGAP REFERENCE
- 500KHz OPERATION
- LOW R_O ERROR AMP

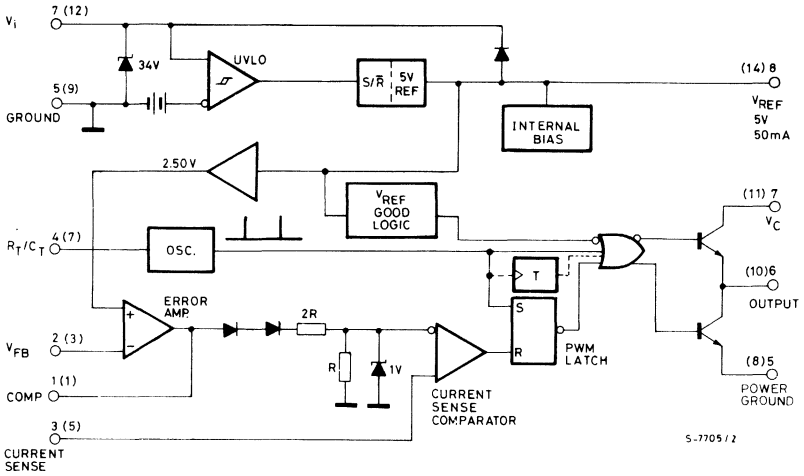
The UC1842/3/4/5 family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under voltage lockout featuring start-up current less than 1mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off-state.

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC1842 and UC1844 have UVLO thresholds of 16V (on) and 10V (off), ideally suited to off-line applications. The corresponding thresholds for the UC1843 and UC1845 are 8.5V and 7.9V. The UC1842 and UC1843 can operate to duty cycles approaching 100%. A range of zero to < 50% is obtained by the UC1844 and UC1845 by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.



Minidip Plastic and Ceramic | **SO-14** | **DIP-14 Plastic**

BLOCK DIAGRAM (Toggle flip flop used only in UC1844 and UC1845)



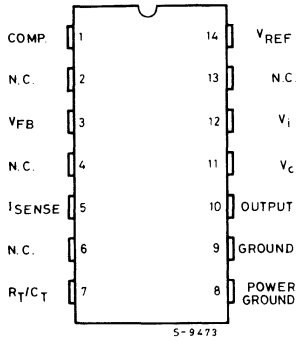
ABSOLUTE MAXIMUM RATINGS *

V_i	Supply voltage (Low impedance source)	30	V
V_i	Supply voltage ($I_i < 30mA$)	Self limiting	
I_O	Output current	± 1	A
E_O	Output energy (capacitive load)	5	μJ
	Analog inputs (Pins 2, 3)	-0.3 to 6.3	V
	Error amplifier output sink current	10	mA
P_{tot}	Power dissipation at $T_{amb} \leq 50°C$ (Minidip, DIP-14)	1	W
P_{tot}	Power dissipation at $T_{amb} \leq 25°C$ (SO-14)	725	mW
T_{stg}	Storage temperature range	-65 to 150	°C
T_L	Lead temperature (Soldering 10s)	300	°C

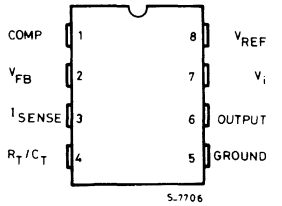
* All voltages are with respect to pin 5, all currents are positive into the specified terminal.

CONNECTION DIAGRAMS
(Top view)

DIP-14 / SO-14



Minidip Plastic and Ceramic



ORDERING NUMBERS

TYPE	PLASTIC MINIDIP	CERAMIC MINIDIP	DIP-14	SO-14
UC1842 UC1843 UC1844 UC1845		UC1842J UC1843J UC1844J UC1845J		
UC2842 UC2843 UC2844 UC2845	UC2842N UC2843N UC2844N UC2845N	UC2842J UC2843J UC2844J UC2845J	UC2842B UC2843B UC2844B UC2845B	UC2842D UC2843D UC2844D UC2845D
UC3842 UC3843 UC3844 UC3845	UC3842N UC3843N UC3844N UC3845N	UC3842J UC3843J UC3844J UC3845J	UC3842B UC3843B UC3844B UC3845B	UC3842D UC3843D UC3844D UC3845D

THERMAL DATA

		Ceramic Minidip	Plastic Minidip	DIP-14 Plastic	SO-14
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	200°C/W	100°C/W	100°C/W	165°C/W

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for $-55 \leq T_{amb} \leq 125°C$ for UC184X; $-25 \leq T_{amb} \leq 85°C$ for UC284X; $0 \leq T_{amb} \leq 70°C$ for UC384X; $V_i = 15V$ (Note 5); $R_T = 10K$; $C_T = 3.3nF$)

Parameter		Test Conditions	UC184X UC284X			UC384X			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
REFERENCE SECTION									
V_{REF}	Output voltage	$T_j = 25°C$ $I_o = 1mA$	4.95	5.00	5.05	4.90	5.00	5.10	V
ΔV_{REF}	Line regulation	$12V \leq V_i \leq 25V$		6	20		6	20	mV
ΔV_{REF}	Load regulation	$1 \leq I_o \leq 20mA$		6	25		6	25	mV
$\Delta V_{REF}/\Delta T$	Temperature stability	(Note 2)		0.2	0.4		0.2	0.4	mV/°C
	Total output variation	Line, Load, Temperature (Note 2)	4.9		5.1	4.82		5.18	V
e_N	Output noise voltage	$10Hz \leq f \leq 10KHz$ $T_j = 25°C$ (Note 2)		50			50		μV
	Long term stability	$T_{amb} = 125°C$, 1000 Hrs (Note 2)		5	25		5	25	mV
I_{sc}	Output short circuit		-30	-100	-180	-30	-100	-180	mA
OSCILLATOR SECTION									
f_s	Initial accuracy	$T_j = 25°C$ (Note 6)	47	52	57	47	52	57	KHz
	Voltage stability	$12 \leq V_i \leq 25V$		0.2	1		0.2	1	%
	Temperature stability	$T_{MIN} \leq T_{amb} \leq T_{MAX}$ (Note 2)		5			5		%
V_4	Amplitude	$V_{PIN\,4}$ peak to peak		1.7			1.7		V
ERROR AMP SECTION									
V_2	Input voltage	$V_{PIN\,1} = 2.5V$	2.45	2.50	2.55	2.42	2.50	2.58	V
I_b	Input bias current			-0.3	-1		-0.3	-2	μA
	A_{VOL}	$2 \leq V_o \leq 4V$	65	90		65	90		dB
B	Unity gain bandwidth	(Note 2)	0.7	1		0.7	1		MHz
SVR	Supply voltage rejection	$12 \leq V_i \leq 25V$	60	70		60	70		dB
I_o	Output sink current	$V_{PIN\,2} = 2.7V$ $V_{PIN\,1} = 1.1V$	2	6		2	6		mA
I_o	Output source current	$V_{PIN\,2} = 2.3V$ $V_{PIN\,1} = 5V$	-0.5	-0.8		-0.5	-0.8		mA
	V_{OUT} High	$V_{PIN\,2} = 2.3V$; $R_L = 15K\Omega$ to ground	5	6		5	6		V
	V_{OUT} Low	$V_{PIN\,2} = 2.7V$, $R_L = 15K\Omega$ to Pin 8		0.7	1.1		0.7	1.1	V

ELECTRICAL CHARACTERISTICS (continued)

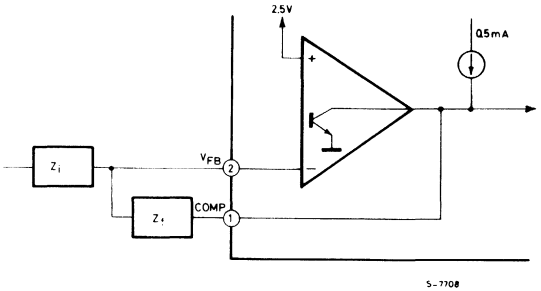
Parameter		Test Conditions	UC184X UC284X			UC384X			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
CURRENT SENSE SECTION									
G_v	Gain	(Notes 3 & 4)	2.85	3	3.15	2.85	3	3.15	V/V
V_3	Maximum input signal	V_{PIN1} = 5V (Note 3)	0.9	1	1.1	0.9	1	1.1	V
SVR	Supply voltage rejection	12 ≤ V_i ≤ 25V (Note 3)		70			70		dB
I_b	Input bias current			-2	-10		-2	-10	µA
	Delay to output			150	300		150	300	ns
OUTPUT SECTION									
I_{OL}	Output low level	I_{SINK} = 20mA		0.1	0.4		0.1	0.4	V
		I_{SINK} = 200mA		1.5	2.2		1.5	2.2	
I_{OH}	Output high level	I_{SOURCE} = 20mA	13	13.5		13	13.5		V
		I_{SOURCE} = 200mA	12	13.5		12	13.5		
t_r	Rise time	T_j = 25°C C_L = 1nF (Note 2)		50	150		50	150	ns
t_f	Fall time	T_j = 25°C C_L = 1nF (Note 2)		50	150		50	150	ns
UNDER-VOLTAGE LOCKOUT SECTION									
	Start threshold	X842/4	15	16	17	14.5	16	17.5	V
		X843/5	7.8	8.4	9.0	7.8	8.4	9.0	
	Min. operating voltage after turn-on	X842/4	9	10	11	8.5	10	11.5	V
		X843/5	7.0	7.6	8.2	7.0	7.6	8.2	
PWM SECTION									
	Maximum duty cycle	X842/3	95	97	100	95	97	100	%
		X844/5	46	48	50	47	48	50	
	Minimum duty cycle				0			0	%
TOTAL STANDBY CURRENT									
I_{st}	Start-Up current			0.5	1		0.5	1	mA
I_I	Operating supply current	V_{PIN2} = V_{PIN3} = 0V		11	17		11	17	mA
V_{IZ}	Zener voltage	I_I = 25mA		34			34		V

Notes: 2. These parameters, although guaranteed, are not 100% tested in production
3. Parameter measured at trip point of latch with V_{PIN2} = 0.
4. Gain defined as:

$$A = \frac{\Delta V_{PIN1}}{\Delta V_{PIN3}}; 0 \leq V_{PIN3} \leq 0.8V$$

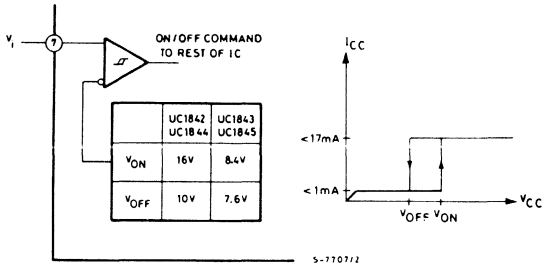
5. Adjust V_i above the start threshold before setting at 15V.
6. Output frequency equals oscillator frequency for the UC1842 and UC1843.
Output frequency is one half oscillator frequency for the UC1844 and UC1845.

Fig. 1 - Error amp configuration



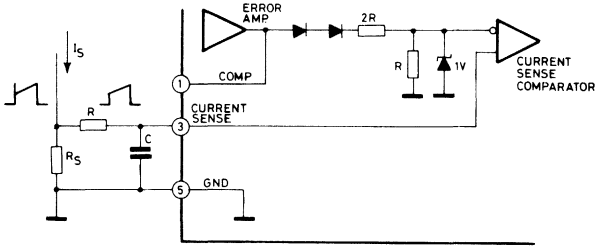
Error amp can source or sink up to 0.5mA

Fig. 2 - Under voltage lockout



During Under-Voltage Lockout, the output driver is biased to sink minor amounts of current. Pin 6 should be shunted to ground with a bleeder resistor to prevent activating the power switch with extraneous leakage currents.

Fig. 3 - Current sense circuit

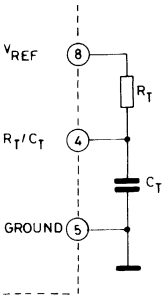


PEAK CURRENT (I_S) IS DETERMINED BY THE FORMULA

$$I_{S\,max} \approx \frac{1.0V}{R_S}$$

A SMALL RC FILTER MAY BE REQUIRED TO SUPPRESS SWITCH TRANSIENTS.

Fig. 4



for $R_T > 5K\Omega$ $f = \frac{1.72}{R_T C_T}$

Fig. 5 - Deadtime vs. C_T ($R_T > 5K\Omega$)

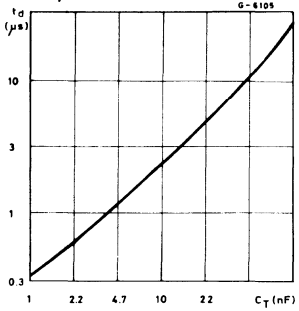


Fig. 6 - Timing resistance vs. frequency

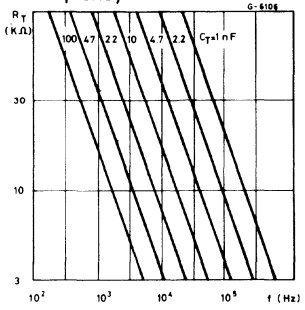


Fig. 7 - Output saturation characteristics

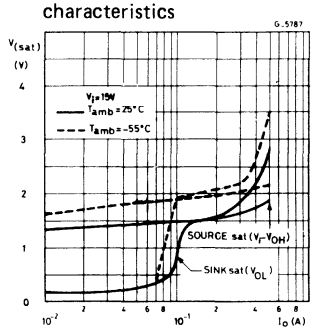


Fig. 8 - Error amplifier open-loop frequency response

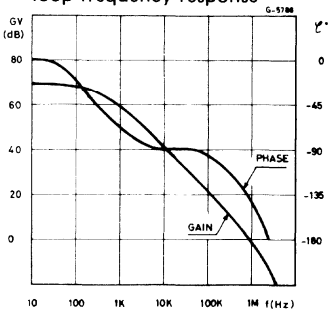
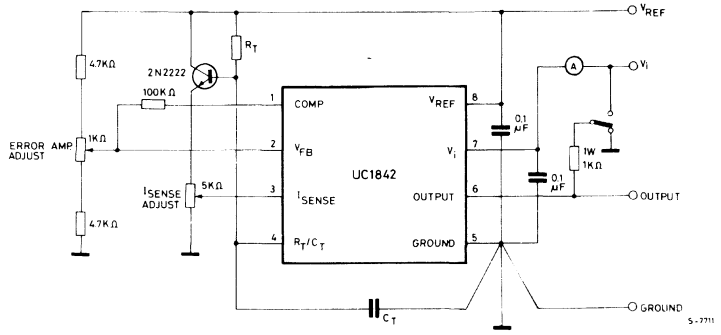


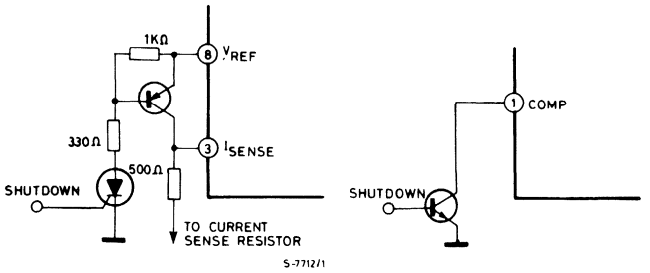
Fig. 9 - Open loop test circuit



High peak currents associated with capacitive loads necessitate careful grounding techniques Timing and bypass capacitors should be connected close to pin 5 in a single point ground.

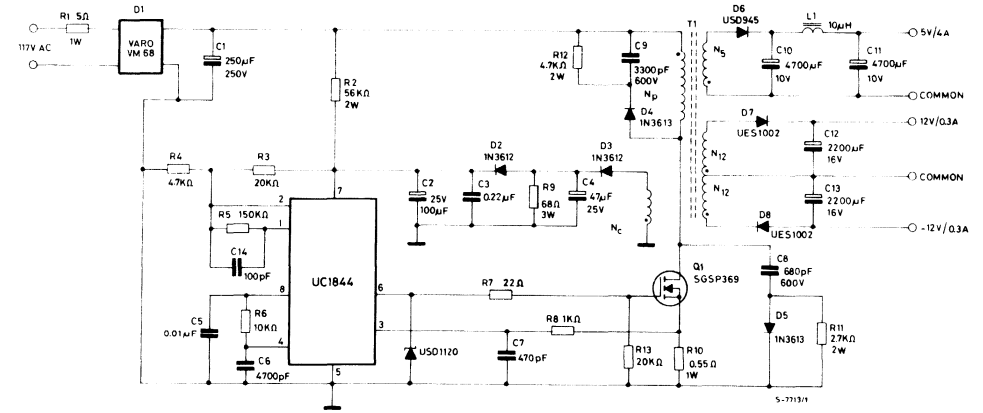
The transistor and 5KΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

Fig. 10 - Shutdown techniques



Shutdown of the UC1842 can be accomplished by two methods; either raise pin 3 above 1V or pull pin 1 below a voltage two diode drops above ground. Either method cause the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pins 1 and/or 3 is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR which will be reset by cycling V_i below the lower UVLO threshold. At this point the reference turns off, allowing the SCR to reset.

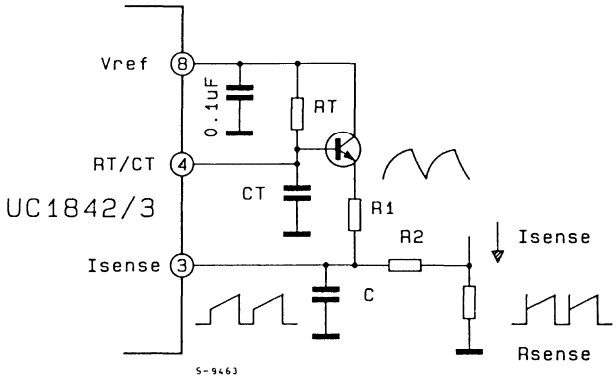
Fig. 11 - Off-line flyback regulator



Power Supply Specifications

1. Input Voltage: 95VAC to 130VAC (50Hz/60Hz)
2. Line Isolation: 3750V
3. Switching Frequency: 40KHz
4. Efficiency @ Full Load: 70%
5. Output Voltage:
   A. +5V, ±5%: 1A to 4A load
      Ripple voltage: 50mV P-P Max.
   B. +12V, ±3%: 0.1A to 0.3A load
      Ripple voltage: 100mV P-P Max.
   C. -12V, ±3%: 0.1A to 0.3A load
      Ripple voltage: 100mV P-P Max.

Fig. 12 - Slope compensation



A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%.

Note that capacitor, C, forms a filter with R_2 to suppress the leading edge switch spikes.

SEVEN DARLINGTON ARRAYS

- SEVEN DARLINGTONS PER PACKAGE
- OUTPUT CURRENT 500mA PER DRIVER (600mA PEAK)
- OUTPUT VOLTAGE 50V
- INTEGRAL SUPPRESSION DIODES FOR INDUCTIVE LOADS
- OUTPUTS CAN BE PARALLELED FOR HIGHER CURRENT
- TTL/CMOS/PMOS/DTL COMPATIBLE INPUTS
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY LAYOUT

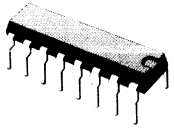
The ULN2001A, ULN2002A, ULN2003A and ULN2004A are high voltage, high current darlington arrays each containing seven open collector darlington pairs with common emitters. Each channel is rated at 500mA and can withstand peak currents of 600mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout.

The four versions interface to all common logic families:

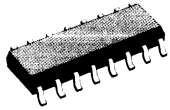
ULN2001A	General purpose, DTL, TTL, PMOS, CMOS
ULN2002A	14-25V PMOS
ULN2003A	5V TTL, CMOS
ULN2004A	6-15V CMOS, PMOS

These versatile devices are useful for driving a wide range of loads including solenoids, relays DC motors, LED displays filament lamps, thermal printheads and high power buffers.

The ULN2001A/2002A/2003A and 2004A are supplied in 16 pin plastic DIP packages with a copper leadframe to reduce thermal resistance. They are available also in small outline package (SO-16) as ULN2001D/2002D/2003D/2004D.



DIP-16 Plastic (0.25)



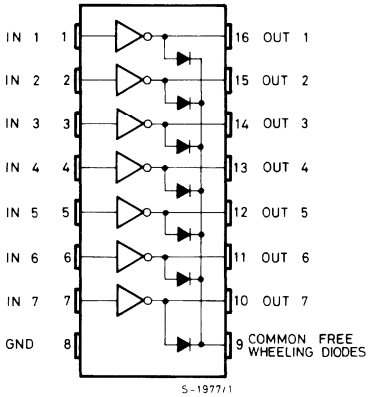
SO-16

ORDERING NUMBER:
ULN2001A/2A/3A/4A (DIP-16)
ULN2001D/2D/3D/4D (SO-16)

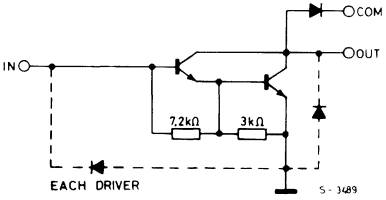
ABSOLUTE MAXIMUM RATINGS

V_o	Output voltage	50	V
V_{in}	Input voltage (for ULN2002A/D - 2003A/D - 2004A/D)	30	V
I_c	Continuous collector current	500	mA
I_b	Continuous base current	25	mA
T_{amb}	Operating ambient temperature range	-20 to 85	°C
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Junction temperature	150	°C

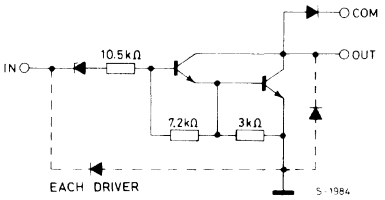
CONNECTION DIAGRAM



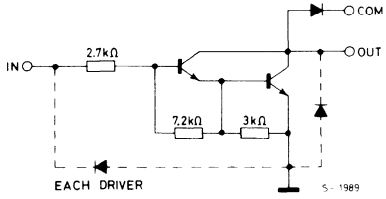
SCHEMATIC DIAGRAM



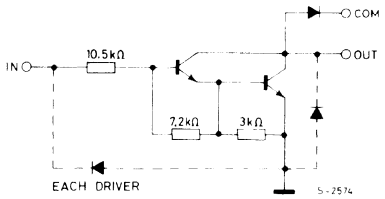
Series ULN-2001A
(each driver)



Series ULN-2002A
(each driver)



Series ULN-2003A
(each driver)



Series ULN-2004A
(each driver)

THERMAL DATA			DIP-16	SO-16
$R_{th\,j\text{-}amb}$	Thermal resistance junction-ambient	max	70°C/W	165°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output leakage current	V_{CE} = 50V				50	μA	1a
		T_{amb} = 70°C	V_{CE} = 50V			100	μA	1a
		T_{amb} = 70°C for **ULN2002A**						
		V_{CE} = 50V	V_i = 6V			500	μA	1b
		for **ULN2004A**						
		V_{CE} = 50V	V_i = 1V			500	μA	1b
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C = 100mA	I_B = 250 μA		0.9	1.1	V	2
		I_C = 200mA	I_B = 350 μA		1.1	1.3	V	2
		I_C = 350mA	I_B = 500 μA		1.3	1.6	V	2
$I_{i(on)}$	Input current	for **ULN2002A**	V_i = 17V		0.82	1.25	mA	3
		for **ULN2003A**	V_i = 3.85V		0.93	1.35	mA	3
		for **ULN2004A**	V_i = 5V		0.35	0.5	mA	3
		V_i = 12V			1	1.45	mA	3
$I_{i(off)}$	Input current	T_{amb} = 70°C	I_C = 500 μA	50	65		μA	4
$V_{i(on)}$	Input voltage	for **ULN2002A**						
		V_{CE} = 2V	I_C = 300 mA			13	V	5
		for **ULN2003A**						
		V_{CE} = 2V	I_C = 200 mA			2.4	V	5
		V_{CE} = 2V	I_C = 250 mA			2.7	V	5
		V_{CE} = 2V	I_C = 300 mA			3	V	5
		for **ULN2004A**						
		V_{CE} = 2V	I_C = 125 mA			5	V	5
		V_{CE} = 2V	I_C = 200 mA			6	V	5
		V_{CE} = 2V	I_C = 275 mA			7	V	5
		V_{CE} = 2V	I_C = 350 mA			8	V	5
h_{FE}	DC forward current gain	for **ULN2001A**						
		V_{CE} = 2V	I_C = 350 mA	1000			–	2
C_i	Input capacitance				15	25	pF	–
t_{PLH}	Turn-on delay time	0.5 V_i to 0.5 V_o			0.25	1	μs	–
t_{PHL}	Turn-off delay time	0.5 V_i to 0.5 V_o			0.25	1	μs	–
I_R	Clamp diode leakage current	V_R = 50V				50	μA	6
		T_{amb} = 70°C	V_R = 50V			100	μA	6
V_F	Clamp diode forward voltage	I_F = 350 mA			1.7	2	V	7

TEST CIRCUITS

Fig. 1a

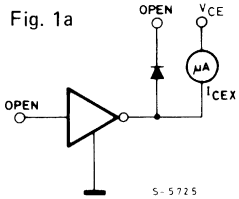


Fig. 1b

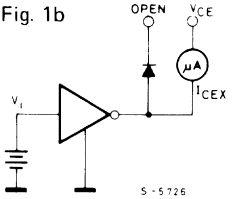


Fig. 2

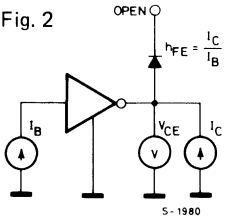


Fig. 3

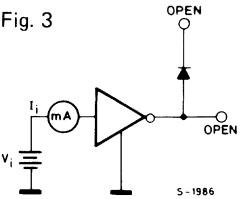


Fig. 4

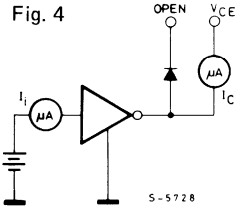


Fig. 5

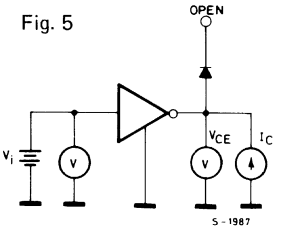


Fig. 6

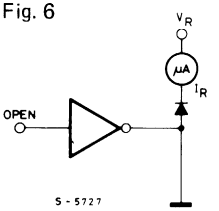
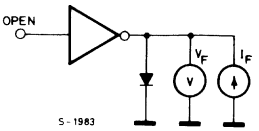


Fig. 7

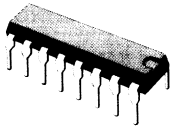


ULN2064B ULN2070B
ULN2066B ULN2074B
ULN2068B ULN2076B

50V - 1.5A QUAD DARLINGTON SWITCHES

- OUTPUT CURRENT TO 1.5A EACH DARLINGTON
- MINIMUM BREAKDOWN 50V
- SUSTAINING VOLTAGE AT LEAST 35V
- INTEGRAL SUPPRESSION DIODES (ULN2064B, ULN2066B, ULN2068B AND ULN2070B)
- ISOLATED DARLINGTON PINOUT (ULN2074B, ULN2076B)
- VERSIONS COMPATIBLE WITH ALL POPULAR LOGIC FAMILIES

Designed to interface logic to a wide variety of high current, high voltage loads, these devices each contain four NPN darlington switches delivering up to 1.5A with a specified minimum breakdown of 50V and a sustaining voltage of 35V measured at 100mA. The ULN2064B, ULN2066B, ULN2068B and ULN2070B contain integral suppression diodes for inductive loads have common emitters. The ULN2074B and ULN2076B feature isolated darlington pinouts and are intended for applications such as emitter follower configurations. Inputs of the ULN2064B, ULN2068B and ULN2074B are compatible with popular 5V logic families and the ULN2066B and ULN2076B are compatible with 6-15V CMOS and PMOS. Types ULN2068B and ULN2070B include a predriver stage to reduce loading on the control logic.

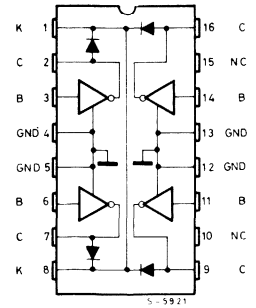


Powerdip (12 + 2 + 2)

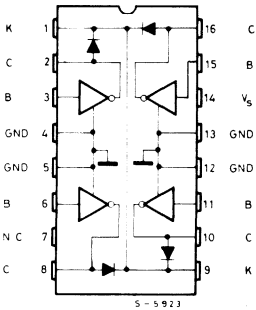
ABSOLUTE MAXIMUM RATINGS

V_{CEX}	Output voltage	50	V
$V_{CE\ (sus)}$	Output sustaining voltage	35	V
I_o	Output current	1.75	A
V_i	Input voltage for ULN2066B/70B/74B/76B	30	V
	for ULN2064B/68B	15	V
I_I	Input current	25	mA
V_s	Supply voltage for ULN2068B	10	V
	for ULN2070B	20	V
P_{tot}	Power dissipation: at T_{amb} = 90°C	4.3	W
	at T_{amb} = 70°C	1	W
T_{amb}	Operating ambient temperature range	-20 to 85	°C
T_{stg}	Storage temperature	-55 to 150	°C

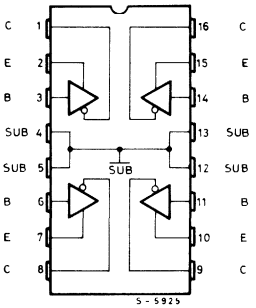
CONNECTION DIAGRAM (Top view) and ORDERING NUMBERS



ULN2064B
ULN2066B

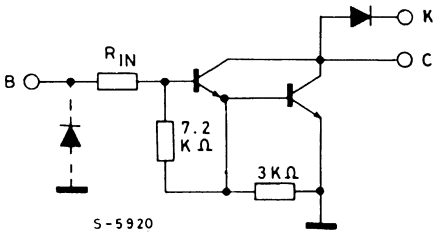


ULN2068B
ULN2070B



ULN2074B
ULN2076B

SCHEMATIC DIAGRAM



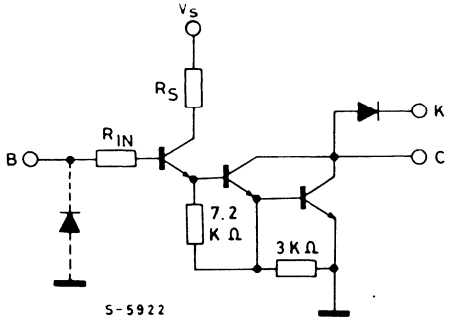
ULN2064B : R_{IN} = 350Ω
ULN2066B : R_{IN} = 3 kΩ

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.	Fig.
I_{CEX}	Output leakage current	for **ULN2064B-ULN2066B** V_{CE} = 50V V_{CE} = 50V T_{amb} = 70°C			 100 500	 µA µA	1
$V_{CE(sus)}$	Collector-emitter sustaining voltage	for **ULN2064B-ULN2066B** I_C = 100mA V_i = 0.4V	 35			 V	2
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C = 500mA I_B = 625µA I_C = 750mA I_B = 935µA I_C = 1A I_B = 1.25mA I_C = 1.25A I_B = 2mA			1.1 1.2 1.3 1.4	V V V V	3
$I_{i(on)}$	Input current	for **ULN2064B** V_i = 2.4V for **ULN2064B** V_i = 3.75V for **ULN2066B** V_i = 5V for **ULN2066B** V_i = 12V	1.4 3.3 0.6 1.7		4.3 9.6 1.8 5.2	mA mA mA mA	4
$V_{i(on)}$	Input voltage	for **ULN2064B** V_{CE} = 2V I_C = 1A V_{CE} = 2V I_C = 1.5A for **ULN2066B** V_{CE} = 2V I_C = 1A V_{CE} = 2V I_C = 1.5A			 2 2.5 6.5 10	 V V V V	5
t_{PLH}	Turn-on delay time	0.5V_i to 0.5V_o			1	µs	
t_{PHL}	Turn-off delay time	0.5V_i to 0.5V_o			1.5	µs	
I_R	Clamp diode leakage current	for **ULN2064B-ULN2066B** V_R = 80V V_R = 80V T_{amb} = 70°C			 50 100	 µA µA	6
V_F	Clamp diode forward voltage	I_F = 1A I_F = 1.5A			1.75 2	V V	7

NOTE: 1 – Input voltage is with reference to the substrate (no connection to any other pins) for the ULN2074B and ULN2076B reference is ground for all other types
2 – Input current may be limited by maximum allowable input voltage

SCHEMATIC DIAGRAM

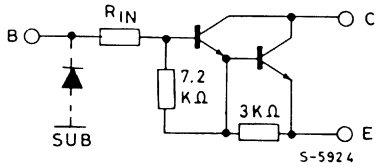


ULN2068B : R_{IN} = 2.5 kΩ R_s = 900Ω
ULN2070B : R_{IN} = 11.6 kΩ R_s = 3.4 KHΩ

ELECTRICAL CHARACTERISTICS (V_s = 5V for ULN2068B, V_s = 12V for ULN2070B, T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.	Fig.
I_{CEX}	Output leakage current	for **ULN2068B-ULN2070B** V_{CE} = 50V V_{CE} = 50V T_{amb} = 70°C			 100 500	 μA μA	1
$V_{CE(sus)}$	Collector-emitter sustaining voltage	for **ULN2068B-ULN2070B** I_C = 100mA V_i = 0.4V	35			V	2
$V_{CE(sat)}$	Collector-emitter saturation voltage	for **ULN2068B** I_C = 500 mA V_i = 2.75V I_C = 750mA V_i = 2.75V I_C = 1A V_i = 2.75V I_C = 1.25A V_i = 2.75V for **ULN2070B** I_C = 500mA V_i = 5V I_C = 750mA V_i = 5V I_C = 1A V_i = 5V I_C = 1.25A V_i = 5V			 1.1 1.2 1.3 1.4 1.1 1.2 1.3 1.4	 V V V V V V V V	2
$I_{i(on)}$	Input current	for **ULN2068B** V_i = 2.75V for **ULN2068B** V_i = 3.75V for **ULN2070B** V_i = 5V for **ULN2070B** V_i = 12V			550 1000 400 1250	μA μA μA μA	4
$V_{i(on)}$	Input voltage	V_{CE} = 2V I_C = 1.5A for **ULN2068B** for **ULN2070B**			 2.75 5	 V V	5
I_s	Supply current	for **ULN2068B** I_C = 500mA V_i = 2.75V for **ULN2070B** I_C = 500mA V_i = 5V			6 4.5	mA mA	8
t_{PLH}	Turn-on delay time	0.5V_i to 0.5V_o			1	μs	
t_{PHL}	Turn-off delay time	0.5V_i to 0.5V_o I_C = 1.25A			1.5	μs	
I_R	Clamp diode leakage current	for **ULN2068B-ULN2070B** V_R = 50V V_R = 50V T_{amb} = 70°C			 50 100	 μA μA	6
V_F	Clamp diode forward voltage	I_F = 1A I_F = 1.5A			1.75 2	V V	7

SCHEMATIC DIAGRAM



ULN2074B : R_{IN} = 350Ω
ULN2076B : R_{IN} = 3 kΩ

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.	Fig.
I_{CEX}	Output leakage current	for **ULN2074B-ULN2076B** V_{CE} = 50V V_{CE} = 50V T_{amb} = 70°C			 100 500	 µA µA	1
$V_{CE(sus)}$	Collector-emitter sustaining voltage	for **ULN2074B-ULN2076B** I_C = 100mA V_i = 0.4V	35			V	2
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C = 500mA I_B = 625µA I_C = 750mA I_B = 935µA I_C = 1A I_B = 1.25mA I_C = 1.25A I_B = 2mA			1.1 1.2 1.3 1.4	V V V V	3
$I_{i(on)}$	Input current	for **ULN2074B** V_i = 2.4V for **ULN2074B** V_i = 3.75V for **ULN2076B** V_i = 5V for **ULN2076B** V_i = 12V	1.4 3.3 0.6 1.7		4.3 9.6 1.8 5.2	mA mA mA mA	4
$V_{i(on)}$	Input voltage	for **ULN2074B** V_{CE} = 2V I_C = 1A V_{CE} = 2V I_C = 1.5A for **ULN2076B** V_{CE} = 2V I_C = 1A V_{CE} = 2V I_C = 1.5A			 2 2.5 6.5 10	 V V V V	5
t_{PLH}	Turn-on delay time	0.5V_i to 0.5V_o			1	µs	
t_{PHL}	Turn-off delay time	0.5V_i to 0.5V_o			1.5	µs	

TEST CIRCUITS

Fig. 1

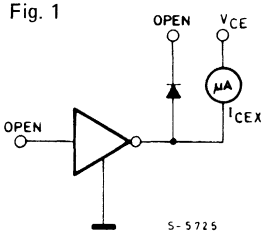


Fig. 2

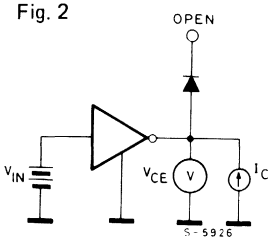


Fig. 3

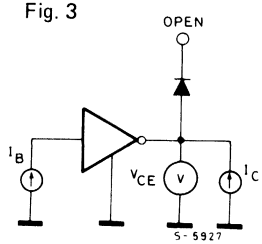


Fig. 4

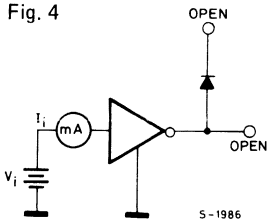


Fig. 5

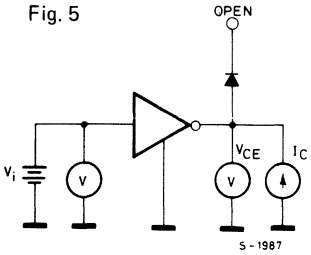


Fig. 6

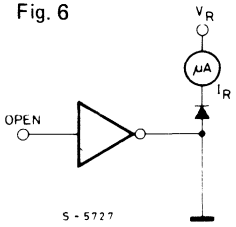


Fig. 7

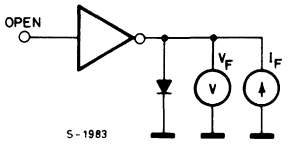


Fig. 8

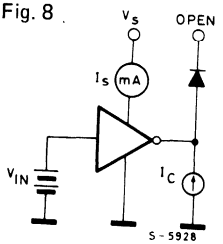


Fig. 9 - Input current as a function of input voltage

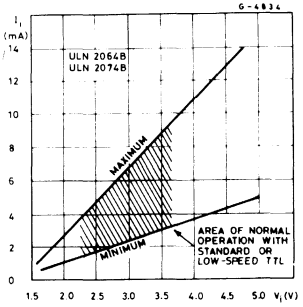


Fig. 10 - Input current as a function of input voltage

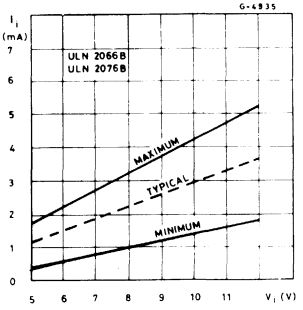
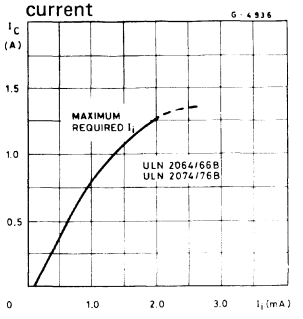


Fig. 11 - Collector current as a function of input current



TYPICAL APPLICATIONS

Fig. 12 - Common-anode LED drivers

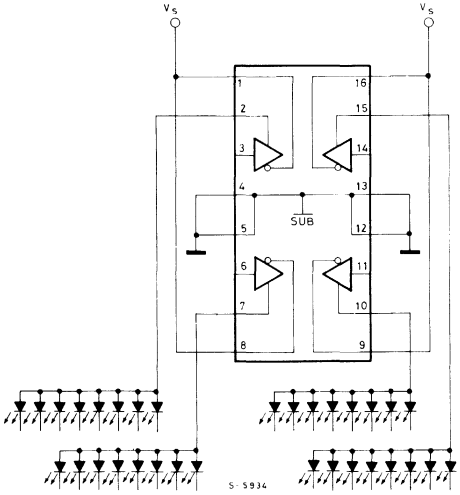
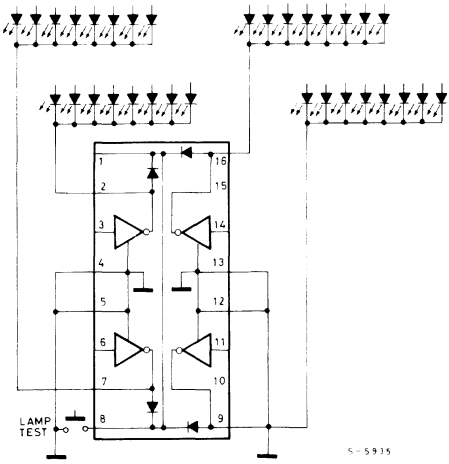


Fig. 13 - Common-cathode LED drivers



MOUNTING INSTRUCTIONS

The $R_{th\ j\text{-}amb}$ can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 14) or to an external heatsink (Fig. 15).
The diagram of figure 16 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "ℓ" of two equal square copper areas having a thickness of 35μ (1.4 mils).
During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.
The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 14 - Example of P.C. board copper area which is used as heatsink.

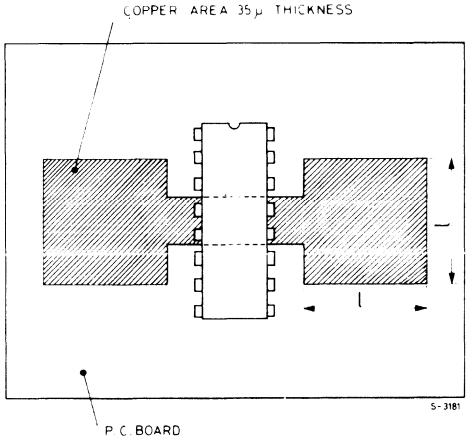


Fig. 15 - External heatsink mouting example

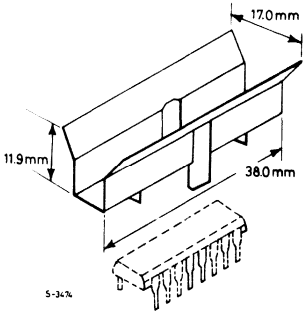


Fig. 16 - Maximum dissipable power and junction to ambient thermal resistance vs. side "ℓ"

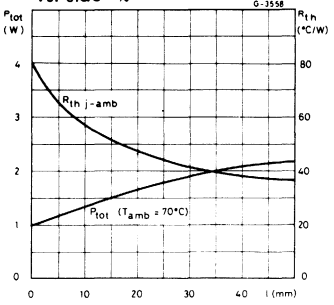
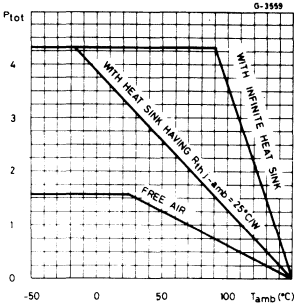


Fig. 17 - Maximum allowable power dissipation vs. ambient temperature



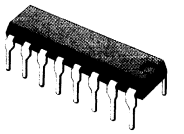
ULN2065B ULN2071B
ULN2067B ULN2075B
ULN2069B ULN2077B

PRELIMINARY DATA

80V - 1.5A QUAD DARLINGTON SWITCHES

- OUTPUT CURRENT TO 1.5A EACH DARLINGTON
- MINIMUM BREAKDOWN 80V
- SUSTAINING VOLTAGE AT LEAST 50V
- INTEGRAL SUPPRESSION DIODES (ULN2065B, ULN2067B, ULN2069B AND ULN2071B)
- ISOLATED DARLINGTON PINOUT (ULN2075B AND ULN2077B)
- VERSIONS COMPATIBLE WITH ALL POPULAR LOGIC FAMILIES

Designed to interface logic to a wide variety of high current, high voltage loads, these devices each contain four NPN darlington switches delivering up to 1.5A with a specified minimum breakdown of 80V and a sustaining voltage of 50V. The ULN2065B, ULN2067B, ULN2069B and ULN2071B contain integral suppression diodes for inductive loads and have common emitters; the ULN2075B and ULN2077B feature isolated darlington pinouts and are intended for applications such as emitter follower configurations. Inputs of the ULN2065B, ULN2069B and ULN2075B are compatible with popular 5V logic families and the ULN2067B, ULN2071B and ULN2077B are compatible with 6-15 CMOS and PMOS. The ULN2069B and ULN2071B include a predriver stage to provide extragain, reducing the load on control logic.

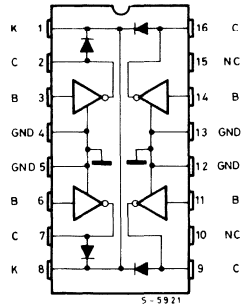


Powerdip (12 + 2 + 2)

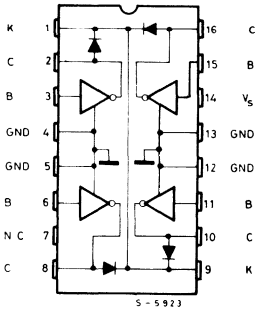
ABSOLUTE MAXIMUM RATINGS

V_{CEX}	Output voltage	80	V
$V_{CE\ (sus)}$	Output sustaining voltage	50	V
I_o	Output current	1.75	A
V_i	Input voltage for ULN2075B - 2077B	60	V
	for ULN2067B - 2071B	30	V
	for ULN2065B - 2069B	15	V
I_i	Input current	25	mA
V_s	Supply voltage for ULN2069B	10	V
	for ULN2071B	20	V
P_{tot}	Power dissipation: at $T_{pins} = 90°C$	4.3	W
	at $T_{amb} = 70°C$	1	W
T_{amb}	Operating ambient temperature range	-20 to 85	°C
T_{stg}	Storage temperature	-55 to 150	°C

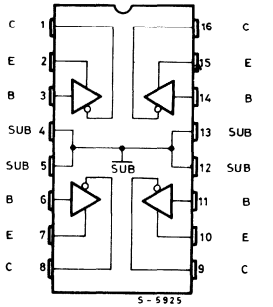
CONNECTIONS DIAGRAMS (Top view) and ORDERING NUMBERS



ULN2065B
ULN2067B

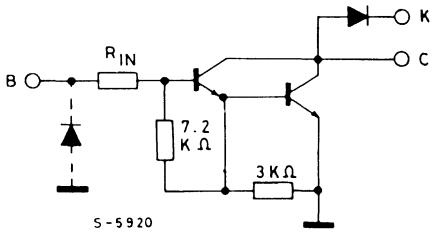


ULN2069B
ULN2071B



ULN2075B
ULN2077B

SCHEMATIC DIAGRAM



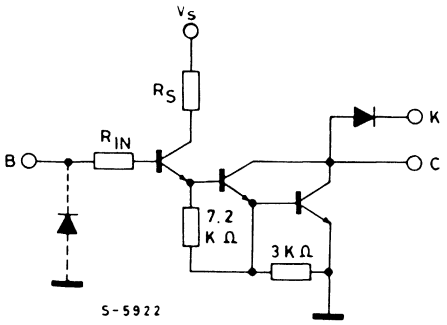
ULN2065B : R_{IN} = 350Ω
ULN2067B : R_{IN} = 3 kΩ

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.	Fig.
I_{CEX}	Output leakage current	for **ULN2065B-ULN2067B** V_{CE} = 80V V_{CE} = 80V T_{amb} = 70°C			 100 500	 µA µA	1
$V_{CE(sus)}$	Collector-emitter sustaining voltage	for **ULN2065B-ULN2067B** I_C = 100mA V_i = 0.4V	 50			 V	2
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C = 500mA I_B = 625µA I_C = 750mA I_B = 935µA I_C = 1A I_B = 1.25mA I_C = 1.25A I_B = 2mA for **ULN2065B-ULN2067B** I_C = 1.5A I_B = 2.25mA			1.1 1.2 1.3 1.4 1.5	V V V V V	3
$I_{i(on)}$	Input current	for **ULN2065B** V_i = 2.4V for **ULN2065B** V_i = 3.75V for **ULN2067B** V_i = 5V for **ULN2067B** V_i = 12V	1.4 3.3 0.6 1.7		4.3 9.6 1.8 5.2	mA mA mA mA	4
$V_{i(on)}$	Input voltage	for **ULN2065B** V_{CE} = 2V I_C = 1A V_{CE} = 2V I_C = 1.5A for **ULN2067B** V_{CE} = 2V I_C = 1A V_{CE} = 2V I_C = 1.5A			 2 2.5 6.5 10	 V V V V	5
t_{PLH}	Turn-on delay time	0.5V_i to 0.5V_o			1	µs	
t_{PHL}	Turn-off delay time	0.5V_i to 0.5V_o			1.5	µs	
I_R	Clamp diode leakage current	for **ULN2065B-ULN2067B** V_R = 80V V_R = 80V T_{amb} = 70°C			 50 100	 µA µA	6
V_F	Clamp diode forward voltage	I_F = 1A I_F = 1.5A			1.75 2	V V	7

NOTE: 1 – Input voltage is with reference to the substrate (no conection to any other pins) for the ULN2075B and ULN2077B reference is ground for all other types
2 – Input current may be limited by maximum allowable input voltage

SCHEMATIC DIAGRAM

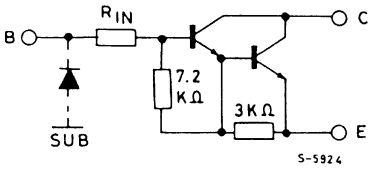


ULN2069B : R_{IN} = 2.5 kΩ, R_s = 900Ω
ULN2071B : R_{IN} = 11.6 kΩ, R_s = 3.4 kΩ

ELECTRICAL CHARACTERISTICS (V_s = 5V for ULN2069B, V_s = 12V for ULN2071B, T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.	Fig.
I_{CEX}	Output leakage current	for **ULN2069B-ULN2071B** V_{CE} = 80V V_{CE} = 80V T_{amb} = 70°C			 100 500	 µA µA	1
$V_{CE(sus)}$	Collector-emitter sustaining voltage	for **ULN2069B-ULN2071B** I_C = 100mA V_i = 0.4V	50			V	2
$V_{CE(sat)}$	Collector-emitter saturation voltage	for **ULN2069B** I_C = 500 mA V_i = 2.75V I_C = 750mA V_i = 2.75V I_C = 1A V_i = 2.75V I_C = 1.25A V_i = 2.75V I_C = 1.5A V_i = 2.75V for **ULN2071B** I_C = 500mA V_i = 5V I_C = 750mA V_i = 5V I_C = 1A V_i = 5V I_C = 1.25A V_i = 5V I_C = 1.5A V_i = 5V			 1.1 1.2 1.3 1.4 1.5 1.1 1.2 1.3 1.4 1.5	 V V V V V V V V V V	2
$I_{i(on)}$	Input current	for **ULN2069B** V_i = 2.75V for **ULN2069B** V_i = 3.75V for **ULN2071B** V_i = 5V for **ULN2071B** V_i = 12V			550 1000 400 1250	µA µA µA µA	4
$V_{i(on)}$	Input voltage	V_{CE} = 2V I_C = 1.5A for **ULN2069B** for **ULN2071B**			 2.75 5	 V	5
I_s	Supply current	for **ULN2069B** I_C = 500mA V_i = 2.75V for **ULN2071B** I_C = 500mA V_i = 5V			 6 4.5	 mA mA	8
t_{PLH}	Turn-on delay time	0.5V_i to 0.5V_o			1	µs	
t_{PHL}	Turn-off delay time	0.5V_i to 0.5V_o I_C = 1.25A			1.5	µs	
I_R	Clamp diode leakage current	for **ULN2069B-ULN2071B** V_R = 80V V_R = 80V T_{amb} = 70°C			 50 100	 µA µA	6
V_F	Clamp diode forward voltage	I_F = 1A I_F = 1.5A			1.75 2	V V	7

SCHEMATIC DIAGRAM



ULN2075B : R_{IN} = 350Ω
ULN2077B : R_{IN} = 3 kΩ

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.	Fig.
I_{CEX}	Output leakage current	for **ULN2075B-ULN2077B** V_{CE} = 80V V_{CE} = 80V T_{amb} = 70°C			 100 500	 μA μA	1
$V_{CE(sus)}$	Collector-emitter sustaining voltage	for **ULN2075B-ULN2077B** I_C = 100mA V_i = 0.4V	50			V	2
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C = 500mA I_B = 625μA I_C = 750mA I_B = 935μA I_C = 1A I_B = 1.25mA I_C = 1.25A I_B = 2mA for **ULN2075B-ULN2077B** I_C = 1.5A I_B = 2.25mA			1.1 1.2 1.3 1.4 1.5	V V V V V	3
$I_{i(on)}$	Input current	for **ULN2075B** V_i = 2.4V for **ULN2075B** V_i = 3.75V for **ULN2077B** V_i = 5V for **ULN2077B** V_i = 12V	1.4 3.3 0.6 1.7		4.3 9.6 1.8 5.2	mA mA mA mA	4
$V_{i(on)}$	Input voltage	for **ULN2075B** V_{CE} = 2V I_C = 1A V_{CE} = 2V I_C = 1.5A for **ULN2077B** V_{CE} = 2V I_C = 1A V_{CE} = 2V I_C = 1.5A			 2 2.5 6.5 10	 V V V V	5
t_{PLH}	Turn-on delay time	0.5V_i to 0.5V_o			1	μs	
t_{PHL}	Turn-off delay time	0.5V_i to 0.5V_o			1.5	μs	

TEST CIRCUITS

Fig. 1

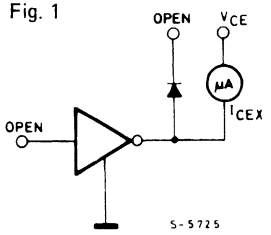


Fig. 2

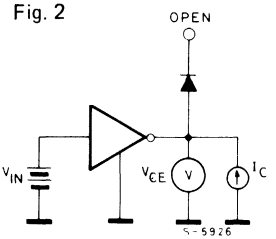


Fig. 3

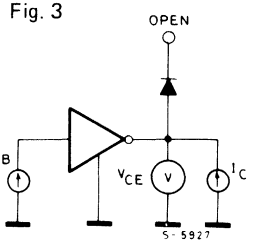


Fig. 4

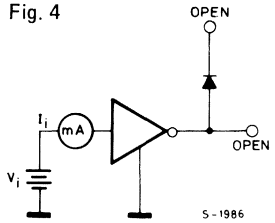


Fig. 5

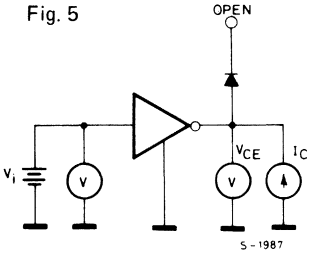


Fig. 6

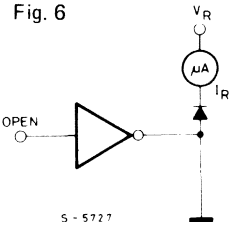


Fig. 7

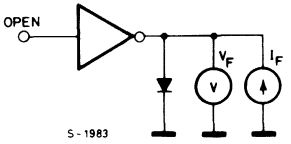


Fig. 8

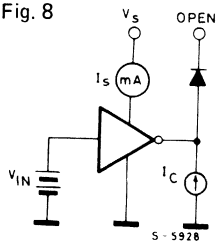


Fig. 9 - Input current as a function of input voltage

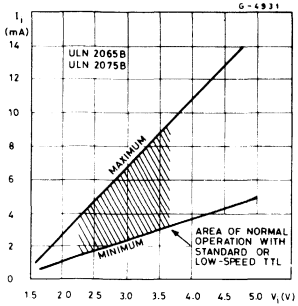


Fig. 10 - Input current as a function of input voltage

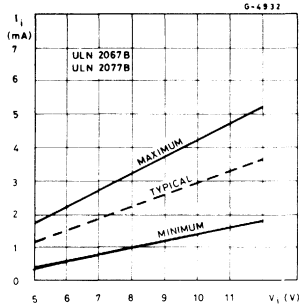
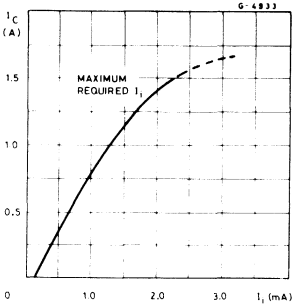


Fig. 11 - Collector current as a function of input current



MOUNTING INSTRUCTIONS

The $R_{th\ j\text{-}amb}$ can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 12) or to an external heatsink (Fig. 13).
The diagram of figure 14 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "ℓ" of two equal square copper areas having a thickness of 35μ (1.4 mils).
During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.
The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 12 - Example of P.C. board copper area which is used as heatsink.

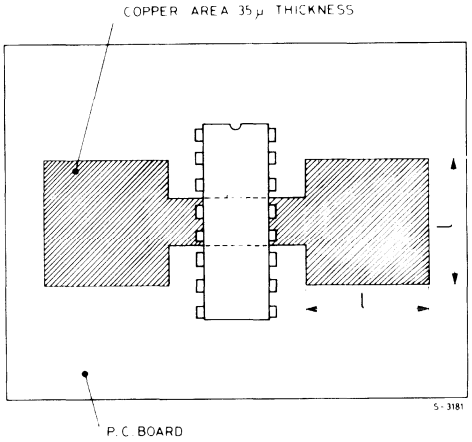


Fig.13 - External heatsink mounting example

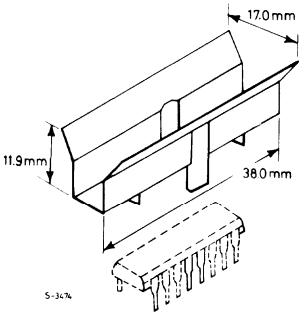


Fig. 14 - Maximum dissipable power and junction to ambient thermal resistance vs. side "ℓ"

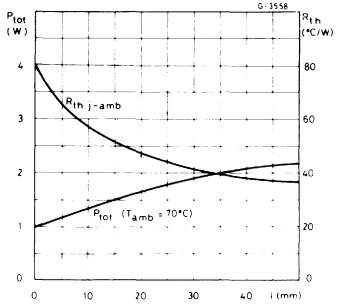
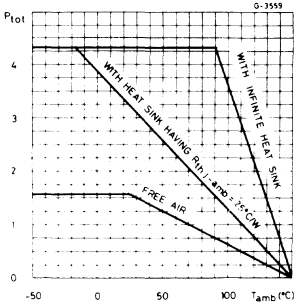


Fig. 15 - Maximum allowable power dissipation vs. ambient temperature



ULN2801A ULN2804A
ULN2802A ULN2805A
ULN2803A

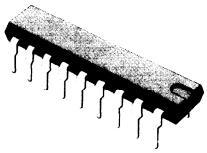
EIGHT DARLINGTON ARRAYS

- EIGHT DARLINGTONS WITH COMMON EMITTERS
- OUTPUT CURRENT TO 500mA
- OUTPUT VOLTAGE TO 50V
- INTEGRAL SUPPRESSION DIODES
- VERSIONS FOR ALL POPULAR LOGIC FAMILIES
- OUTPUT CAN BE PARALLELED
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY BOARD LAYOUT

The ULN2801A -ULN2805A each contain eight darlington transistors with common emitters and integral suppression diodes for inductive loads. Each darlington features a peak load current rating of 600mA (500mA continuous) and can withstand at least 50V in the off state. Outputs may be paralleled for higher current capability.

Five versions are available to simplify interfacing to standard logic families: the ULN2801A is designed for general purpose applications with a current limit resistor; the ULN2802A has a 10.5KΩ input resistor and zener for 14-25V PMOS; the ULN2803A has a 2.7KΩ input resistor for 5V TTL and CMOS; the ULN2804A has a 10.5KΩ input resistor for 6-15V CMOS and the ULN2805A is designed to sink a minimum of 350mA for standard and Schottky TTL where higher output current is required.

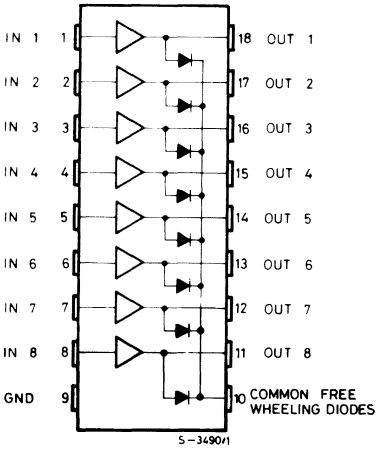
All types are supplied in a 18-lead plastic DIP with a copper lead from and feature the convenient input-opposite-output pinout to simplify board layout,



DIP-18 Plastic

CONNECTION DIAGRAM

(top view)

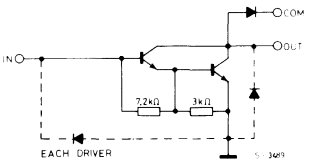


ABSOLUTE MAXIMUM RATINGS

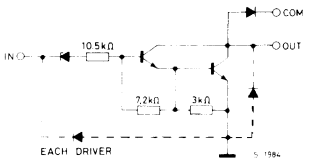
V_o	Output voltage	50	V
V_i	Input voltage for ULN 2802A, 2803A, 2804A	30	V
	for ULN 2805A	15	V
I_C	Continuous collector current	500	mA
I_B	Continuous base current	25	mA
P_{tot}	Power dissipation (one Darlington pair)	1.0	W
	(total package)	2.25	W
T_{amb}	Operating ambient temperature range	-20 to 85	°C
T_{stg}	Storage temperature range	-55 to 150	°C

SCHEMATIC DIAGRAMS

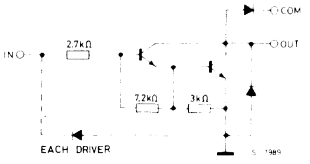
For ULN 2801A (each driver for PMOS-CMOS)



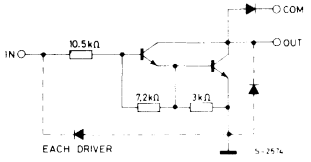
For ULN 2802A (each driver for 14-15V PMOS)



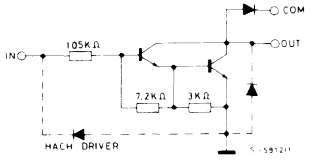
For ULN 2803A (each driver for 5V, TTL/CMOS)



For ULN 2804A (each driver for 6-15V CMOS/PMOS)



For ULN 2805A (each driver for high out TTL)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	55	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output leakage current	V_{CE} = 50V T_{amb} = 70°C V_{CE} = 50V T_{amb} = 70°C for **ULN 2802A** V_{CE} = 50V V_i = 6V for **ULN 2804A** V_{CE} = 50V V_i = 1V			50 100 500 500	µA µA µA µA	1a 1a 1b 1b
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C = 100 mA I_B = 250 µA I_C = 200 mA I_B = 350 µA I_C = 350 mA I_B = 500 µA		0.9 1.1 1.3	1.1 1.3 1.6	V V V	2
$I_{i(on)}$	Input current	for **ULN 2802A** V_i = 17V for **ULN 2803A** V_i = 3.85V for **ULN 2804A** V_i = 5V V_i = 12V for **ULN 2805A** V_i = 3V		0.82 0.93 0.35 1 1.5	1.25 1.35 0.5 1.45 2.4	mA mA mA mA mA	3
$I_{i(off)}$	Input current	T_{amb} = 70°C I_C = 500 µA	50	65		µA	4
$V_{i(on)}$	Input voltage	for **ULN 2802A** V_{CE} = 2V I_C = 300 mA for **ULN 2803A** V_{CE} = 2V I_C = 200 mA V_{CE} = 2V I_C = 250 mA V_{CE} = 2V I_C = 300 mA for **ULN 2804A** V_{CE} = 2V I_C = 125 mA V_{CE} = 2V I_C = 200 mA V_{CE} = 2V I_C = 275 mA V_{CE} = 2V I_C = 350 mA for **ULN 2805A** V_{CE} = 2V I_C = 350 mA			13 2.4 2.7 3 5 6 8 2.4	V V V V V V V V V	5
h_{FE}	DC forward current gain	for **ULN 2801A** V_{CE} = 2V I_C = 350 mA	1000				2
C_i	Input capacitance			15	25	pF	–
t_{PLH}	Turn-on delay time	0.5 V_i to 0.5 V_o		0.25	1	µs	–
t_{PHL}	Turn-off delay time	0.5 V_i to 0.5 V_o		0.25	1	µs	–
I_R	Clamp diode leakage current	V_R = 50V T_{amb} = 70°C V_R = 50V			50 100	µA µA	6
V_F	Clamp diode forward voltage	I_F = 350 mA		1.7	2	V	7

TEST CIRCUITS

Fig. 1a

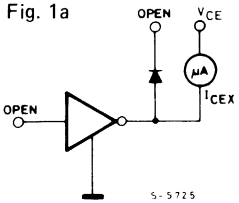


Fig. 1b

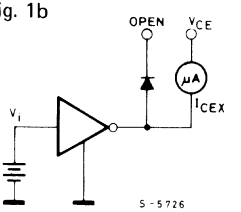


Fig. 2

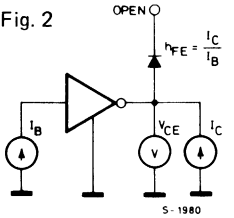


Fig. 3

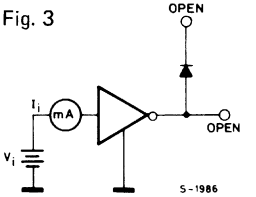


Fig. 4

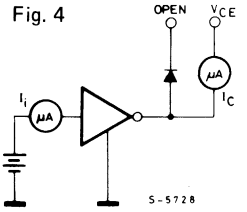


Fig. 5

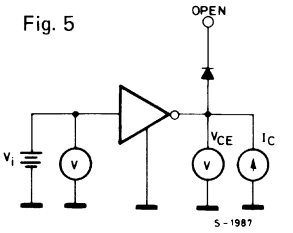


Fig. 6

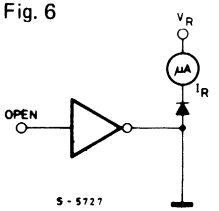


Fig. 7

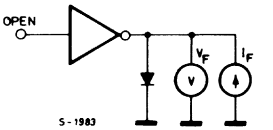


Fig. 8 - Collector current as a function of saturation voltage

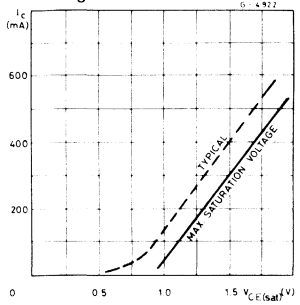


Fig. 9 - Collector current as a function of input current

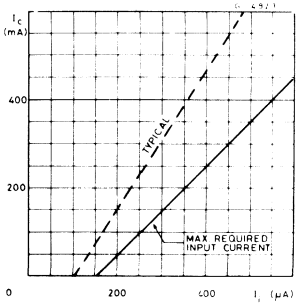


Fig. 10 - Allowable average power dissipation as a function of ambient temperature

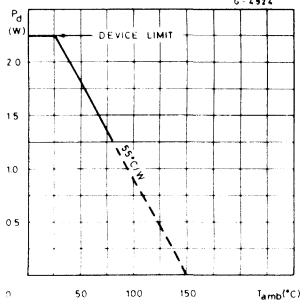


Fig. 11 - Peak collector current as a function of duty cycle

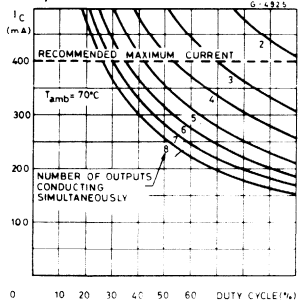


Fig. 12 - Peak collector current as a function of duty cycle

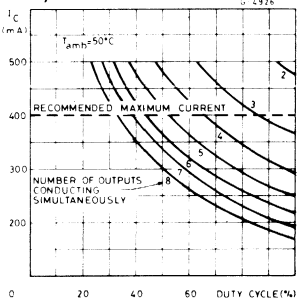


Fig. 13 - Input current as a function of input voltage (for ULN 2802A)

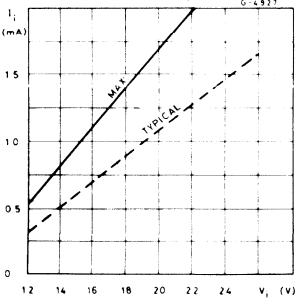


Fig. 14 - Input current as a function of input voltage (for ULN 2804A)

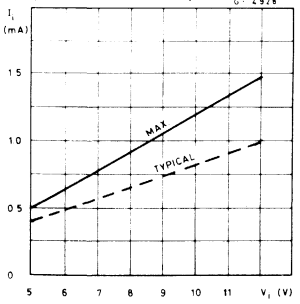


Fig. 15 - Input current as a function of input voltage (for ULN 2803A)

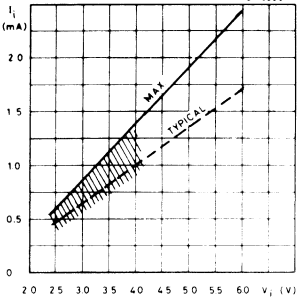
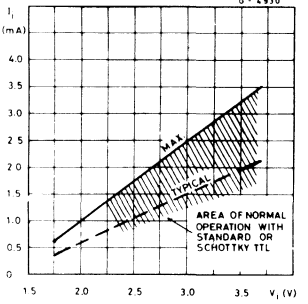


Fig. 16 - Input current as a function of input voltage (for ULN 2805A)



ULQ2001R
ULQ2002R
ULQ2003R
ULQ2004R

SEVEN DARLINGTON ARRAYS

- SEVEN DARLINGTONS PER PACKAGE
- OUTPUT CURRENT 500mA PER DRIVER (600mA PEAK)
- OUTPUT VOLTAGE 50V
- INTEGRAL SUPPRESSION DIODES FOR INDUCTIVE LOADS
- OUTPUTS CAN BE PARALLELED FOR HIGHER CURRENT
- TTL/CMOS/PMOS/DTL COMPATIBLE INPUTS
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY LAYOUT

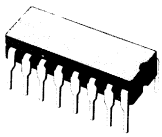
The ULQ2001R, ULQ2002R, ULQ2003R and ULQ2004R are high voltage, high current darlington arrays each containing seven open collector darlington pairs with common emitters. Each channel is rated at 500mA and can withstand peak currents of 600mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout.

The four versions interface to all common logic families.

ULQ2001R	General purpose, DTL, TTL, CMOS
ULQ2002R	14-25V PMOS
ULQ2003R	5V TTL, CMOS
ULQ2004R	6-15V CMOS, PMOS

These versatile devices are useful for driving a wide range of loads including solenoids, relays DC motors, LED displays, filament lamps, thermal printheads and high power buffers.

The ULQ2001R, ULQ2002R, ULQ2003R and ULQ2004R are supplied in 16 pin ceramic DIP packages.

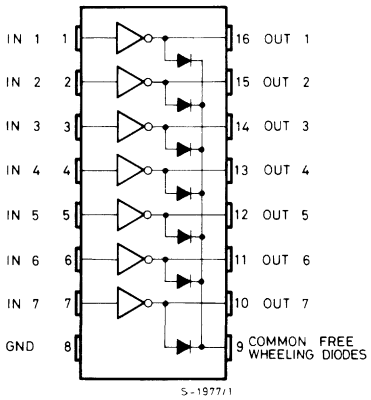


DIP-16 Ceramic

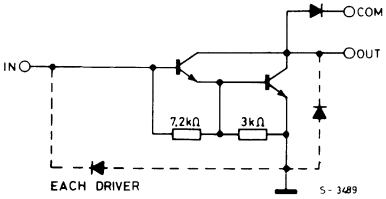
ABSOLUTE MAXIMUM RATINGS

V_o	Output voltage	50	V
V_{in}	Input voltage (for ULQ2002R/2003R/2004R)	30	V
I_c	Continuous collector current	500	mA
I_b	Continuous base current	25	mA
T_{amb}	Operating ambient temperature range	-20 to + 85	°C
T_{stg}	Storage temperature range	-55 to 150	°C

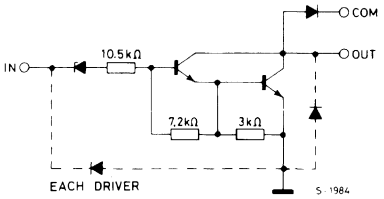
CONNECTION DIAGRAM



SCHEMATIC DIAGRAM



Series ULQ2001R
(each driver)



Series ULQ2002R
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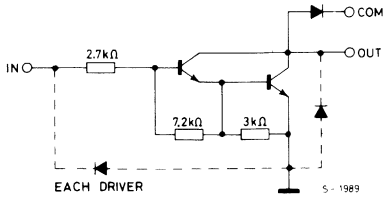

Series ULQ2003R
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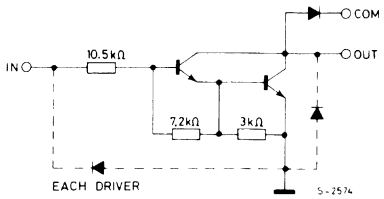


Series ULQ2004R
(each driver)

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	150	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output leakage current	V_{CE} = 50V				50	μA	1a
		T_{amb} = 70°C	V_{CE} = 50V			100	μA	1a
		T_{amb} = 70°C for **ULQ2002R**						
		V_{CE} = 50V	V_i = 6V			500	μA	1b
		for **ULQ2004R**						
		V_{CE} = 50V	V_i = 1V			500	μA	1b
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C = 100mA	I_B = 250 μA		0.9	1.1	V	2
		I_C = 200mA	I_B = 350 μA		1.1	1.3	V	2
		I_C = 350mA	I_B = 500 μA		1.3	1.6	V	2
$I_{i(on)}$	Input current	for **ULQ2002R**	V_i = 17V		0.82	1.25	mA	3
		for **ULQ2003R**	V_i = 3.85V		0.93	1.35	mA	3
		for **ULQ2004R**	V_i = 5V		0.35	0.5	mA	3
		V_i = 12V			1	1.45	mA	3
$I_{i(off)}$	Input current	T_{amb} = 70°C	I_C = 500 μA	50	65		μA	4
$V_{i(on)}$	Input voltage	for **ULQ2002R**						
		V_{CE} = 2V	I_C = 300 mA			13	V	5
		for **ULQ2003R**						
		V_{CE} = 2V	I_C = 200 mA			2.4	V	5
		V_{CE} = 2V	I_C = 250 mA			2.7	V	5
		V_{CE} = 2V	I_C = 300 mA			3	V	5
		for **ULQ2004R**						
		V_{CE} = 2V	I_C = 125 mA			5	V	5
		V_{CE} = 2V	I_C = 200 mA			6	V	5
		V_{CE} = 2V	I_C = 275 mA			7	V	5
		V_{CE} = 2V	I_C = 350 mA			8	V	5
h_{FE}	DC forward current gain	for **ULQ2001R**						
		V_{CE} = 2V	I_C = 350 mA	1000			–	2
C_i	Input capacitance				15	25	pF	–
t_{PLH}	Turn-on delay time	0.5 V_i to 0.5 V_o			0.25	1	μs	–
t_{PHL}	Turn-off delay time	0.5 V_i to 0.5 V_o			0.25	1	μs	–
I_R	Clamp diode leakage current	V_R = 50V				50	μA	6
		T_{amb} = 70°C	V_R = 50V			100	μA	6
V_F	Clamp diode forward voltage	I_F = 350 mA			1.7	2	V	7

TEST CIRCUITS

Fig. 1a

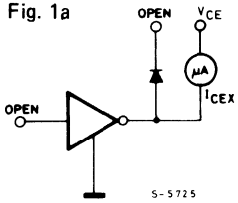


Fig. 1b

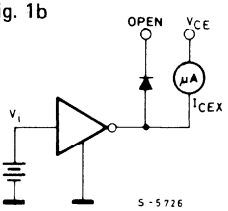


Fig. 2

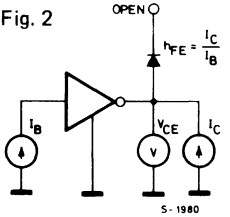


Fig. 3

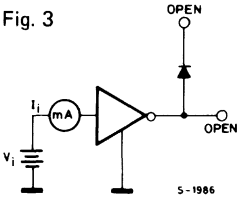


Fig. 4

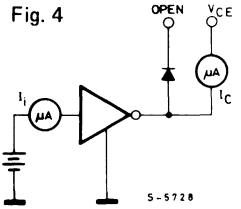


Fig. 5

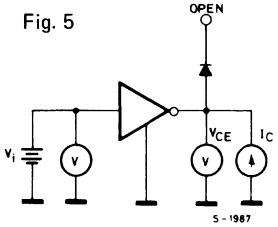


Fig. 6

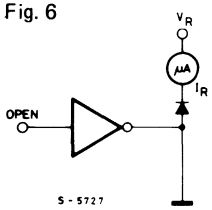
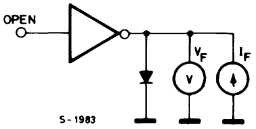
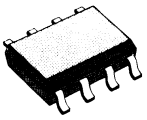


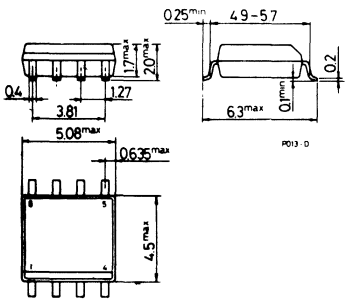
Fig. 7



PACKAGES

SO-8





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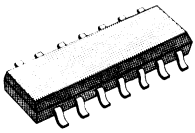

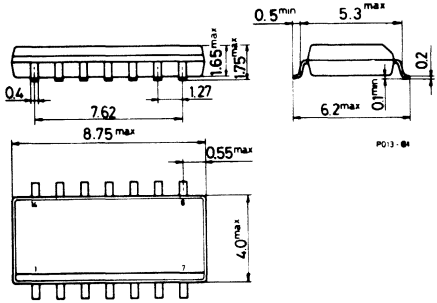

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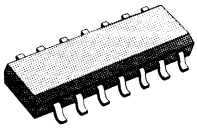

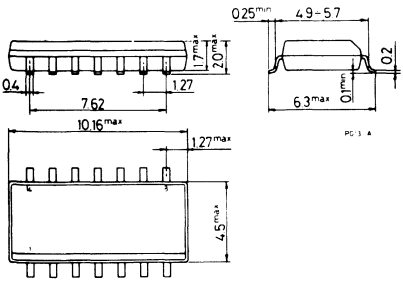

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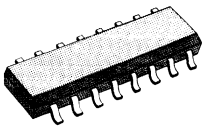
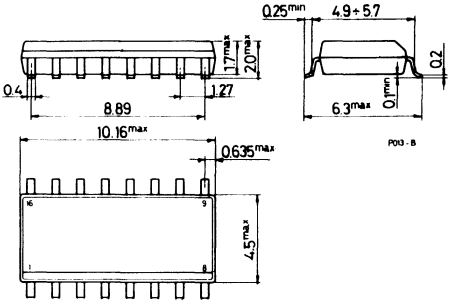
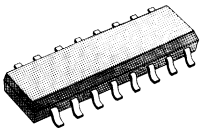
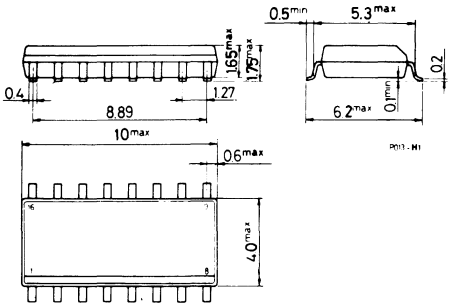




PACKAGES

SO-16 Jedec





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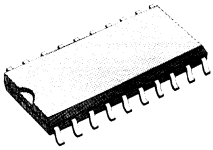
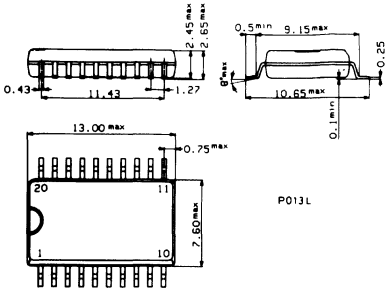
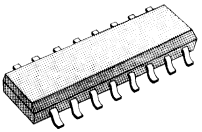
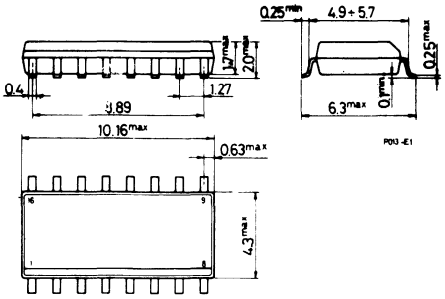


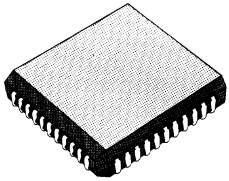


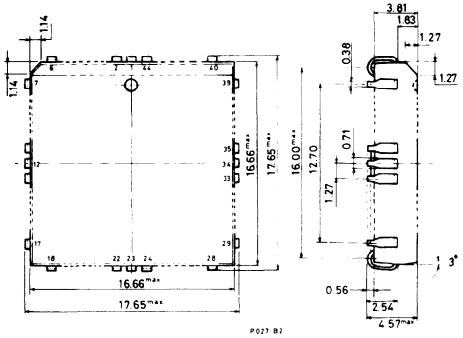
SO-16P



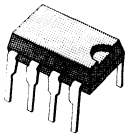


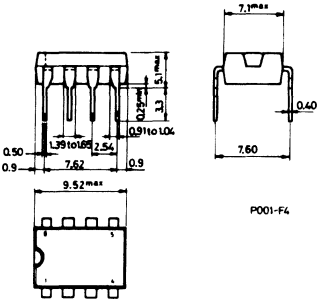
PLCC-44 Plastic Chip Carrier



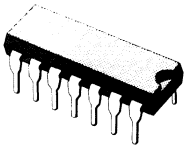


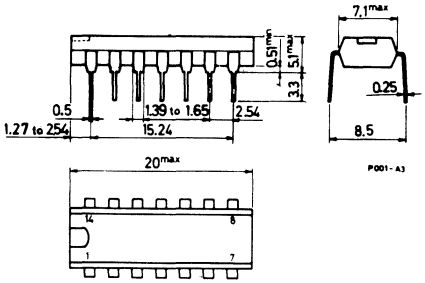
8 lead Plastic Minidip
4 + 4 lead Powerdip



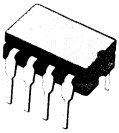


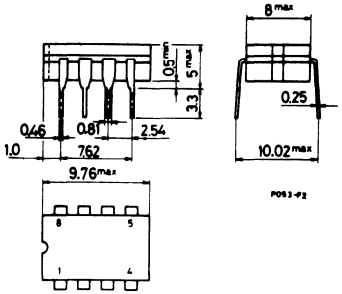
14 lead Plastic Dip



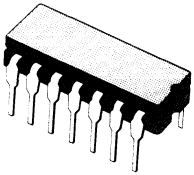


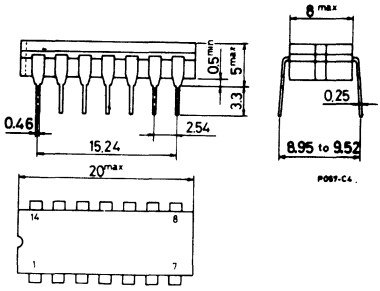
8 lead Ceramic Minidip





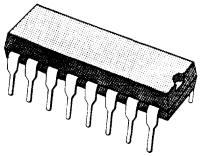
14 lead Ceramic Dip

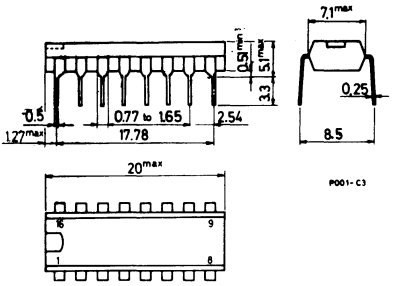




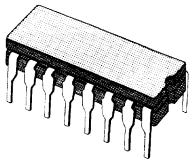
PACKAGES

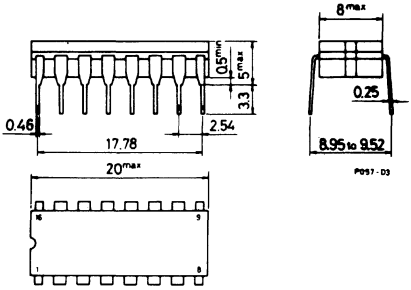
16 lead Plastic Dip (0.25)



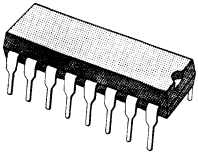


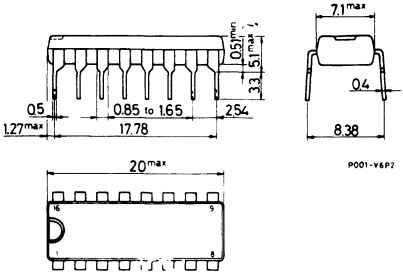
16 lead Ceramic Dip



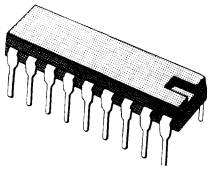


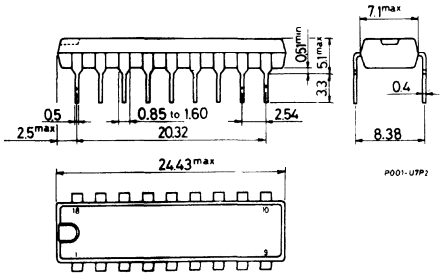
16 lead Plastic Dip (0.4)
8 + 8 lead Powerdip
12 + 2 + 2 lead Powerdip



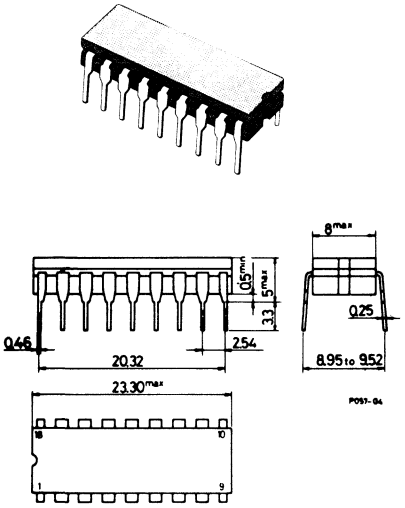


18 lead Plastic Dip (0.4)
12 + 3 + 3 lead Powerdip
9 + 9 lead Powerdip

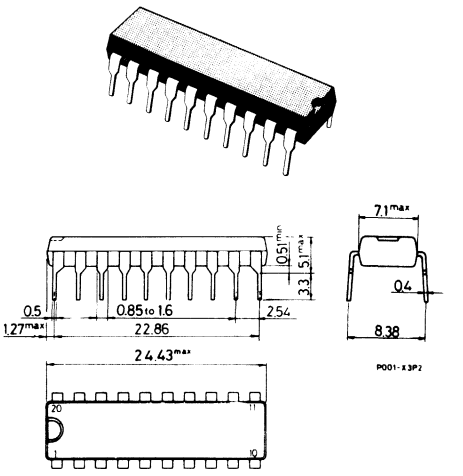




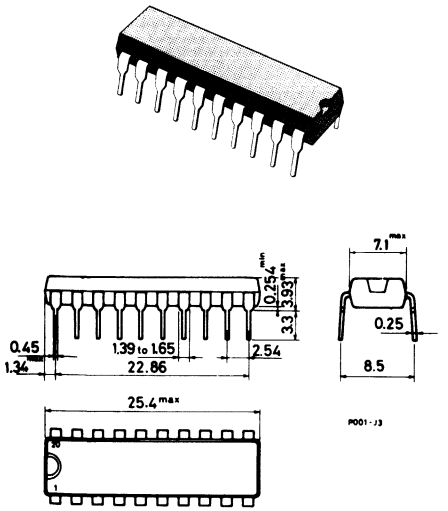
18 lead Ceramic Dip



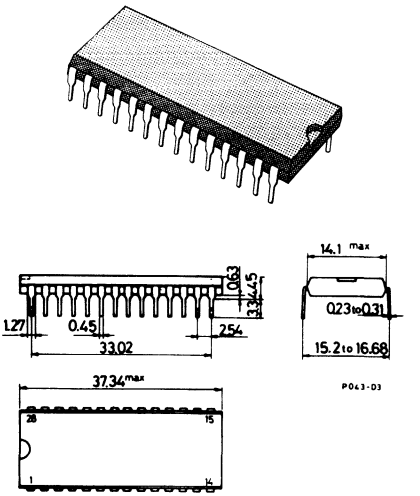
20 lead Plastic Dip (0.4)
16 + 2 + 2 Powerdip



20 lead Plastic Dip (0.25)

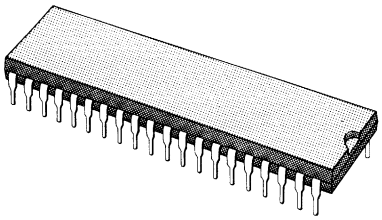


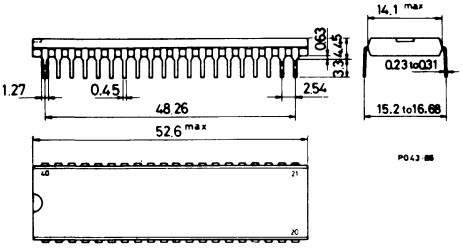
28 lead Plastic Dip



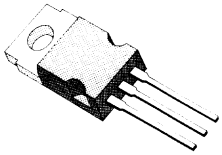
PACKAGES

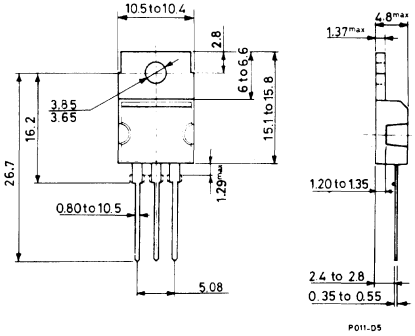
40 lead Plastic Dip



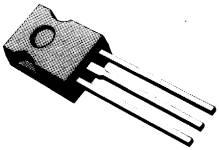


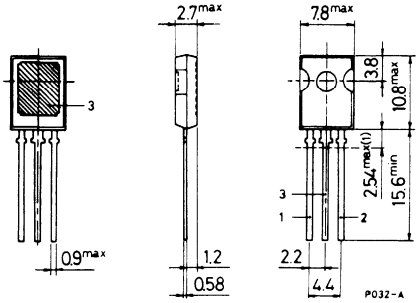
TO-220





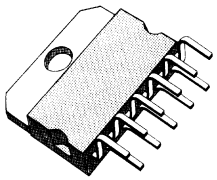
SOT-82

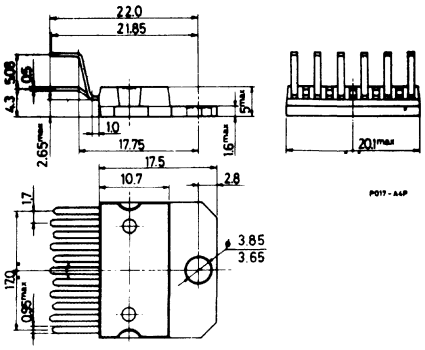




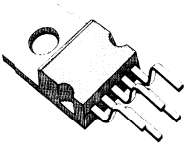
(1) Within this region the cross-section of the leads is uncontrolled

MULTIWATT-11

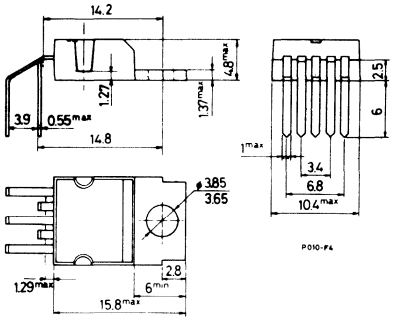




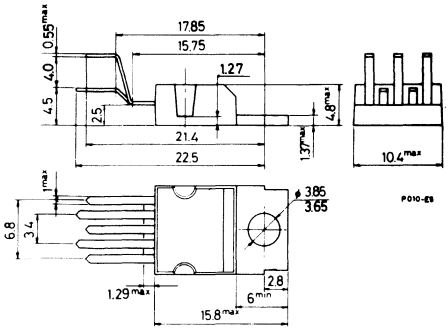
PENTAWATT



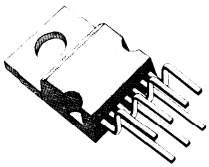
Horizontal Version



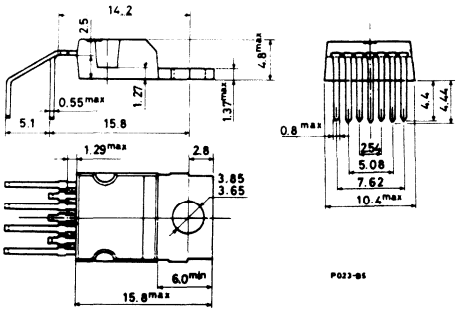
Vertical Version



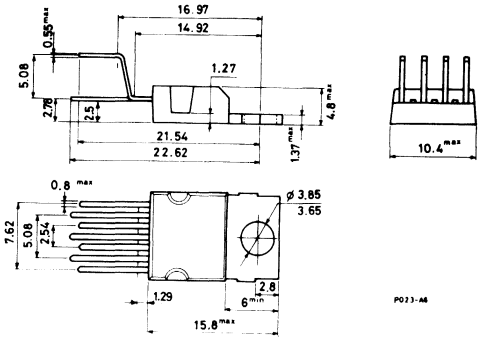
HEPTAWATT



Horizontal Version

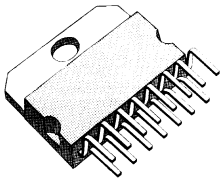


Vertical Version



PACKAGES

MULTIWATT-15



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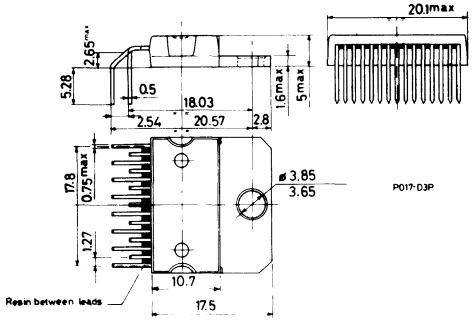

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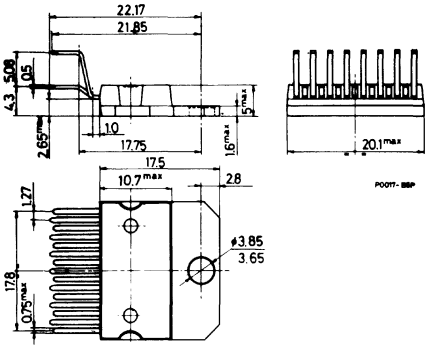
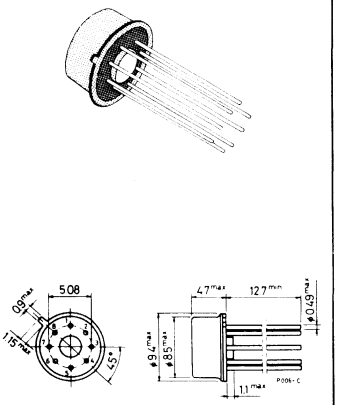
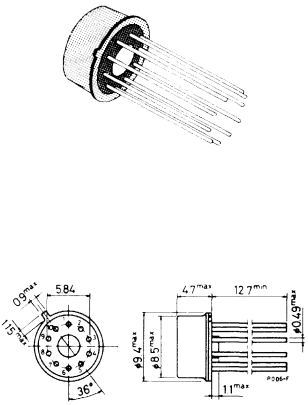


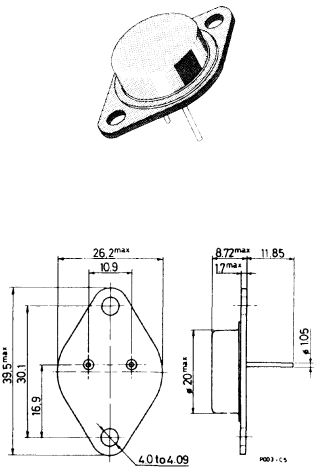
TO-99 (8 Pin)



TO-100 (10 Pin)



TO-3



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